X 1215

Cartridge Disk Drive Unit

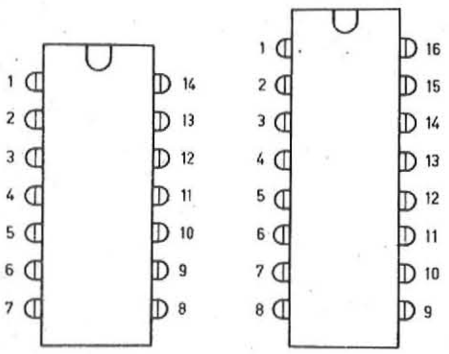
Vol. IV: Diagrams

Data
Systems

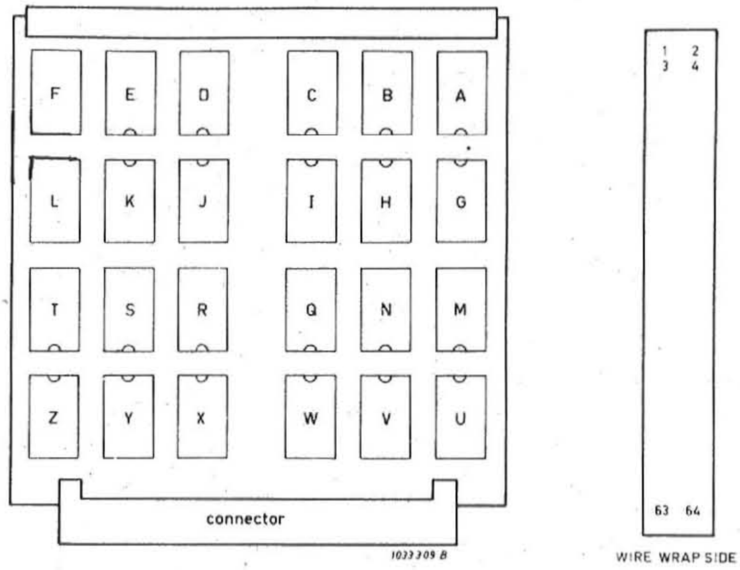
1. KEY TO DIAGRAMS.

1-1 GENERAL

The key to logic refers to the logic circuits on the printed circuit boards (figure 4-1). The voltage levels used in the CDD are +5V for a logic "1" and OV for a logic "O".
Each printed circuit board has a 64 pin female connector on which pin 2 is used for +5V and pins 4, 14, 26, 40, 52 and 64 are used for logical earth. The logic used in the CDD is generally called TTL (Transistor - Transistor Logic) consisting of integrated circuits. These integrated circuits are contained in "dual in line" packages with 14 pin or 16 pin connections (figure 4-1A). Discrete component circuits containing separate resistors, capacitors, transistors or diodes are also sometimes used.
Figure 4-1B shows the organisation of component location on the printed circuit boards.



A



B

Figure 4-1

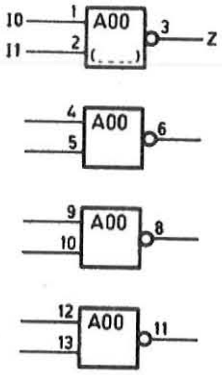
1-2 LOGIC SYMBOLS

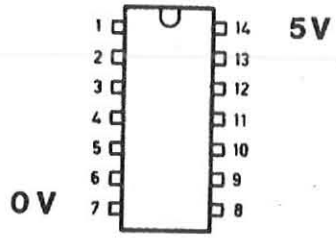
Function name : A00

Code number : 9330 500 71XX0

Supplier type : FJH131; 7400; 9N00

Drawing symbol :





Description :

The A00 comprises four, independent NAND-gates, each provided with two inputs and a totem pole output stage.

Logic function:

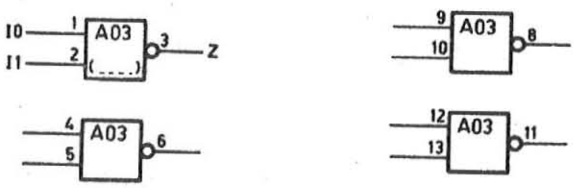
$Z = \overline{I0.I1}$

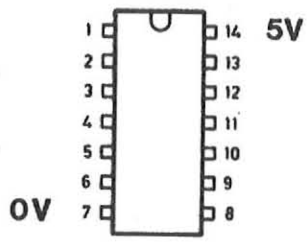
Function name : A03

Code number : 9331 935 30XX0

Supplier type : 74132

Drawing symbol :





Description :

The A03 comprises four, independent NAND-gates, each provided with two inputs Schmitt trigger and a totem pole output stage.

Logic function :

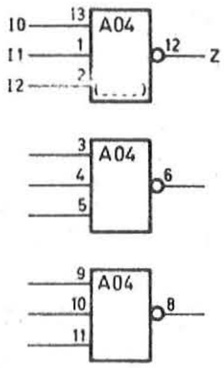
$Z = \overline{I_0 \cdot I_1}$

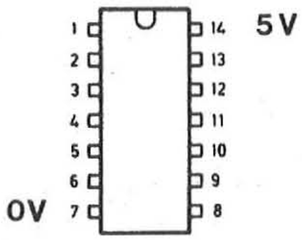
Function name : A04

Code number : 9330 500 31XX0

Supplier type : FJH121 ; 7410 ; 9N10

Drawing symbol :





Description :

The A04 comprises three, independent NAND-gates, each provided with three inputs and a totem pole output stage.

Logic function :

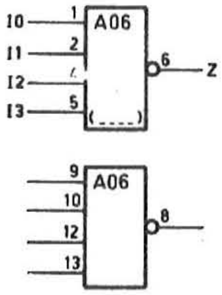
$Z = \overline{I_0 \cdot I_1 \cdot I_2}$

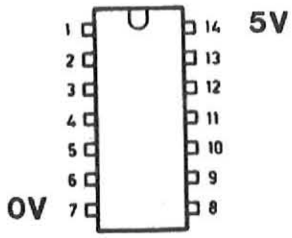
Function name : A06

Code number : 9330 499 91XX0

Supplier type : FJH111; 7420; 9N20

Drawing symbol :





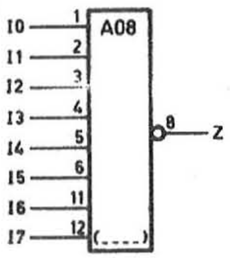
Description :

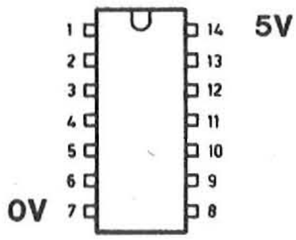
The A06 comprises two independent NAND-gates, each provided with four inputs and a totem pole output stage.

Logic function :

$Z = \overline{I_o \cdot I_1 \cdot I_2 \cdot I_3}$

Function name	:	A08
Code number	:	9330 499 51XX0
Supplier type	:	FJH101 ; 7430 ; 9N30
Drawing symbol	:	





Description :

The A08 comprises one NAND-gate, with eight inputs and a totem pole output stage.

Logic function :

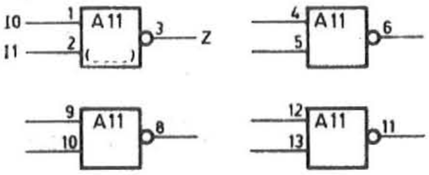
$Z = \overline{I_o \cdot I_1 \cdot I_2 \cdot I_3 \cdot I_4 \cdot I_5 \cdot I_6 \cdot I_7}$

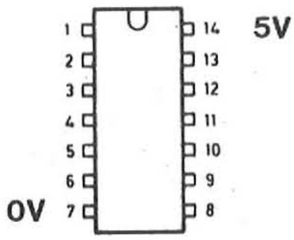
Function name : A11

Code number : 9331 719 20XX0

Supplier type : 7438 ; 9N38

Drawing symbol :





Description :

The A11 comprises four, independent NAND-gates, each provided with two inputs and an open collector output stage.

Logic function :

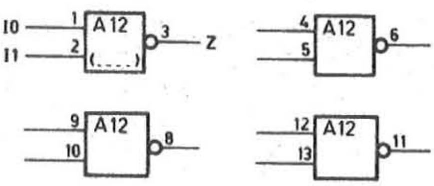
$Z = \overline{I_o \cdot I_1}$

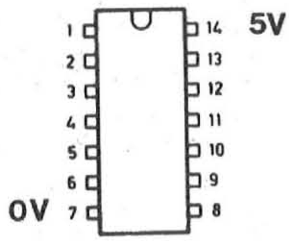
Function name : A12

Code number : 5122 000 05831

Supplier type : 74H00 ; 9H00

Drawing symbol :





Description :

The A12 comprises four, independent, high speed NAND-gates, each provided with two inputs and a totem pole output stage.

Logic function :

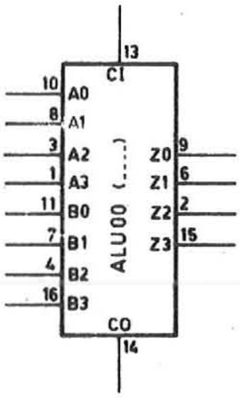
$Z = \overline{I_o \cdot I_1}$

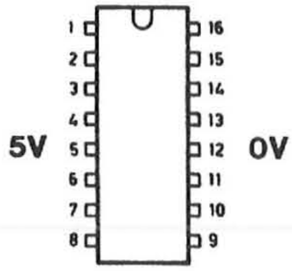
Function name : ALU00

Code number : 9330 649 50XX0

Supplier type : FJH211; 7483; 9383

Drawing symbol :





Description :

The ALU00 comprises a full adder for two 4-bit binary numbers (A0 through A3 and B0 through B3) plus a carry input CI. Four outputs (Z0 through Z3) are provided for each bit and the carry output CO is obtained from the last bit.

Function table:

The function table is presented in two parts for simplicity:

- Input conditions at A0, A1, B0, B1 and CI determine the outputs Z0 and Z1 together with the internal carry C1 obtained from this addition.
- Input conditions at A2, A3, B2, B3 and the internal carry C1 determine the outputs Z2, Z3 and CO.

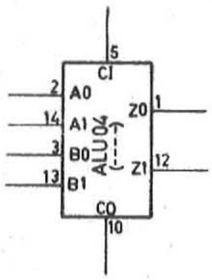
Input				Output CI=0 C1=0			CI=1 C1=		
A0 / A2	B0 / B2	A1 / A3	B1 / B3	Z0 / Z2	Z1 / Z3	C1 / C0	Z0 / Z2	Z1 / Z3	C1 / C0
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

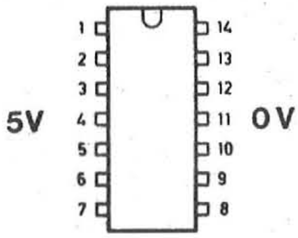
Function name : ALU04

Code number :

Supplier type : FJH201; 7482; 9382

Drawing symbol :





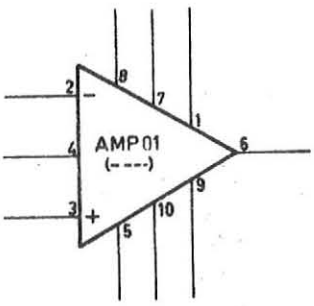
Description :

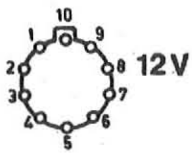
The ALU04 comprises a full adder for two 2-bit binary numbers (A0 through A1 and B0 through B1) plus a carry input CI.
Two outputs (Z0 and Z1) are provided for each bit and the carry output CO is obtained from the last bit.

Function table :

INPUT				OUTPUT					
				When CI=0			When CI=1		
A0	B0	A1	B1	Z0	Z1	C0	Z0	Z1	C0
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

Function name : AMP01
Code number : 9331 353 50112
Supplier type : TBA281
Drawing symbol :





Description :

The AMP01 comprises a monolithic integrated voltage regulator circuit consisting of a temperature compensated reference amplifier, error amplifier, power series feed transistor and a current limiter.
The AMP01 is used in power supplies.
The pins have the following functions:

1) Current sense
2) Inverting input
3) Non-inverting input
4) V-ref
5) Negative supply voltage
6) V-out*
7) V-collector
8) Positive supply voltage
9) Frequency compensation
10) Current limit.

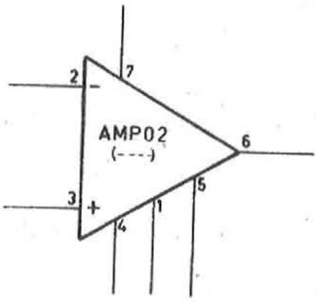
* without external transistor I load max. = 50 mA.

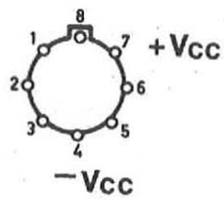
Function name : AMP02

Code number : 9331 370 00112

Supplier type : TBA221; 72741N

Drawing symbol :





Description :

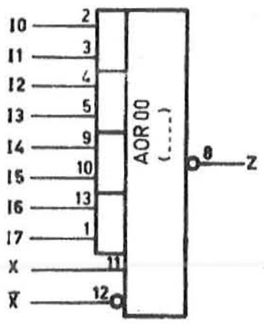
The TBA221 comprises a high gain d.c. differential amplifier, with a voltage gain of 100.000. The TBA221 does not require external frequency compensation components, has input null adjustment facilities and short circuit protection.

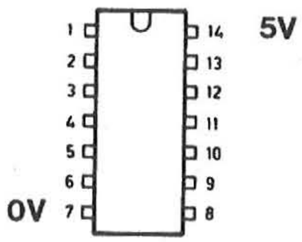
Function name : AOR00

Code number : 9330 502 71XX0

Supplier type : FJH181; 7454; 9N54

Drawing symbol :





Description :

The AOR00 comprises four two input AND-gates, which are followed by an OR-gate and an inverter. The inverter has a totem pole output stage. The AOR00 has a possibility for expanding via inputs X and $\overline{X}$

Logic function :

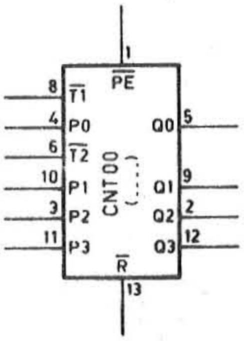
$$Z = \overline{I_o.I_1 + I_2.I_3 + I_4.I_5 + I_6.I_7 + X.\overline{X}}$$

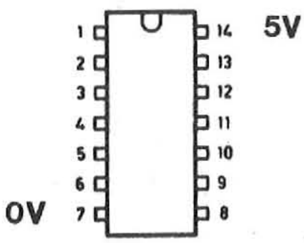
Function name : CNT00

Code number : 9330 887 00XX0

Supplier type : FJB93197; 74197; 93197

Drawing symbol :

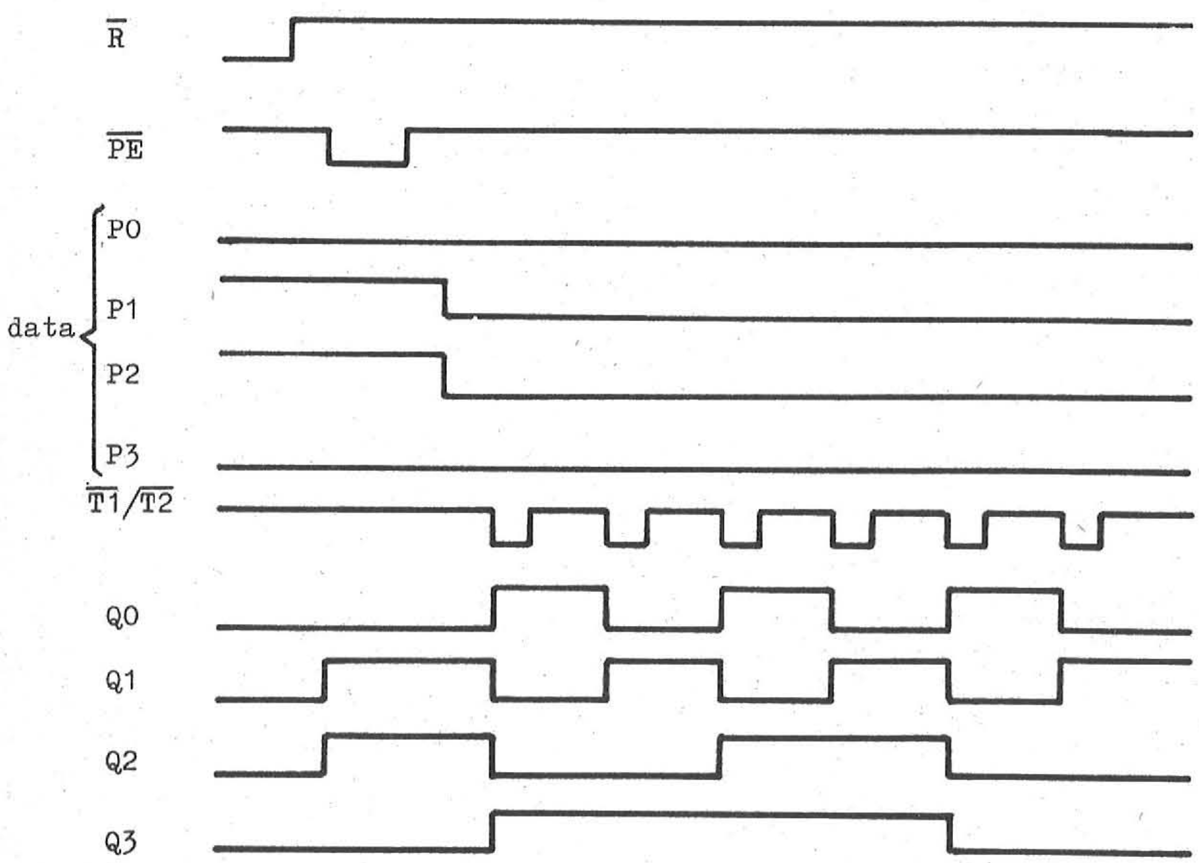




Description :

The presettable decade and binary counter CNT00 comprises a modulo 2 binary counter and a modulo 8 binary counter. By connecting output Q0 (pin 5) to trigger input $\overline{T2}$ (pin 6) the circuit can be used as a modulo 16 counter. The modulo 16 counter can be increased by one upon the negative-going edge of the trigger input $\overline{T1}$, provided that the inputs $\overline{PE}$ and $\overline{R}$ are '1'. The whole counter can be reset by making input $\overline{R}$ '0'.
The information at the inputs P0, P1, P2 and P3 is stored and placed on the outputs Q0, Q1, Q2 and Q3 as soon as the input $\overline{PE}$ becomes '0', provided that the input $\overline{R}$ is '1'.
The modulo 2 counter can be increased by one upon the negative-going edge of trigger input $\overline{T1}$, provided that the inputs $\overline{PE}$ and $\overline{R}$ are '1'.
The modulo 8 counter can be increased by one upon the negative-going edge of the trigger input $\overline{T2}$, provided that the inputs $\overline{PE}$ and $\overline{R}$ are '1'.

Timing diagram :



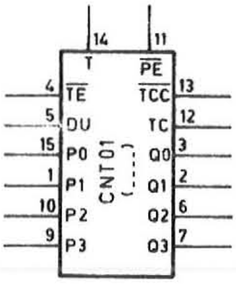
Note: Q0 is not connected to $\overline{T2}$

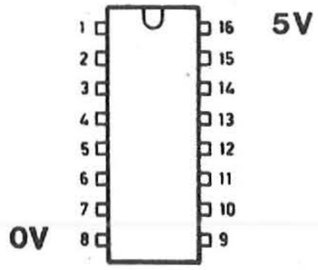
Function name : CNT01

Code number : 9331 623 70XX0

Supplier type : FJB93191; 74191; 93191

Drawing symbol :

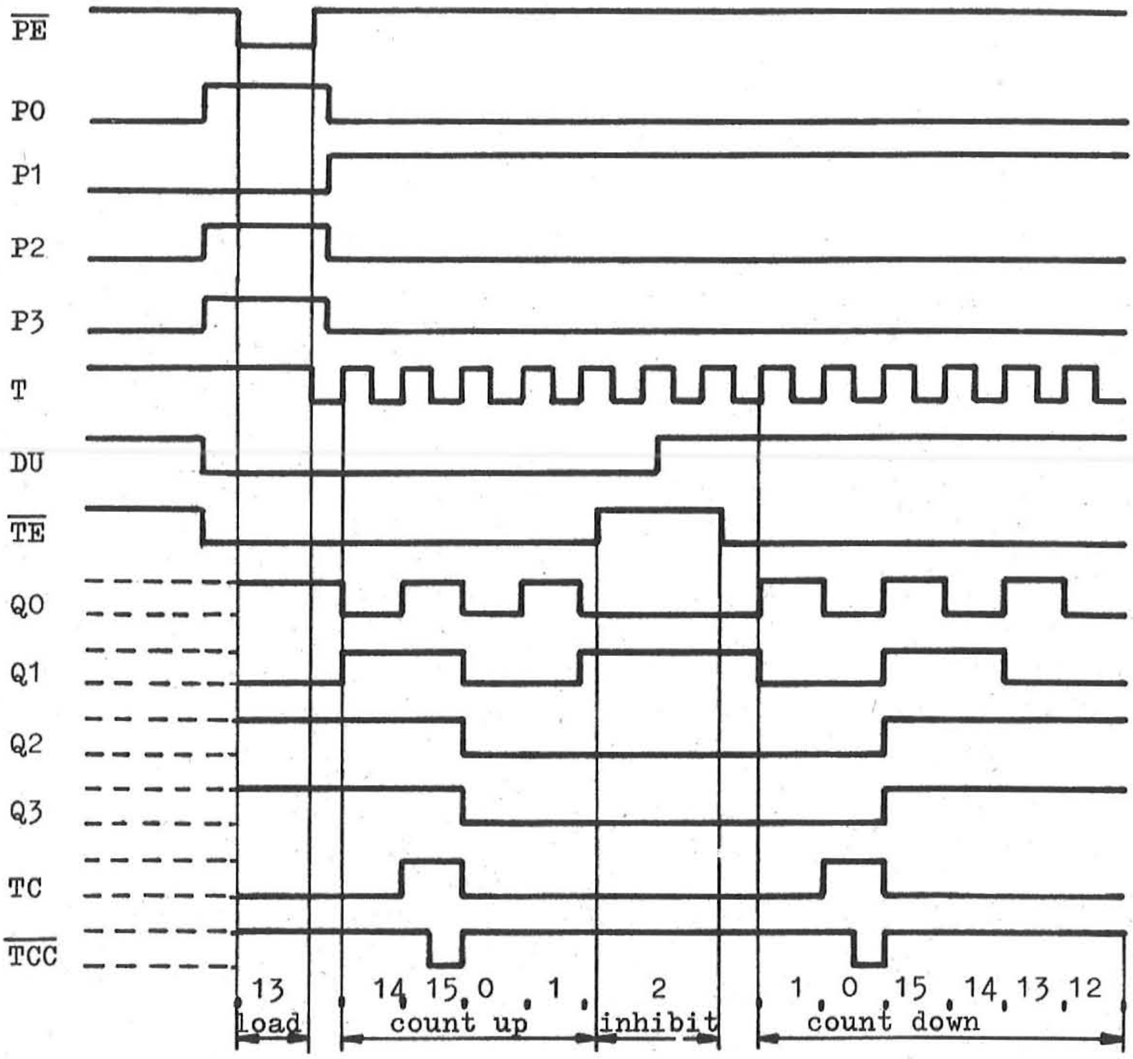




Description :

The CNT01 is a 4-bit binary up/down counter. The outputs Q0 thr. Q3 may be preset to any state by placing the desired data on the inputs P0 thr.P3 and an '0' on input $\overline{PE}$. The outputs Q0 thr. Q3 can be changed on the positive-going edge of the input T if the enable input $\overline{TE}$ is '0'. A '1' at input $\overline{TE}$ inhibits counting. Level changes at the enable input $\overline{TE}$ should be made only when input T is '1'. The direction of the count is determined by the state of the down/up input DU. When the input is '0', the counter counts up and when the input is '1', it counts down. The output TC is '1' when the count on the outputs Q0 thr. Q3 is 0 (counting down) or 15 (counting up). The logic function is $TC = \overline{Q0}.\overline{Q1}.\overline{Q2}.\overline{Q3}.\ DU + Q0.Q1.Q2.Q3.\ \overline{DU}$.
The output $\overline{TCC}$ is '0' when the count on the outputs Q0 thr. Q3 is 0 (counting down) or 15 (counting up) and only during the time that the inputs T and $\overline{TE}$ are '0'.
The counter can be reset by placing all zero's on the inputs P0 thr. P3 and an '0' on input $\overline{PE}$.

Timing diagram :

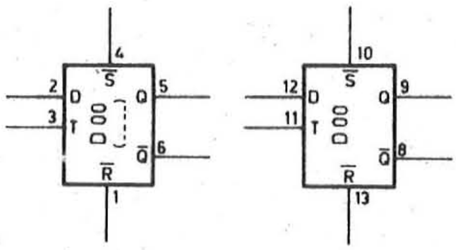


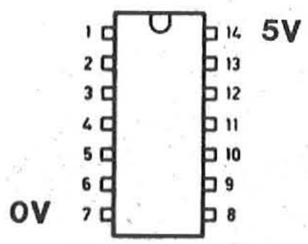
Function name : DOO

Code number : 9330 504 70XX0

Supplier type : FJJ131; 7474; 9N74

Drawing symbol :





Description :

The DOO comprises two, independent edge-triggered D-type flip-flops with direct SET and RESET inputs. On the positive-going edge of the trigger input T, the information on the D-input will be stored and placed on the outputs Q and $\overline{Q}$.

Function table :

D	T	Q	$\overline{Q}$
0	↑	0	1
1	↑	1	0

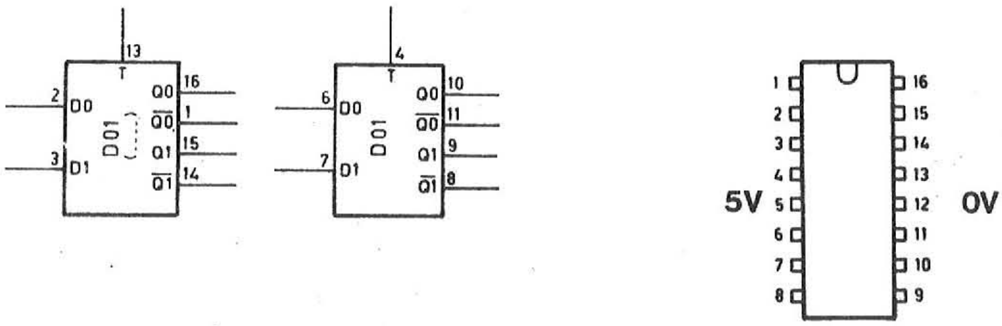
Note: both inputs $\overline{S}$ and $\overline{R}$ must be '1'

Function name : D01

Code number : 9330 648 10XXO

Supplier type : FJJ181; 7475; 9375

Drawing symbol :



Description :

The D01 comprises four D-type flip-flops. Each of the two flip-flops has a common trigger input. During the time the trigger input is high, changes on the data input will be transferred to the outputs. When the trigger input is low, the outputs are unaffected by the input.

Function table :

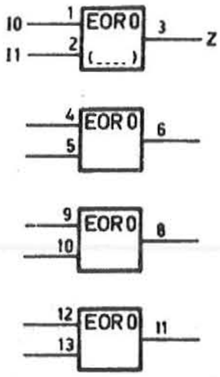
D	T	Q	$\overline{Q}$
0	1	0	1
1	1	1	0

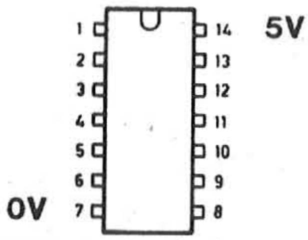
Function name : EOR00

Code number : 9331 329 60XX0

Supplier type : FJH271; 7486; 9N86

Drawing symbol :





Description :

The EOR00 comprises four,independent exclusive OR-gates, each provided with two inputs and a totem pole output stage.

Logic function :

$Z = I_o \cdot \overline{I_1} + \overline{I_o} \cdot I_1$

Function table :

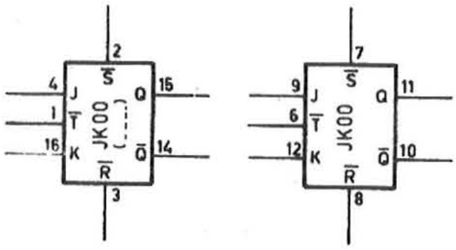
I_o	I_1	Z
0	0	0
0	1	1
1	0	1
1	1	0

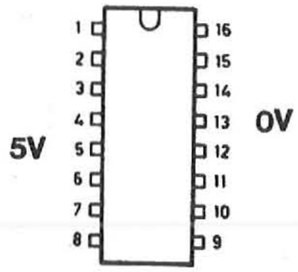
Function name : JK00

Code number :

Supplier type : 74H106; 9H106

Drawing symbol :





Description :

The JK00 comprises two, independent, negative-edge triggered JK flip-flops with direct SET and RESET inputs. If the J-input is '1' and the K-input '0', the flip-flop will be set on the negative-going edge of input $\overline{T}$. If the J-input is '0' and the K-input '1', the flip-flop will be reset. When both J and K inputs are '1', the outputs Q and $\overline{Q}$ will change on every negative-going edge of the trigger input $\overline{T}$ (the flip-flop is toggling). The flip-flop can be set or reset directly by placing a '0' on input $\overline{S}$ or $\overline{R}$ respectively. These inputs override all other inputs.

Function table :

J	K	$\overline{T}$	OLD Q	OLD $\overline{Q}$	NEW Q	NEW $\overline{Q}$
0	0	↓	0	1	0	1
			1	0	1	0
0	1	↓	0	1	0	1
			1	0	0	1
1	0	↓	0	1	1	0
			1	0	1	0
1	1	↓	0	1	1	0
			1	0	0	1

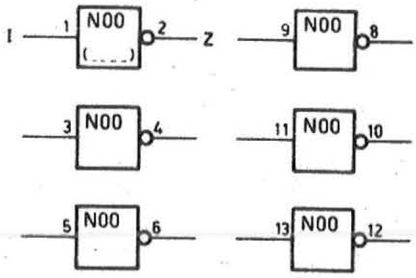
Note: the inputs $\overline{S}$ and $\overline{R}$ must be '1'

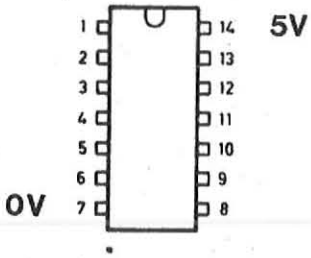
Function name : N00

Code number : 9331 094 31XX0

Supplier type : FJH241; 7404; 9N04

Drawing symbol :





Description :

The N00 comprises six,independent inverters with a totem pole output stage.

Function table :

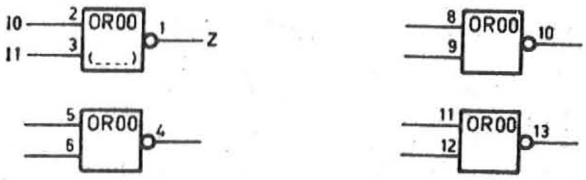
I	Z
0	1
1	0

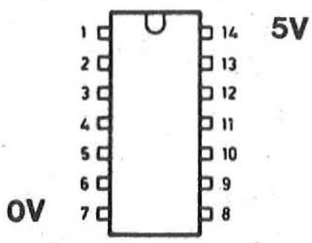
Function name : OR00

Code number : 9330 806 21XX0

Supplier type : FJH221; 7402; 9N02

Drawing symbol :





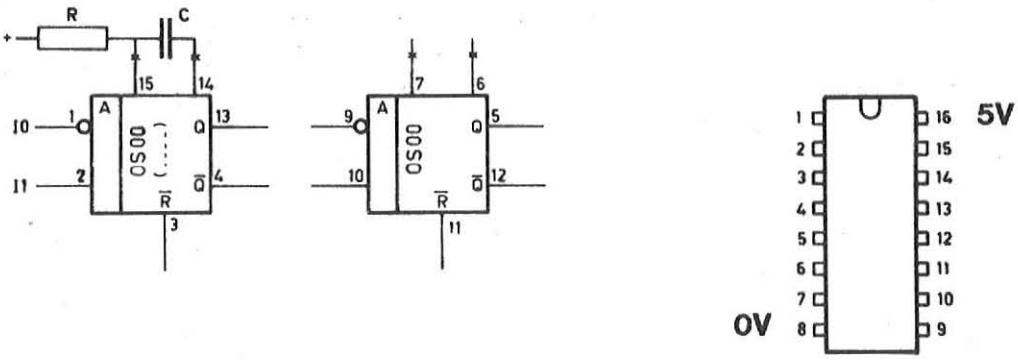
Description :

The OR00 comprises four independent NOR-gates, each provided with two inputs and a totem pole output stage.

Logic function :

$Z = \overline{I_0 + I_1}$

Function name	:	OS00
Code number	:	9331 667 30XX0
Supplier type	:	74123
Drawing symbol	:	



Description :

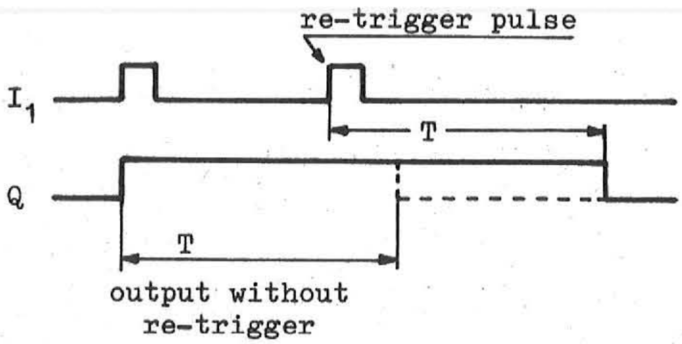
The OS00 comprises two re-triggerable, monostable multivibrators. By triggering the one-shot before the output pulse is terminated, the output pulse will be extended. The input $\overline{R}$ permits any output pulse to be terminated at a time independent of the timing components R and C.
Input I_0 is a negative-edge triggered input and will trigger the one-shot when it becomes '0', as long as input I_1 is '1'. Input I_1 is a positive-edge triggered input and will trigger the one-shot when it becomes '1', as long as input I_0 is '0'. The duration T (see timing diagram) of the output Q and $\overline{Q}$ depends on the RC network which is connected externally to the integrated circuit.
When input $\overline{R}$ becomes '0' it will terminate the output pulses.

Function table :

Inputs		Outputs	
I_0	I_1	Q	$\overline{Q}$
1	*	0	1
*	0	0	1
0	↑	⊓	⊔
↓	1	⊓	⊔

* =don't care

Timing diagram :



Note:
(i) input I_0 must be '0'.
(ii) outputs are similarly affected when triggered by input I_0 ('1' to '0') with I_1 held at a '1'.