14 MEMORY MODULES

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14.1 MEMORY MODULES IDENTIFICATIONS

Type Number	Description	6810/12	6813/14	Mounting Code	Power requirements
				6881/6824	
PTS6822 P843-108	Memory module 8k 16-bit words of read/write core, cycle time 1.2 u sec.	X	X	1 slot	+ 5V.2.6A
PTS6823 P843-116	Memory module 16k 16-bit words of read/write core, cycle time 1.2 usec.	X	X		
P843-216	Memory module 16k words of read/write core, cycle time 0.7 usec.	X	X		
PTS6825 P843-232	Memory module 32k words of read/write core, cycle time 0.7 u sec.		X		
PTS 6781 P843-528	Random access memory 128kW 21 bits			X 1 slot	

Testprograms: core memory 0-32K - ⟩ MEMTSC
core memory above 32K - ⟩

Power consumption for different core sizes in Ampères

Module size	+5V	-5V	16V
8K (1.2 µsec.) O.	2.5A	0.12A	3.6A
N.O.	2.4A	0.12A	0.4A
16K (1.2 µsec.) O.	2.8A	0.18A	4.6A
N.O.	2.6A	0.18A	0.5A
16K (0.7 µsec.) O.	3.2A	0.18A	5.7A
N.O.	2.7A	0.18A	0.7A
32K (0.7 µsec.) O.	4.5A	0.3A	4.7A
N.O.	4.0A	0.3A	0.7A

To derive power consumption at system-level, one module is assumed operating (O).
The other modules are considered not-operating (N.O.)

Example: 2 x 16K (1,2 µsec) modules: +5V, 5.4A, -5V, 0.36A, 16V, 5.1A.

14.2 INSTALLATION DETAILS

Total capacity	Module(s) used	Addressing
8K.....	...One 8K-module.....	.....0-8K
16K.....	...One 16K-module....	.....0-16K
16K.....	...One 8K-module.....	.....0-8K
	One 8K-module.....	.....8-16K
24K.....	...One 16K-module....	.....0-16K
	One 8K-module.....	.....16-24K
32K.....	...One 16K-module....	.....0-16K
	One 16K-module ...	....16-32K

Before locating a memory module in the computer rack its address field must be strapped to enable correct addressing of the module. The Figures 2-22, 2-23, 2-24 and 2-25 show the existing versions of CMM straps.

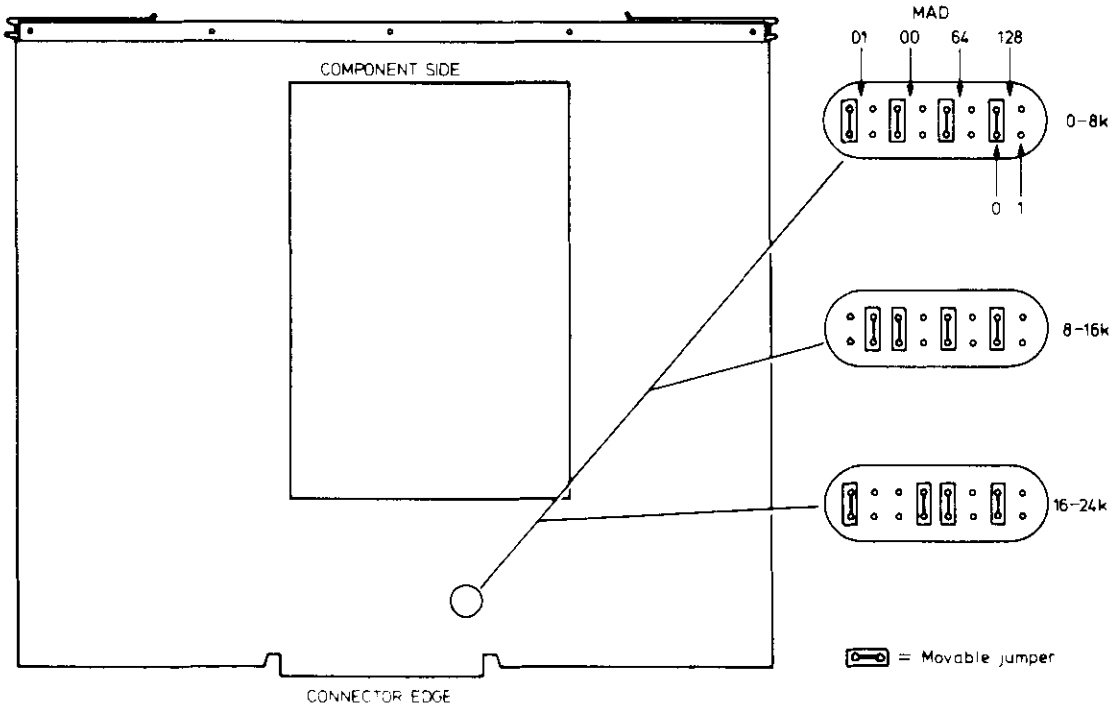


Figure 14.1 JUMPERS ON THE ELCOMA 8K CMM

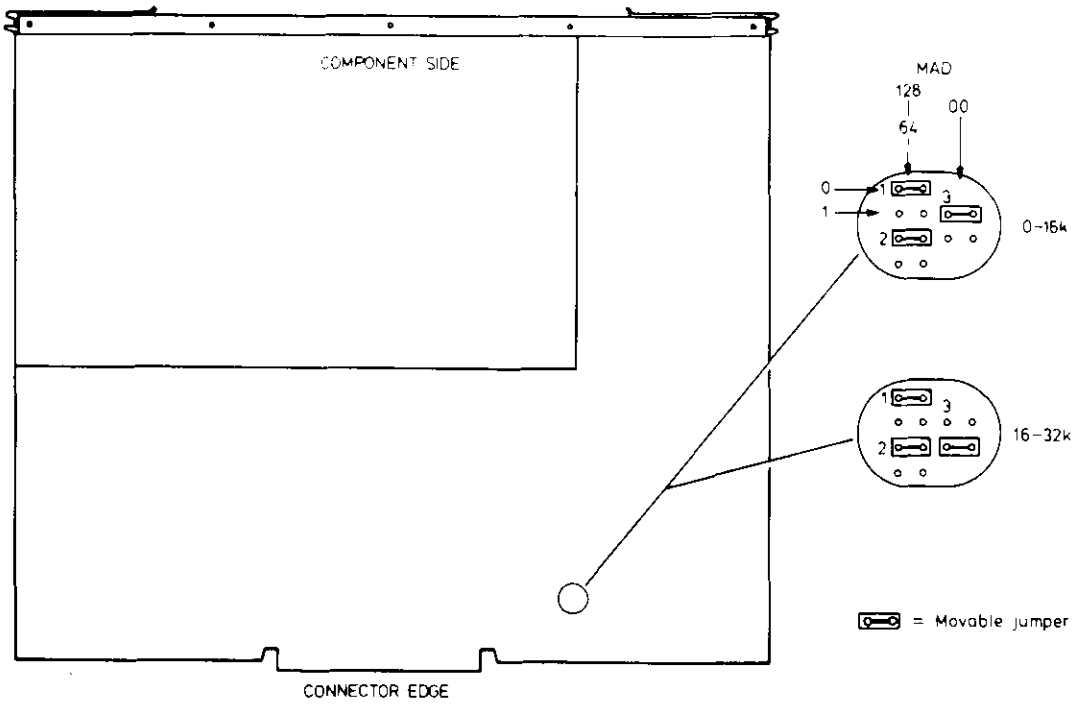


Figure 14.2 JUMPERS ON THE ELCOMA 16K CMM (EARLY VERSION)

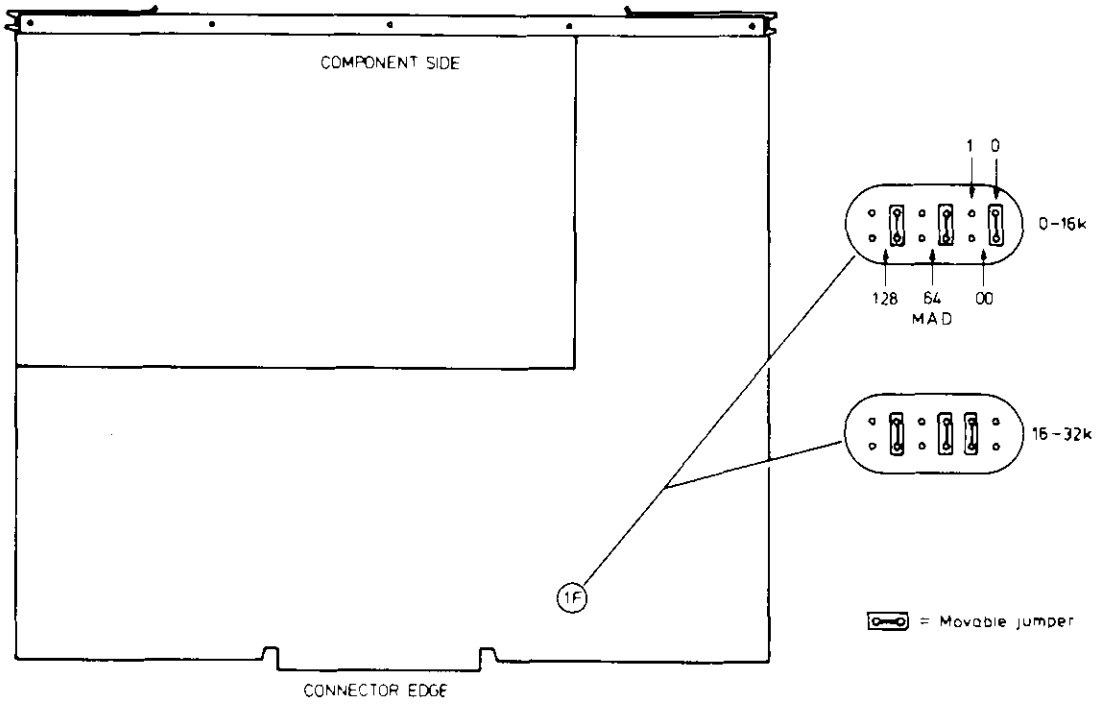


Figure 14.3 JUMPERS ON THE ELCOMA 16K CMM (LATER VERSION)

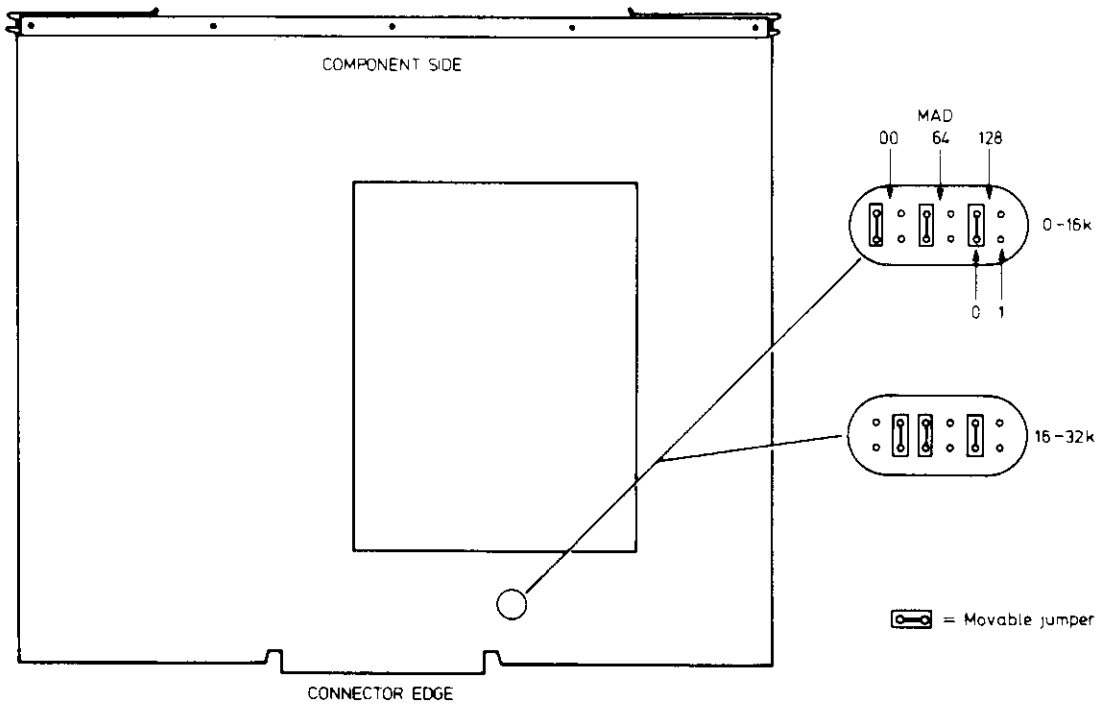
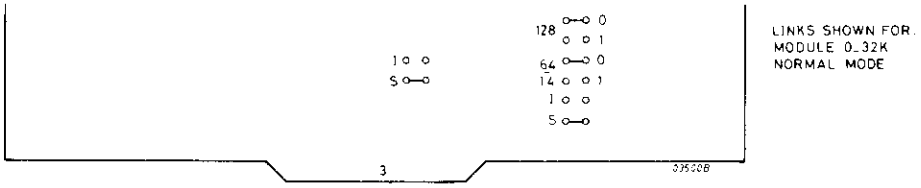


Figure 14.4 JUMPERS ON THE ELCOMA 16K CMM (EARLY VERSION)

The memory module or modules which comprises a complete memory are located as standard in slots 2 and 3 in the computer rack. Where both slots 2 and 3 are used for memory it is common practice to locate the first memory module (from address zero) in slot 2. However, as no physical differences exist between the slots, no fast ruling is necessary for the positioning of the two modules in specific slots.

STRAP ON S/N	AD 00/14	MAD 64	MAD 128	STRAP ON I
0 -16K	0	0	0	0 -32K even (bit 14)
16 -32K	1	0	0	0 -32K odd
32 -48K	0	1	0	32-64K even
48 -64K	1	1	0	32-64K odd
64 -80K	0	0	1	64-96K even
80 -96K	1	0	1	64-96K odd
96 -112K	0	1	1	96-128K even
112-128K	1	1	1	96-128K odd

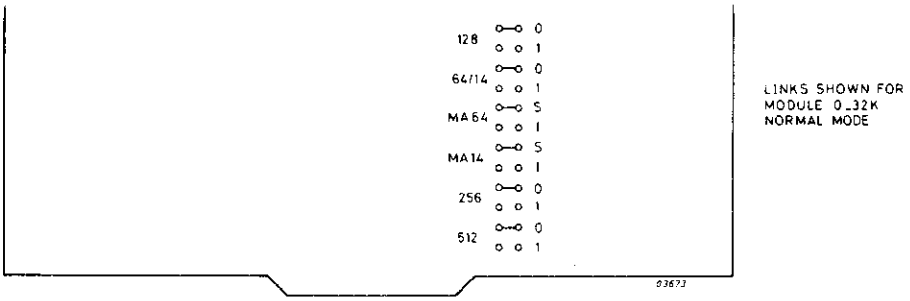
S = Standard addressing
I = Interleaving mode odd addressing



STRAPS ON S STANDARD	MAD 64/14	MAD 128	STRAPS ON I INTERLEAVING
0 -32K	0	0	0 - 64K even
32-64K	1	0	0 - 64K odd
64-96K	0	1	64-128K even
96-128K	1	1	64-128K odd

Figure 14.5a: 32K AMPEX

PTS6825 MEMORY MODULE



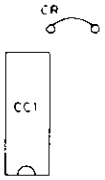
STRAPS ON S STANDARD	MAD 64/14	MAD 128	MAD 256	MAD 512	STRAPS ON I INTERLEAVING
0-32K	0	0	0	0	0-64K even
32-64K	1	0	0	0	0-64K odd
64-96K	0	1	0	0	64-128K even
96-128K	1	1	0	0	64-128K odd
128-160K	0	0	1	0	128-192K even
160-192K	1	0	1	0	128-192K odd
192-224K	0	1	1	0	192-256K even
224-256K	1	1	1	0	192-256K odd

448-480K	0	1	1	1	448-512K even
480-512K	1	1	1	1	448-512K odd

Figure 14.5b: 32 K FABRIEK MEMORY MODULE

STRAPSETTING M128E/32/64 MODULES

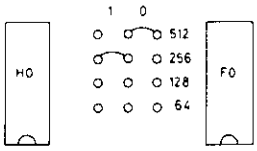
STRAP 1
(Clear Register)



: Normally fitted for applications in which the CLEARN bus line is used.

STRAPS 2 and 3
(Memory Module No.)

STRAPS 4 and 5
(Memory Module Size)

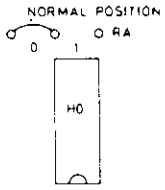


: EXAMPLE ONLY

Memory Module No. 1
Memory Size 128K

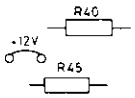
Note: For 64K variant fit strap '128'
For 32K variant fit strap '64'.

STRAP 6



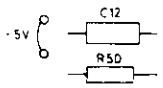
: Normally fitted to interconnect MI-1 and N04. Can be refitted to interconnect MI-1 and H0-10 so that a test program resides in memory block 16-32K. This allows memory block 0-16K to be tested.

STRAP 7



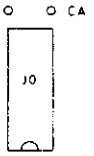
: Normally fitted. Open during initial production-test to protect memory stack.

STRAP 8



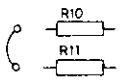
: Normally fitted. Open during initial production-test to protect memory stack.

STRAP 9



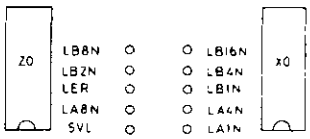
: Not normally fitted: When fitted cancels the first 32K of stack addresses of Memory Module 0, only to accomodate another type of memory e.g. a 32K core memory.

STRAP 10



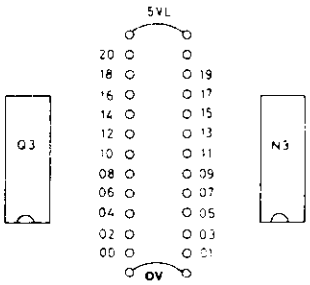
: Normally fitted, open during production test.

TEST CONNECTOR 1

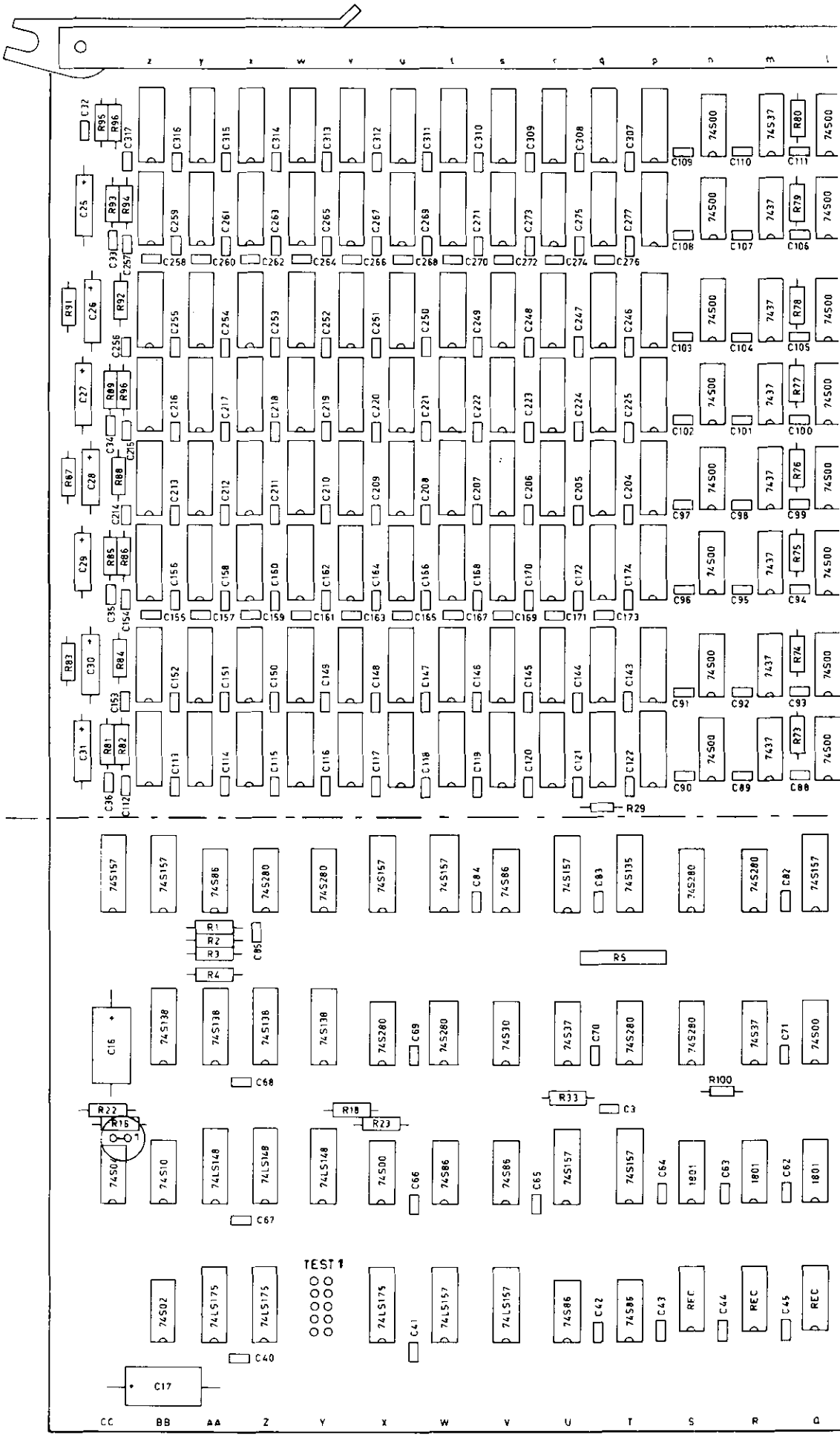


: During production-test it drives an LED display. Sometimes it is used to drive an application display.

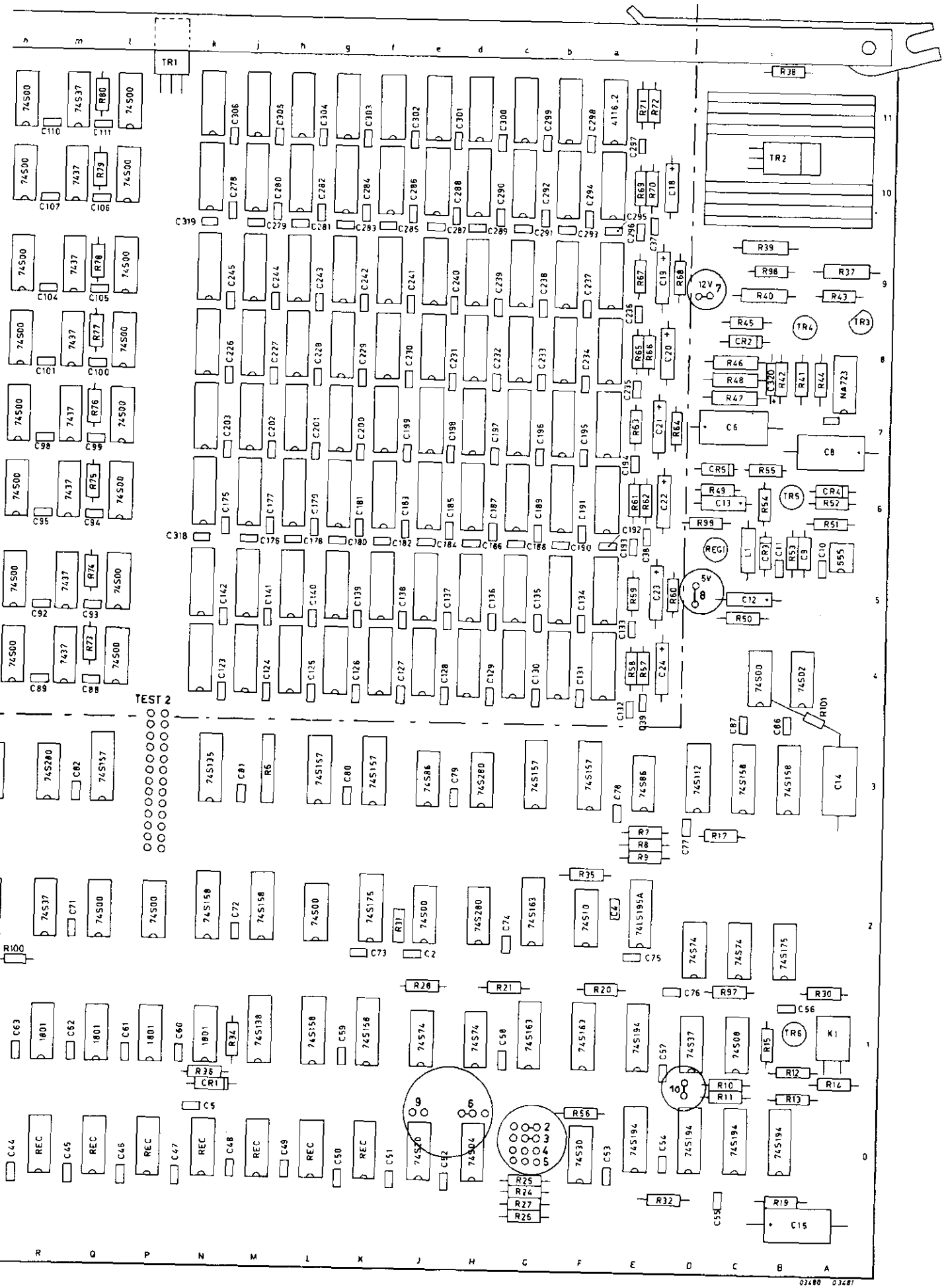
TEST CONNECTOR 2



: During production-test it is connected to a test box which simulates single-bit errors. Not normally used in the field.



LAYOUT


TR1
TR2
TR3
TR4
TR5
TR6
K1
TEST 2
12V
5V
REG1
555
NA723
03480 03481

14.5 SHORT DESCRIPTION TESTPROGRAM

TESTABLE CONFIGURATIONS

The test program MEMTSC Release 2 can be used for testing core - and semiconductor memories of 32-256 Kbytes in the terminal computers 6805 and 6810-6813. Basic testing requires no extra equipment, a cassette or a diskette drive and the SOP provide the necessary man-to-machine interfaces.

WATCHED & TESTED FUNCTIONS

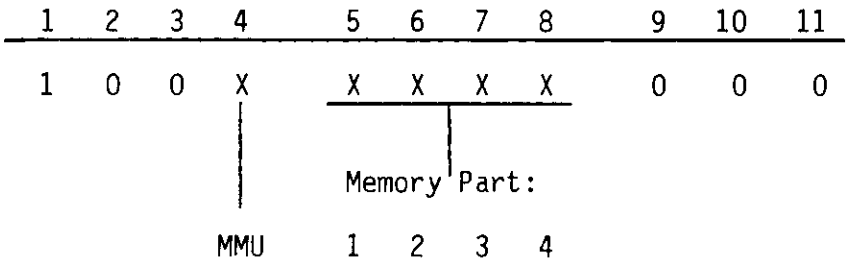
The program basically:

- Watches the power on/off handling in PSU and CPU (note: for test of this function; use instead the test program CPUTSC Release 2).
- Watches the occurence of invalid instruction codes.
- Watches the occurence of unwanted interrupts (all interrupts that are not expected by the program).
- Tests the memory function. Program move enables a test of the complete memory.

BAISC TEST - 'GO/NO GO'

PROGRAM LOAD & INITIATION

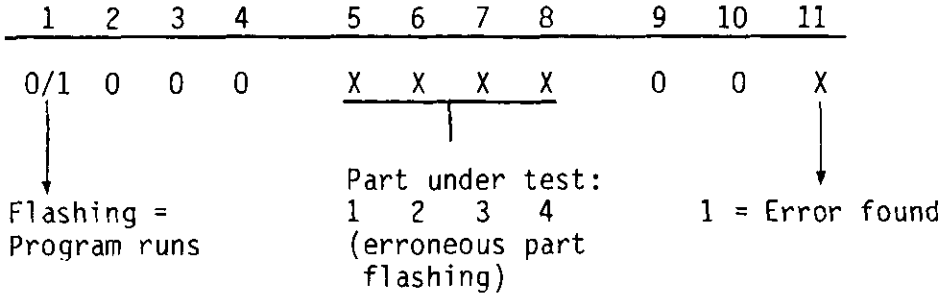
When the program has been loaded from a cassette or a diskette drive, it will automatically start a short sequence for initiating timers and identifying the memory system. Then it stops and lights the following SOP indicator (marked with 1):



Note: Lit X-indicator = fitted unit. When MMU is fitted; each memory part represents 64 Kbytes in a physical memory module of its own. If no MMU is fitted; each part represents 16 Kbytes without any fixed relation to physical memory modules (a module may contain 16, 32 or 64 Kbytes).

PROGRAM RUN & ERROR INDICATIONS

Select NO STOP on error by operating SOP switch 3 (the indicator will be lit), and start the program by operating SOP switch 1. The program will now run through a single-shot test cycle, provide that no stop is caused by another operation of SOP switch 1, or a watched function (power failure, invalid instruction or unwanted interrupt). If no errors are found, a complete test cycle takes about 35 seconds/64 Kbytes. During run time the SOP indicators will display:



Should SOP switch 1 be operated during run time, or if no errors have been found at the end of the test, the program returns to the initial state described in section 2.1.

Should the program stop on a watched function, or find one or more memory errors, it will switch to an error display state. The three rightmost SOP indicators will then display the main function that has failed.

9	10	11	
0	0	1	= Power On/Off Error
0	1	1	= Invalid Instruction Code
1	0	1	= Unwanted Interrupt
1	1	1	= Memory Error

Further error investigations are described in detailed description

Program MEM

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	818E	Write	LDR	A9,A11
0088	85A7	Load	STR	A13,A9
008A	91A0		ADKL	A9,2
008C	0002			
008E	E992		CWR	A9,A12
0090	5C0A		RB(4)	Load
0092	5700		RF	* +2
0094	818E		LDR	A9,A11
0096	80A6	RDC	LDR*	A8,A9
0098	E896		CWR	A8,A13
009A	5002		RF(0)	Suit3
009C	207F		HLT	Fault
009E	91A0	Suit3	ADKL	A9,2
00A0	0002			
00A2	E992		CWR	A9,A12
00A4	5C10		RB(4)	RDC
00A6	5F22		RB	Write

Start the program:
- Load the starting address in register A11
- Load the ending address in register A12
- Load the test-pattern in register A13
- Load the start-address of the program (/0086) into register A0
- Push the RUN button

After Start:
If no fault the program runs in loop

Fault: program stops at /009E

- A9 contains address of erronous memory location
- A8 ,, read pattern
- A13 ,, expected pattern

DUMP FACILITY

This program enables an area of memory to be printed out on either the ASR or PTS3100, or to be Displayed. It can be loaded either with the IPL routine or by hand using the control panel switches. Once loaded the following routine should be used:

- Load the starting address to be printed into register A7. *)
- Load the ending address of the area into register A8.
- Load the starting address of the program into register A0.
- Push the RUN button.

The program will stop when the last memory address has been either printed or displayed.

*) Bit 15 must be zero.

Program DUMP

Memory Address	Data	Program Instructions		
0080	FFFF		DATA	-/FFFF
0082	0000		DATA	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	47D0		CIO	A7,1,/10
008A	813C	WORD	LDR *	A1,A7
008C	0204		LDK	A2,4
008E	060F	CONT	LDK	A6,/F
0090	A604		ANR	A6,A1
0092	E558		LC	A5, TABLE, A6
0094	00BE			
0096	E549		SC	A5,BUFF + 1.A2
0098	00CF			
009A	39E4		SRC	A1,4

Memory Address	Data	Program Instructions		
009C	1A01		SUK	A2,1
009E	5C12		RB(NZ)	CONT
00A0	E348	OUT1	LC	A3,BUFF,A2
00A2	00CE			
00A4	4310		OTR	A3,0,/10
00A6	5C04		RB(NA)	* -2
00A8	1201		ADK	A2,1
00AA	EA20		CWK	A2,6
00AC	0006			
00AE	5C10		RB(NE)	OUT1
0080	1702		ADK	A7,2
00B2	EF02		CWR	A7,A8
00B4	5D2C		RB(NG)	WORD
00B6	4790		CIO	A7,0,/10
00B8	4FD0		SST	A7,/10
00BA	5C04		RB(NA)	* -2
00BC	5F3A		RB	START
00BE	3031	TABLE	DATA	'0123456789'
00C0	3233			
00C2	3435			
00C4	3637			
00C6	3839			
00C8	4142		DATA	'ABCDEF'
00CA	4344			
00CC	4546			
00CE	0D0A	BUFF	DATA	/0D0A

Notes: