13 CPU P6814/P6824 (CP7RA)

LIST OF ILLUSTRATIONS

LIST OF TABLES

13.1 PTS6814/24 CPU IDENTIFICATIONS

Type number : CPU board CP7R (CP7RA) with integrated serial CU (V24).

Test Programs : CPU - TP57RE Mem TSC rel.4 see chapter 14
MIOP
Integrated CU
PER3100 - PERTST

Devices
PER3100 - PTS 6862-003

Power Consumption :

- +5VL 9A
- +12VL 50mA
- -12VL 50mA

Note: 12NC code on the sticker on the board.

CP7R : 5111 199 6758X
CP7RA : 5111 199 6201X (5322 216 21084)
CP7RA : 5131 194 44400 (PTS)

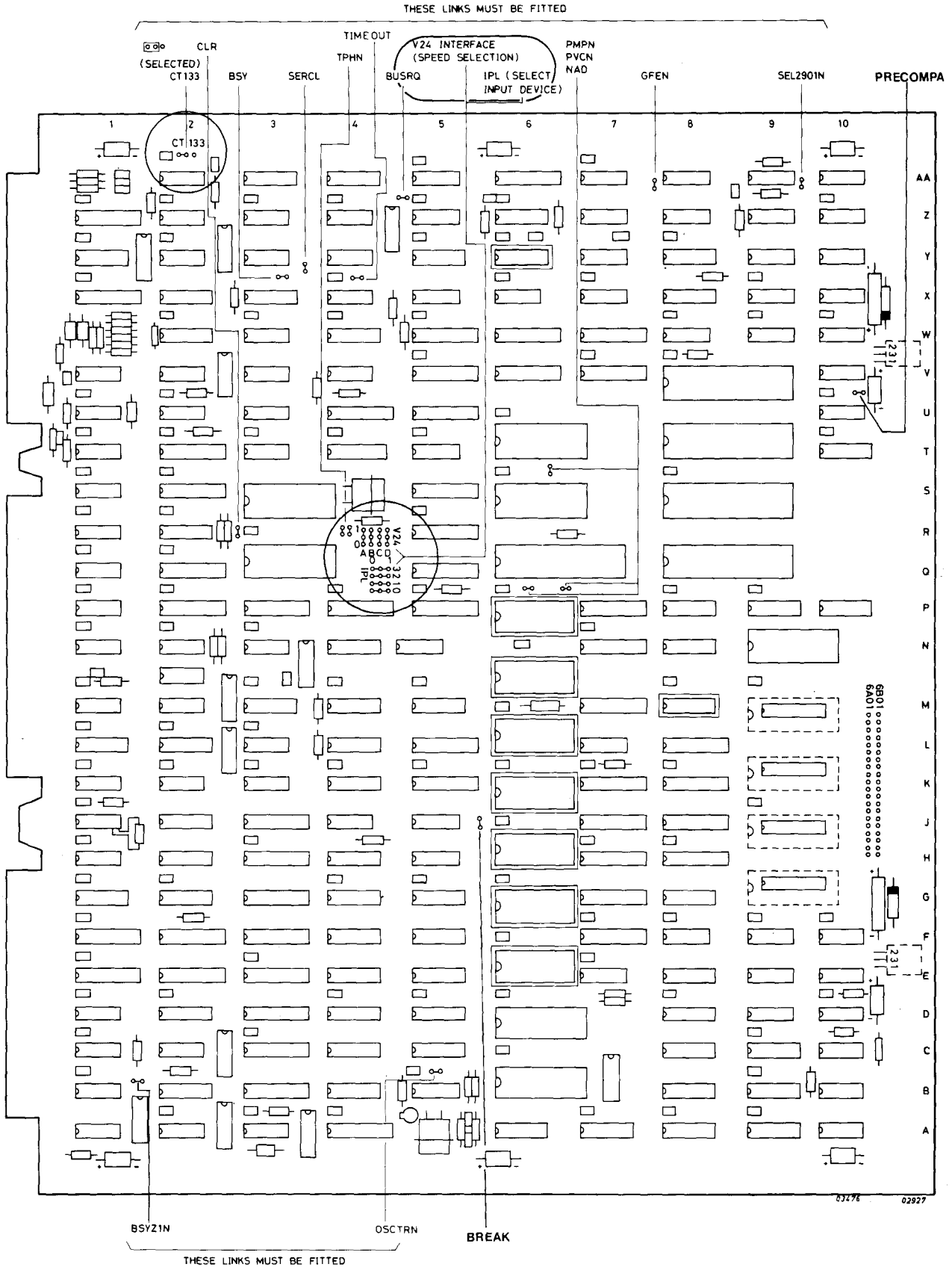
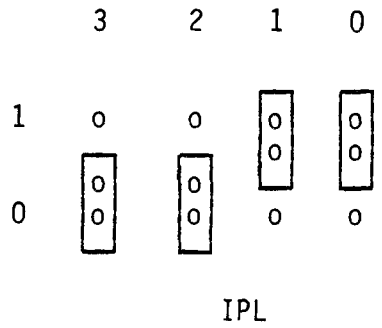


Figure 13.1 (CP7RA) LINK POSITIONS

3	2	1	0	WORD	IPL WORD	MEMORY ADDRESS HEX
OPS3N	OPS2N	OPS1N	OPSON			
0	0	0	0	0	255	1FE
0	0	0	1	1	254	1FC
0	0	1	0	2	253	1FA
0	0	1	1	3	252	1F8
0	1	0	0	4	251	1F6
0	1	0	1	5	250	1F4
0	1	1	0	6	249	1F2
0	1	1	1	7	248	1F0
1	0	0	0	8	247	1EE
1	0	0	1	9	246	1EC
1	0	1	0	10	245	1EA
1	0	1	1	11	244	1E8
1	1	0	0	12	243	1E6
1	1	0	1	13	242	1E4
1	1	1	0	14	241	1E2
1	1	1	1	15	240	1E0

Table 13.1 SELECT IPL INPUT DEVICE

The following diagram shows the identification that is silkscreened on the card and an example of word selection:



IPL

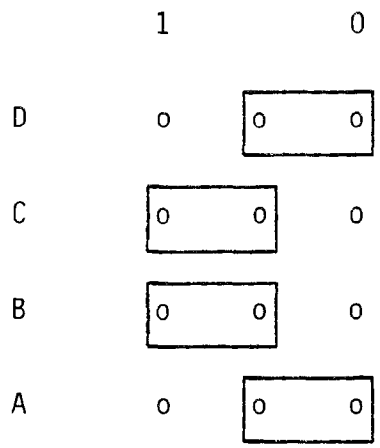
Example: word 3, memory address 1F8. The content of this word is loaded in register A15 during IPL.

In P6814/24 These Straps are set to '0'

Transmit/Receive U Link Positions				Baud Rate
D	C	B	A	
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1,200
1	0	0	0	1,800
1	0	0	1	2,000
1	0	1	0	2,400
1	0	1	1	3,600
1	1	0	0	4,800
1	1	0	1	7,200
1	1	1	0	9,600
1	1	1	1	19,200

Table 13.2 V24 INTERFACE SPEED SELECTION

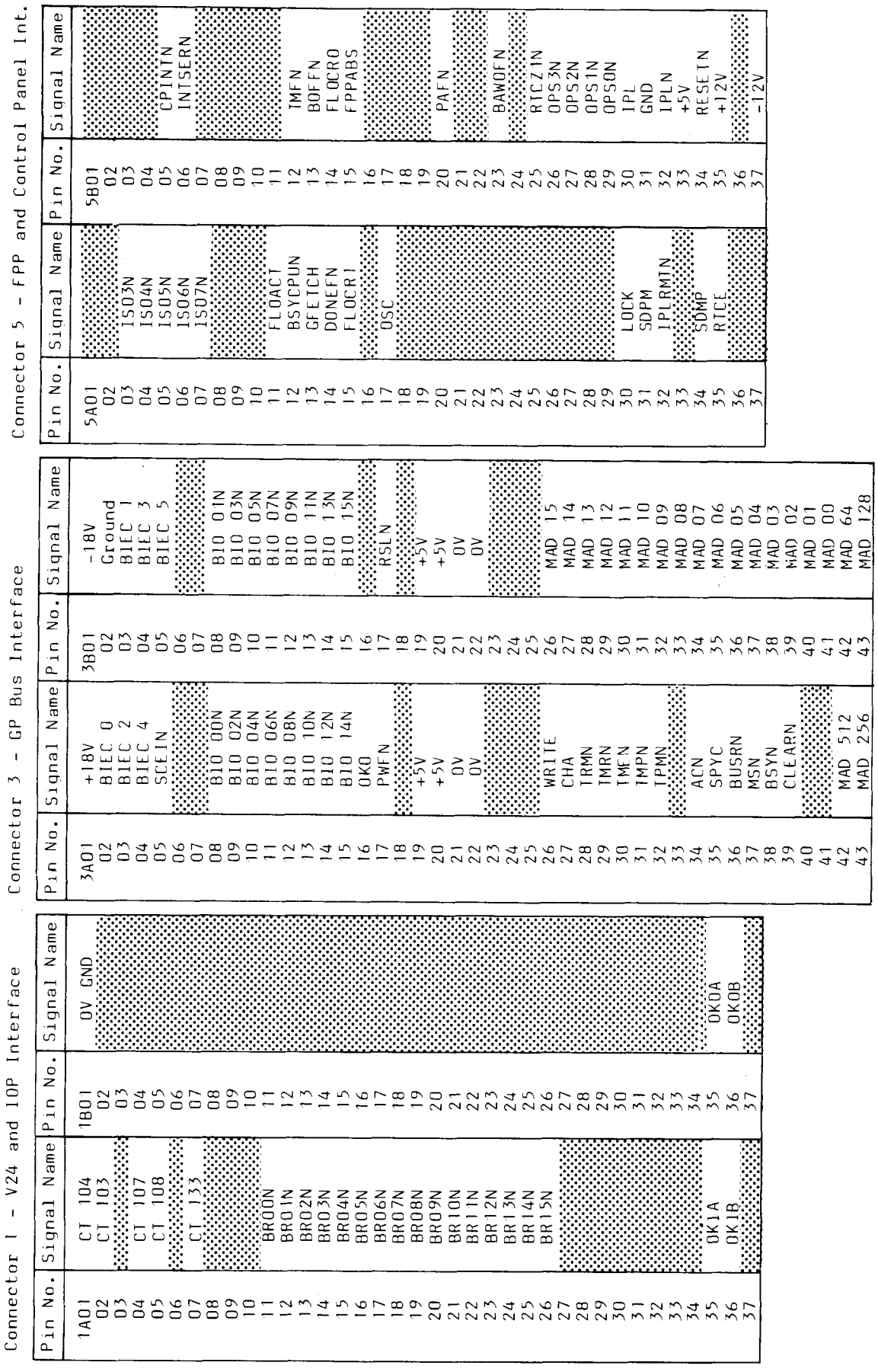
The following diagram shows the identification that is silkscreened on the card, and an example of speed selection:



Selected speed is 600 bauds (PER 3100)

Note: The maximum speed authorised for the PER 3100 is 600 bauds.

13.3 INTERFACE CONNECTIONS see also chapter 6



Connector 1 - V24 and IOP Interface

Pin No.	Signal Name	Pin No.	Signal Name
1A01	CT 104	1B01	0V GND
02	CT 103	02	
03		03	
04	CT 107	04	
05	CT 108	05	
06		06	
07	CT 133	07	
08		08	
09		09	
10		10	
11	BR00N	11	
12	BR01N	12	
13	BR02N	13	
14	BR03N	14	
15	BR04N	15	
16	BR05N	16	
17	BR06N	17	
18	BR07N	18	
19	BR08N	19	
20	BR09N	20	
21	BR10N	21	
22	BR11N	22	
23	BR12N	23	
24	BR13N	24	
25	BR14N	25	
26	BR15N	26	
27		27	
28		28	
29		29	
30		30	
31		31	
32		32	
33		33	
34		34	
35	OK1A	35	OK0A
36	OK1B	36	OK0B
37		37	

Connector 3 - GP Bus Interface

Pin No.	Signal Name	Pin No.	Signal Name
3A01	+18V	3B01	-18V
02	BIEC 0	02	Ground
03	BIEC 2	03	BIEC 1
04	BIEC 4	04	BIEC 3
05	SCEIN	05	BIEC 5
06		06	
07		07	
08	BIO 00N	08	BIO 01N
09	BIO 02N	09	BIO 03N
10	BIO 04N	10	BIO 05N
11	BIO 06N	11	BIO 07N
12	BIO 08N	12	BIO 09N
13	BIO 10N	13	BIO 11N
14	BIO 12N	14	BIO 13N
15	BIO 14N	15	BIO 15N
16	OKO	16	RSLN
17	PWFN	17	
18		18	
19	+5V	19	+5V
20	+5V	20	+5V
21	0V	21	0V
22	0V	22	0V
23		23	
24		24	
25		25	
26	WRITE	26	MAD 15
27	CHA	27	MAD 14
28	TRMN	28	MAD 13
29	TMRN	29	MAD 12
30	TMFN	30	MAD 11
31	TMPN	31	MAD 10
32	TPMN	32	MAD 09
33		33	MAD 08
34	ACN	34	MAD 07
35	SPYC	35	MAD 06
36	BUSRN	36	MAD 05
37	MSN	37	MAD 04
38	BSYN	38	MAD 03
39	CLEARN	39	MAD 02
40		40	MAD 01
41		41	MAD 00
42	MAD 512	42	MAD 64
43	MAD 256	43	MAD 128

Connector 5 - FPP and Control Panel Int.

Pin No.	Signal Name	Pin No.	Signal Name
5A01		5B01	
02		02	
03	ISO3N	03	
04	ISO4N	04	
05	ISO5N	05	CPINTN
06	ISO6N	06	INTSERN
07	ISO7N	07	
08		08	
09		09	
10	FLOACT	10	
11		11	IMFN
12	BSYCPUN	12	
13	GFETCH	13	BOFFN
14	DONEFN	14	FLOCRO
15	FLOCRI	15	FPPABS
16		16	
17	OSC	17	
18		18	
19		19	
20		20	PAFN
21		21	
22		22	
23		23	BAWOFN
24		24	
25		25	RICZIN
26		26	OPS3N
27		27	OPS2N
28		28	OPS1N
29		29	OPS0N
30	LOCK	30	IPL
31	SDPM	31	GND
32	IPLRMIN	32	IPLN
33		33	+5V
34	SDMP	34	RESETN
35	RTCE	35	+12V
36		36	
37		37	-12V

Figure 13.2 CP7RA CONNECTORS (REAR VIEW)

Signal Name	Source (Pin No)	Destination (Pin No)	Description
ACN	GPB C.U.s	CP7R/G (3A34)	Active low to indicate to the CPU that the C.U. accepts the request to carry out a designated function.
BROON-15N	IOP CUs	CP7R/E (1A11-26)	Break Request Lines active low, BR00 has the highest priority.
BAWOFN	Power Supply	CP7R/J (5B23)	When semi-conductor memories are employed, this signal (Battery Was Off) indicates that data has been lost.
BIEC 0-5	GPB C.U.s	CP7R/E (3A02-04 3B03-05)	Binary Coded Interrupts
BIO 00-15N	CP7R/D (3A08-15, 3B08-15)		Bidirectional data lines between CP7RA and all GPB Master and Slave Units.
BSYN	GPB Masters	CP7R/K (3A38)	A bidirectional line between all GPB Masters; when a Master has been selected this line is low to indicate Busy to other Masters.
BUSRN	GPB Masters	CP7R/K (3A36)	A bidirectional line between all GPB Masters; any Master may force this line low to request the Bus.
BOFFN	CP7R/G (5B13)	FPP	Active low to inhibit BIO and enable FPP to set BIO instead.
BSYCPUN	CP7R/K (5A12)	FPP	Active low indicates that the CPU is Busy with the Bus.
CHA	CP7R/I (3A27)	GP Bus	When received by the Memory CHA = 1 for Character Operation and CHA = 0 for Word Operation. For Control Units and External Registers CHA = 0.
CLEARN	CP7R/D (3A39)	GPB Masters and Slaves	General reset of all devices, active low for a minimum time of 90´S.
CPINTN	CP7R/E (5B05)	CP7R	Control Panel Interrupt, to be linked at the Back Panel to the Interrupt (IS) Lines.
CT103	CP7R/D (1A02)	D.T.E.	Serial data
CT104	D.T.E.	CP7R/D (1A01)	Serial data
CT107	D.T.E.	CP7R/D (1A04)	Modem ready
CT108	CP7R/D (1A05)	D.T.E	Connect Modem to Line

Table 13.2a INTERFACE SIGNALS (CONNECTORS 1,3,5)

Signal Name	Source (Pin No)	Destination (Pin No)	Description
CT133	D.T.E	CP7R/D (1A07)	Ready for Receiving
DONEFN	FPP	CP7R/A (5A14)	Indicates to the CPU that the FPP has finished the transfer.
FLOCRO-1	FPP	CP7R/G (5B14,5A15)	From the FPP Condition Register to the CPU Condition Register.
FLOACT	CP7R/G (5A11)	FPP	Sent at the beginning of an FPP instruc tion to time the actual processing and to synchronise the end of the operation.
FPPABS	FPP	CP7R/J (5B15)	When the FPP Card is inserted this signal is forced low.
GFETCH	CP7R/C (5A13)	CP7R/N	Indicates an Instruction Fetch cycle and restarts the CPU sequensor in some cases.
IPLRMTN	Remote Terminal	CP7R/J) (5A32))	These 3 signals are all associated with the same function, i.e. to indicate,to
IPL		CP7R/J)- (5B30))	the CPU External Test Logic that a code is to be received on Lines OPS OON-03N
IPLN		CP7R/J) (5B32))	
ISO3N-07N	CUs	CP7R/E (5A03-07)	Interrupt Request Lines
INTSERN	CP7R/D (5B06)	CP7R/	An Interrupt from the Operator Interface (Serial Interface) when either a Write, Read, Wait or Echo condition is active. This signal is linked on the Back Panel to the Interrupt IS Line
LOCK	Control Panel	CP7R/D (5A30)	LOCK = 0 means Control Panel functions are enabled; LOCK = 1 means Control Panel functions are inhibited.
MAD 00-15	CP7R/I (3B26-41)	GPB Slaves	Used with MAD 64-512 to represent a Memory Address in true value. MAD 00 is the most significant bit.
MAD 64-512	CP7R/I (3B42-43, 3A42-43)	GPB MENS	See above.
MSN	GPB Masters	CP7R/K (3A37)	A bidirectional line between all GPB Masters; originating from the Master selected to indicate to all other Master that a Master is selected.

Table 13.2a INTERFACE SIGNALS (CONNECTORS 1,3, 5)-CONT'D

Signal Name	Source (Pin No)	Destination (Pin No)	Description
OKO	CP7R/L (3A16)	Next Master	The Bus Controller sends OKO to search for the highest priority of the Master requesting the Bus.
OKIO/OO	CP7R/L (1A35	CP7R/L (1B35)	Derived from the OKO signal OKIO is the input to IOPO, and OKOO is the output of IOPO.
OKI1/O1	CP7R/L (1A36)	CP7R/L (1B36)	Derived from the OKO signal OK11 is the input to IOP1 and OKO1 is the output of of IOP1.
OSC	CP7R/A (5A17)	FPP	Derived from the CPU basic clock frequency of 45nSec.
OPSON-3N	Remote Device	CP7R/J (5B26-29)	Four address lines, the code of which is used to address the last sixteen words of the Bootstrap.
PAFN	CP7R/G (5B20)		Page Fault
PWFN	Power Supply	CP7R/K (3A17)	Indicates to the CPU that a Power Failure has occurred. The CPU only enters the Power Fail Routine if the failure is for 10mS or more. If less than 10mS the Power Failure is ignored.
RESETN	CP7R/D (5B34)	Control Panel	Derived from the Power Supply signal RSLN signal RESETN is the Master Reset for the Control Panel
RSLN	Power Supply	CP7R/A (3B17)	To ensure an orderly start procedure this signal stays low until power has stabilised.
RTCE		CP7R/G (5A35)	Real Time Clock Enable
SDMP	CP7R/D (5A34)	Control Panel	Serial Data Master to Panel
SDPM	Control Panel	CP7R/D (5A31)	Serial Data Panel to Master
SPYC	CP7R/K (3A35)	Masters	Scan Priority Chain (Low active)
TMEN	CP7R/K (3A30)	Ext. Reg.	Timing Master to External Register, active low to validate the addresses and data; this signal also resets the Timeout Circuit.
TMFN	CP7R/G (5B12)	FPP	Timing Master to Floating Point Processor, active low to validate the addresses and data.

Table 13.2a INTERFACE SIGNALS (CONNECTORS 1,3, 5)-CONT'D

Signal Name	Source (Pin No)	Destination (Pin No)	Description
TMRN	CP7R/K	Memory	Timing Master to Memory, active low to validate addresses and data. This signal also resets the Timeout Circuit.
TMPN	CP7R/K (3A31)	C.U.	Timing Master to Peripheral (C.U.) active low to validate addresses and data. This signal also resets Timeout Circuit.
TPMN	CP7R/K (3A32)	Master	Timing Peripheral to Master, active low to validate data. Reply to TMPN.
TRMN	CP7R/K (3A28)	Master	Timing Memory to Master, active low to validate data. Reply to TMRN or TMEN.
SCEIN	CP7R/E (3A05)		Scan External Interrupts
RTCZ1N	Power Supply	CP7R/G (5B25)	
WRITE	CP7R/I (3A26)	GP Bus	Indicates to the GPB Slaves the direction of Bus Transfer; WRITE = 1 means Transfer Master to Slave, WRITE = 0 means Transfer Slave to Master.

Table 13.2a INTERFACE SIGNALS (CONNECTORS 1,3, 5)-CONT'D

Pin	Sig. Name	Description
6B01	ROMAD08	)
02	07	)
03	06	)
04	05	) Micro-program ROM Address Lines, note
05	04	)- that only 9 of the 11 lines are available
06	03	) here, for ROMAD 09 and 10 see pins 6A17 and 6A18.
07	02	) (CP7R/B)
08	01	)
09	ROMAD00	)
10	BSYIOP	(CP7R/L)
11	BSYCPUB	Indicates CPU busy with Bus (CP7R/K)
12	TMP	Indicates Transfer Master to Peripheral (CP7R/K)
13	TMR	Indicates Transfer Master to Memory (CP7R/K)
14	OSCENB	Enables the internal clock (CP7R/A)
15		)- Not used
16		)
17	RSLFN	Simulates RSLN from the Power Supply (CP7R/A)
18	APA	Enables an external test of the CPU Sequencer signal
19	5V	AP (CP7R/A)
20	5V	
6A01	D00	)
02	01	)
03	02	)
04	03	)
05	04	)
06	05	)
07	06	)
08	07	)
09	08	)- 3 - state internal CPU Bus (CP7R/D)
10	19	)
11	10	)
12	11	)
13	12	)
14	13	)
15	14	)
16	D15	)
17	ROMAD10	)
18	ROMAD09	)- See pin nos 6B01-6B09
19	0V	)
20	0V	

Table 13.3 TEST CONNECTOR NO. 6 (DEVELOPMENT ONLY)

13.4 V24 CONTROL UNIT

13.4.1 GENERAL

An USART 8251 is used as interface between Console Typewriter and CU.
The type 8251 is also used for the interface Control Panel - CPU.

USART : Universal Synchronous Asynchronous Receiver Transmitter.

CTW : Selectable baudrate : 50 - 19.200 baud.
Panel : Fixed baudrate : 4800 baud.

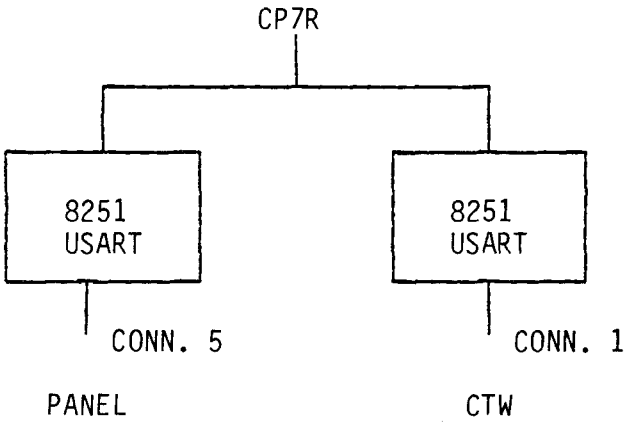


Figure 13.3 V24 AND PANEL INTERFACE

STRAPS : 5 straps total (baudrate and CT133)
CU Address : /10 (fixed)
Int. level : 7
HSI : see page 13-13

13.4.2 FACILITIES

I/O DEVICE INTERFACE

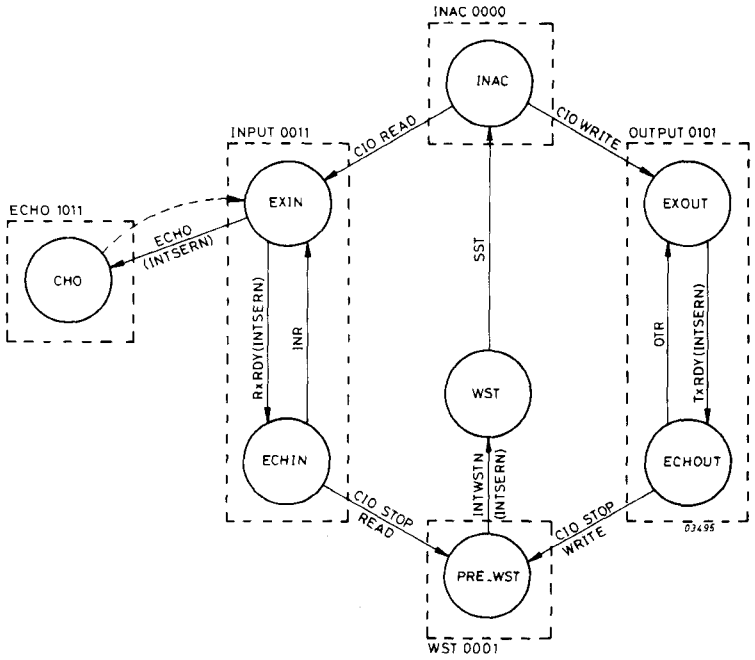
* Connection to an I/O device having V24/28 interface according CCITT.
* Programmed channel with or without using interrupt handling.
* The CU is working in half duplex mode. However, the line to an I/O device may be a so called 4 wire connection. 4 Wire line connection allows echo mode (software selection).
* The V24 line 'Ready For Receiving' CT133/CT119 may control the throughput during the output mode. (Used by PER3100). To be selected by a strap.
* Used V24 lines: CT101, 102, 103, 104, 107, 108, 109, 133. CT 107/108 must be controlled by CU/CTW.
* Break detection in order to set control panel interrupt.
* Transfer rate 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19.200 bits/sec.
* Character of line composed of:
  - 1 Start bit, rec. 1 or 2 Stop bits, trx. 2 Stop bits (normally).
  - 8 Data bits
  - Software selectable (parity bit) (number of stop bits).
  - Device address /10 (non selectable)

PANEL INTERFACE

* A-synchronous interface according CCITT V28 for serial transmission and reception.
* Transfer rate 4800 bits/sec.
* Character on line composed of:
  - 1 Start bit, (at least) 2 Stop bits.
  - 8 Data bits
  - (no parity)

Note: For interface connections see chapter 4 - figure 36, 37.

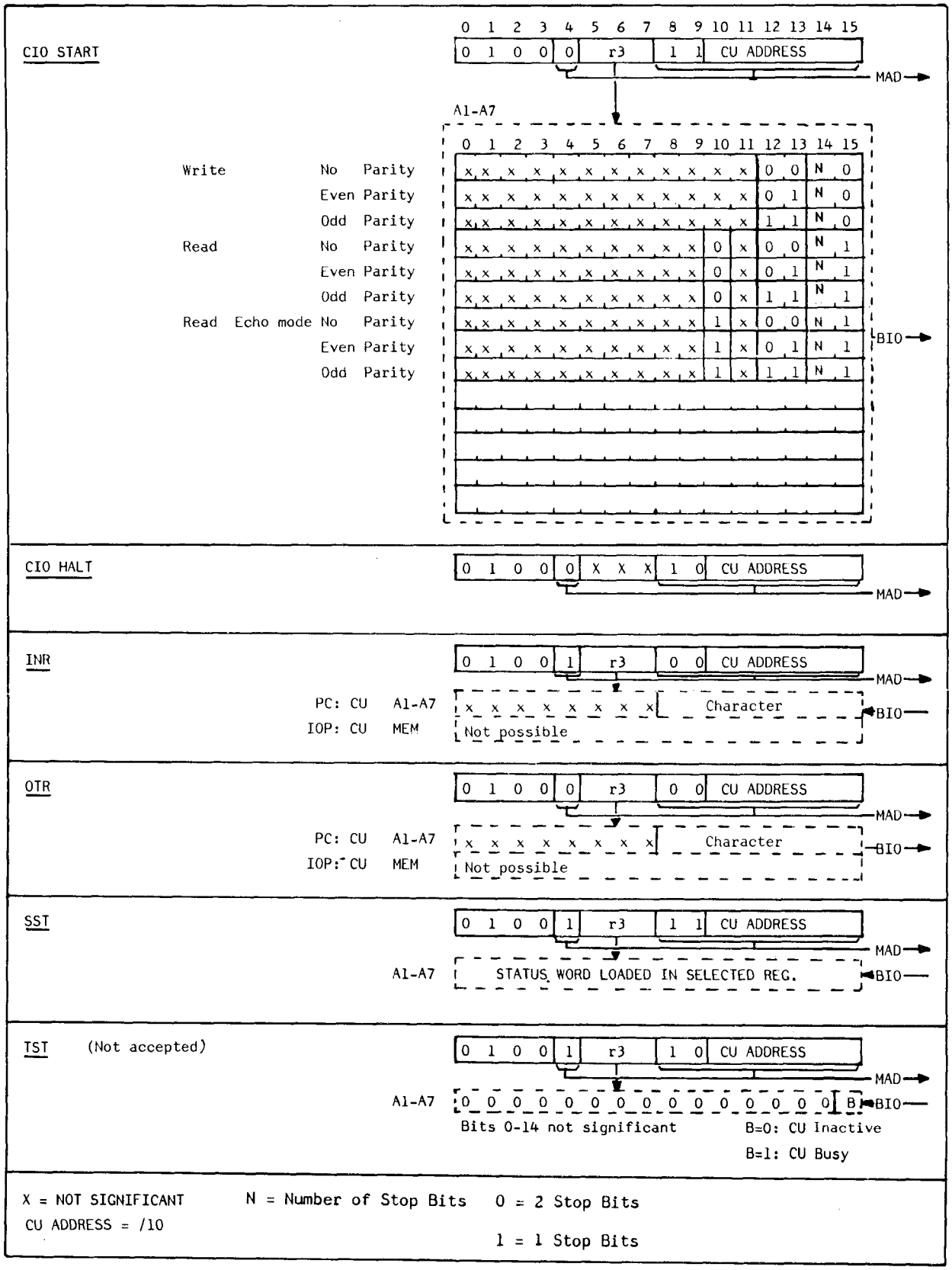
13.4.3 CONTROL UNIT STATES



Note: The states of the V24 Interface have a different significance at CPU level. Only ECHO, OUTPUT, INPUT are read by the V24 Status Indicators. When these bits are all zero, the CU is in the Inactive State.

Figure 13.4 V24 INTERFACE STATES

13.4.4 HARDWARE-SOFTWARE INTERFACE DETAILS V24

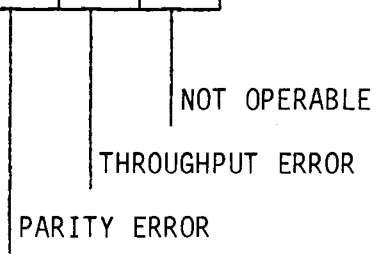


Note: * Bit 14 = 1: only one stop bit (necessary it terminal operates with one stop bit

Figure 13.5 INSTRUCTION-/COMMAND-WORD FORMATS

13.4.4.1 STATUS WORD

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0	0	0	0			



NOT OPERABLE

Bit 15 is set if the device is not connected or not operable.

THROUGHPUT ERROR

Bit 14 is set during input mode, if the interrupt is not yet answered by the CPU (INR) and the next input character arrives.

PARITY ERROR

Bit 13 is set when during input mode the received character has incorrect parity.

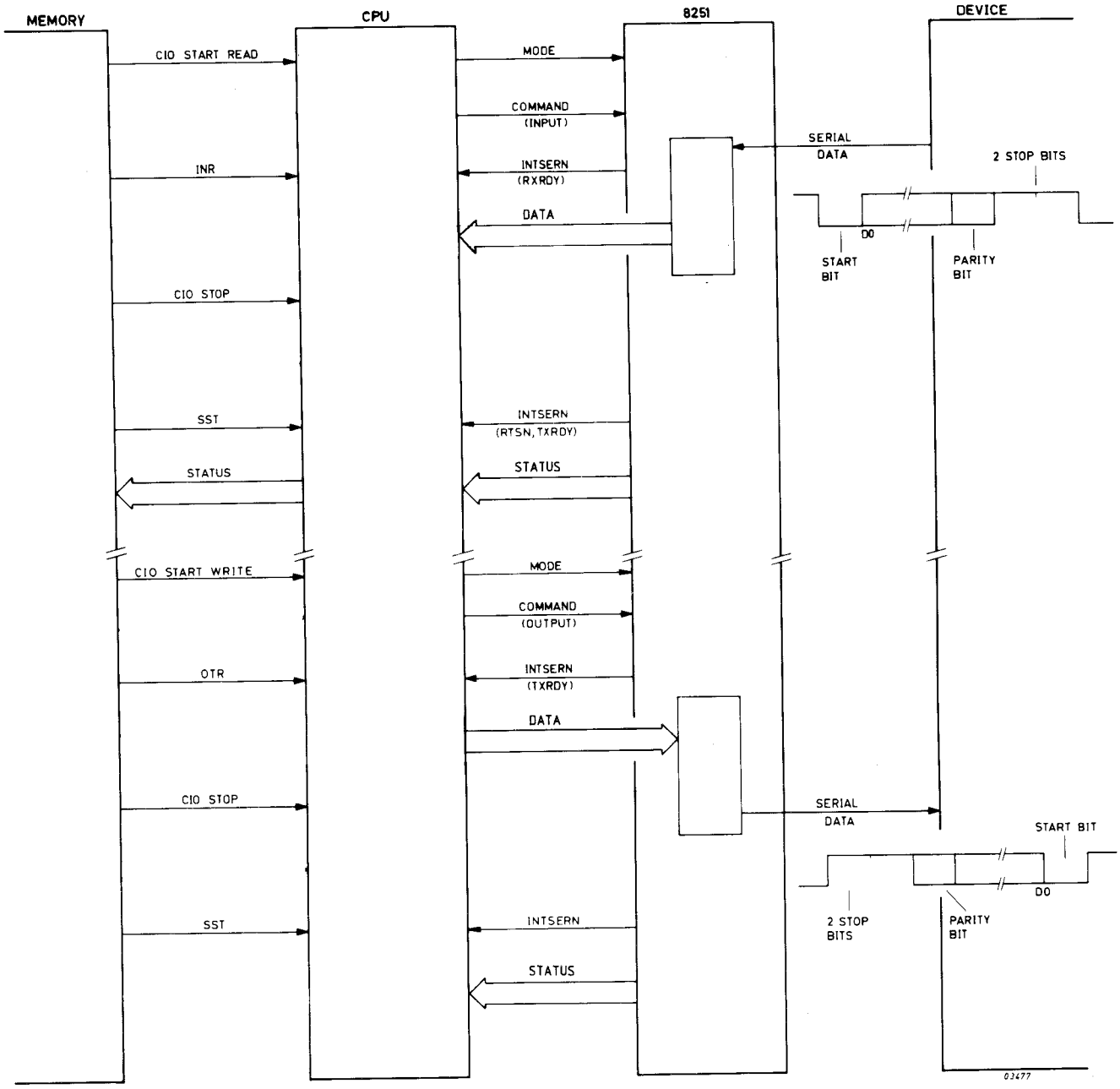


Figure 13.6 V24 PERIPHERAL INTERFACE DIALOGUES

13.5 HARDWARE SOFTWARE INTERFACE DETAILS CPU

In case the CPU detects either an unknown instruction code or a priviledged instruction in USER mode, the CPU will jump to the TRAP routine.
Actions executed by the CPU are slightly different from an interrupt:

- store Program Counter (here: address of the 'wrong' instruction
- store PSW (save condition register)
- update A15 (for possible interrupt)

] STACK

- INHibit for interrupts
- USER to SYSTEM mode
- ABI to address /7E

(/7E contains the startaddress of the TRAP routine)

Memory Layout of Interrupt and Trap Table:

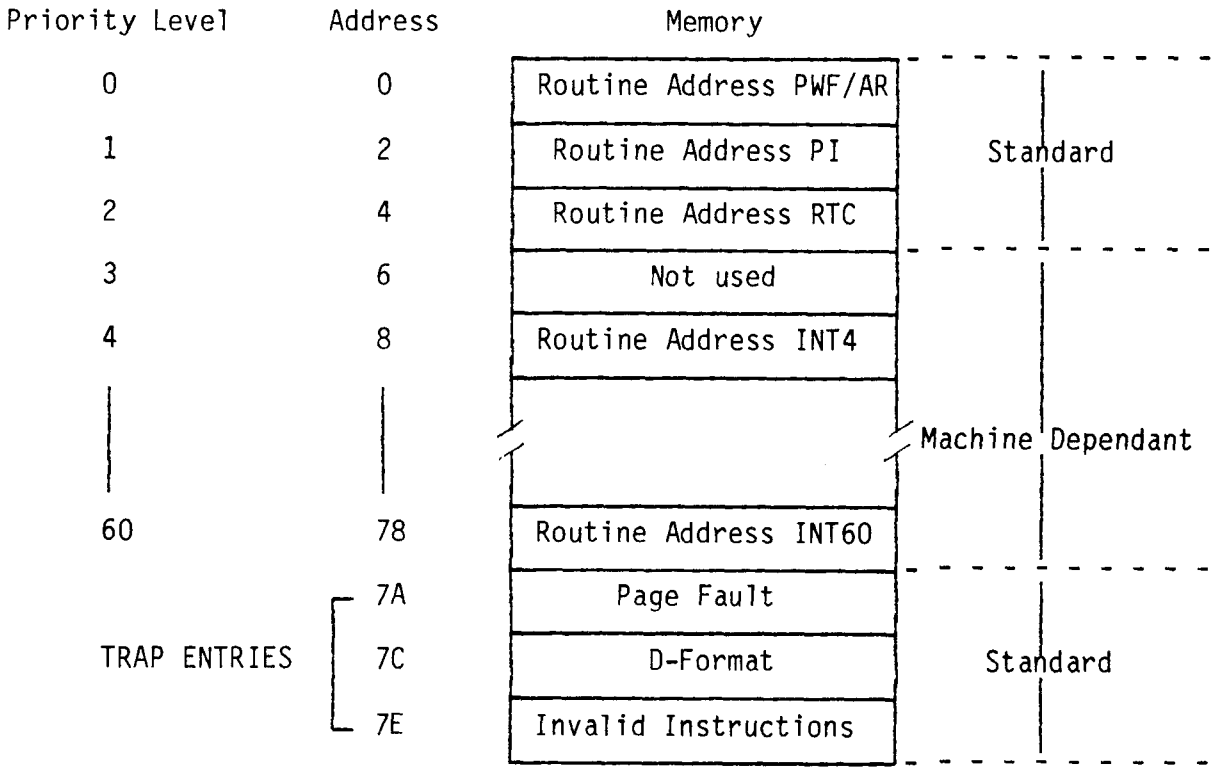


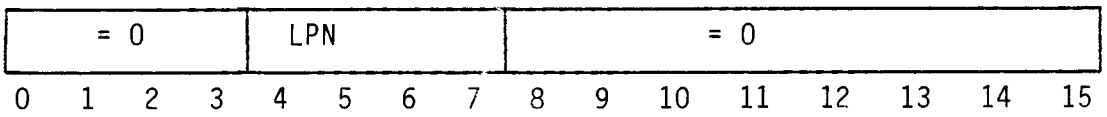
Table 13.4 INTERRUPT/TRAP LEVELS

Three kinds of traps can occur:

Memory Access Fault

Trap entry: /7A
This trap is activated whenever the CPU (User Mode) is informed of a "Page Fault" detection in the Memory Management Unit. For the particular trap, in addition to the P and PSW registers, a third parameter is pushed up into the stack: the 3rd word contains the Logical Page Number (LPN) on which the page fault was detected:

FORMAT:



Not Wired Instruction in D-Format

Trap entry: /7C
This trap can be used for software simulation of not wired instructions of the D-format type (OPC = 1101, T8 mode).

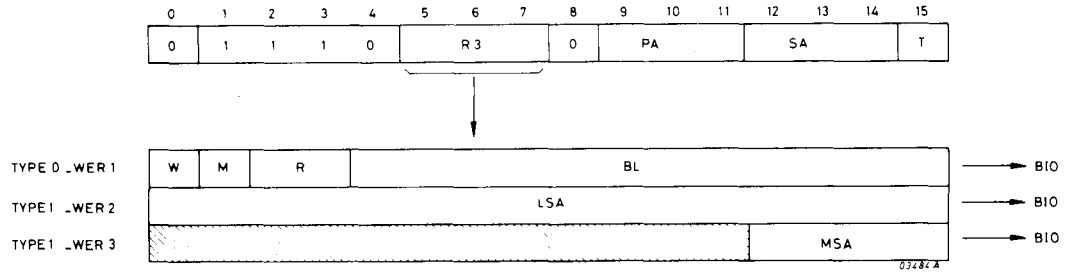
Invalid Instructions

Trap entry: /7E
This trap is dedicated for "abort" action if any of the following are detected:

. non-existing instructions
. privileged instructions detected in User Mode
. system stack access in User Mode

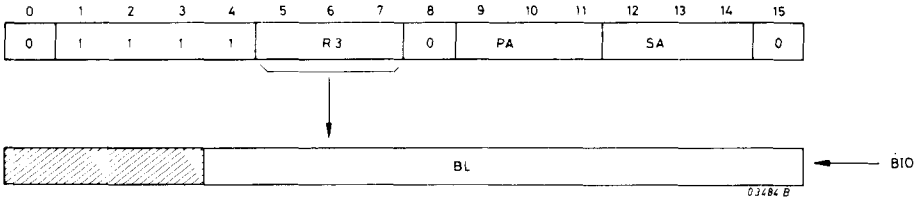
13.6 HARDWARE SOFTWARE INTERFACE DETAILS MIOP

13.6.1 IOP WRITE EXTERNAL REGISTER INSTRUCTIONS (WER)



PA IOP Address; for MIOP always 000 or 001 (IOPØ or IOP1).
SA Sub-channel address linked to PA to give the 6-bit C.U. address.
T Type of WER = 0 (WER 1), = 1 (WER 2 and 3).
W Word Transfer Indicator: = 0 transfer is an 8-bit character
M Output Mode: = 1 direction of exchange is memory to C.U.
R Address Bits (MAD128 and MAD64). If WER 3 is used these bits are overwritten by the MSA Field.
BL 12-bit block length: depending on W the block length is eiher a number of words or characters. When BL = 0 the length is 2^{12} words or bytes.
LSA Least significant bits of the memory start address of the block to be read or written.
MSA Most significant bits of the memory start address.

READ EXTERNAL REGISTER INSTRUCTION (RER)



PA IOP Address: for MIOP always 000 or 001 (IOPØ or IOP1).
SA Sub-channel address: linked to PA to give the 6-bit C.U. address.
BL Indicates the remaining length to be transferred.

Figure 13.7 IOP COMMAND FORMATS

13.6.2 MEMORY MANAGEMENT UNIT - FUNCTIONS

The Memory Management Unit (MMU) is a hardware facility which provides extended memory addressing and memory protection facilities for the P857R system.

EXTENDED MEMORY ADDRESSING (TRANSLATION)

The principal function of the MMU is to extend the memory addressing up to 512K physical words (20 address bits). (See Figure 13.8).
The basic rules for the operation of this facility are as follows:

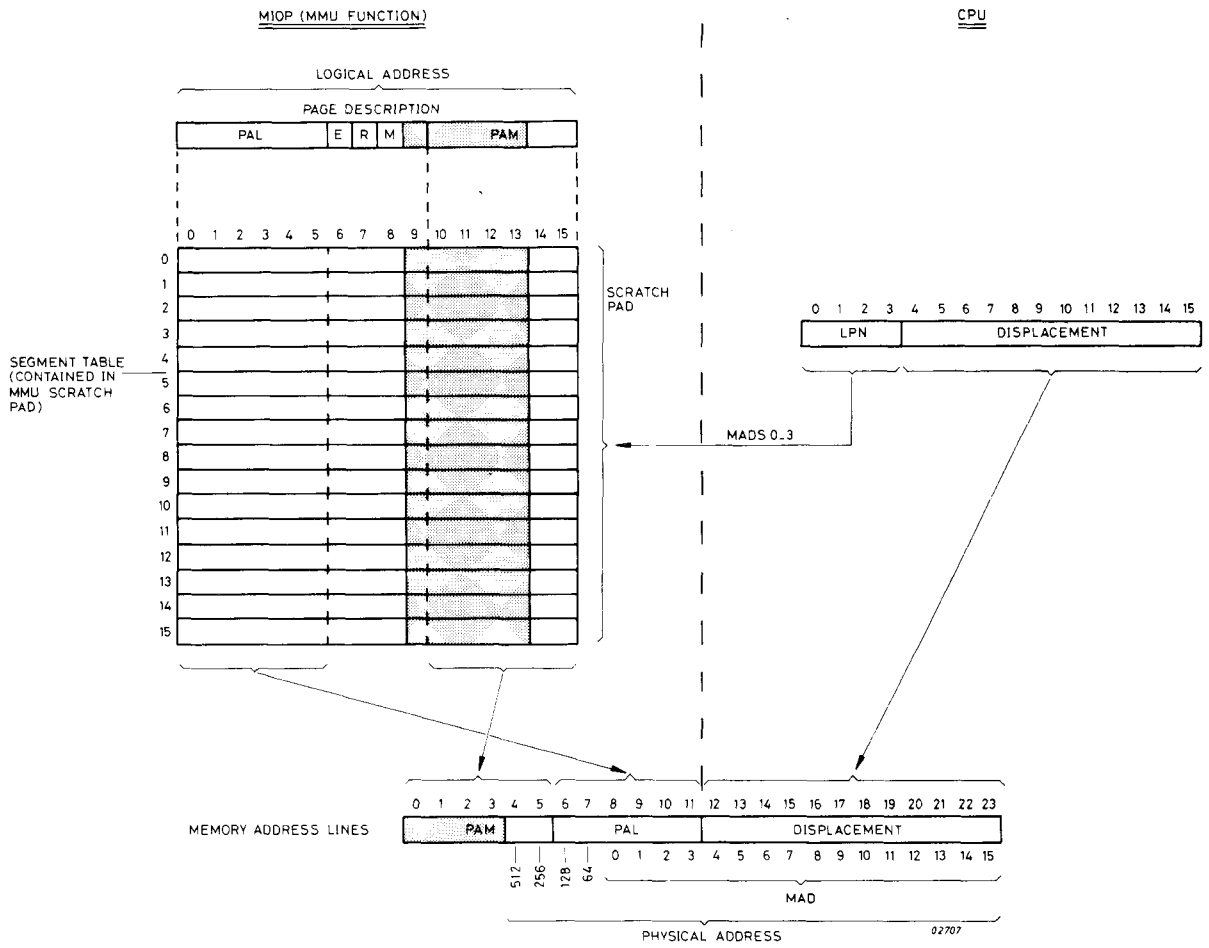
- A 16 segment table is pre-loaded with page addresses by one Table Load Instruction.
- All CPU/Memory transfers via the MMU use the four most significant address lines (MAD0-3) to select the table segment (page 0-15). The content of each page gives the 8 most significant MAD address bits plus 3 control bits.
- The Table Store instruction is used by software to read the 16 word segment table for test purposes or for dynamic relocation.

MEMORY PROTECTION

For memory protection purposes 2 information bits are loaded into the segment table at the same time that the TL instruction loads the page addresses; these information bits are:

- Bit 6 (E) Page Error if 1 page restricted to system mode only.
- Bit 7 (R) Read Only Indicator = 1 to protect the page against Write operations If a program in User Mode attempts to Write on this page then the translation is blocked.

In both of these cases the MMU indicates to the CPU that a Page Fault (PAF) has occured.



ABBREVIATIONS

PAL	— PAGE ADDRESS LEAST SIGNIFICANT
PAM	— PAGE ADDRESS MOST SIGNIFICANT
E	— PAGE ERROR; = 1 EXCEPT FOR MEMORY RESIDENT PAGES OF USER PROGRAM
R	— READ ONLY INDICATOR; = 1 TO PROTECT THE PAGE AGAINST WRITE OPERATIONS
M	— MODIFIED INDICATOR; = 1 WHEN A WRITE OPERATION IS PERFORMED FOR THAT PAGE
LPN	— LOGICAL PAGE NUMBER
DISPLACEMENT	— GIVES THE ADDRESS RELATIVE TO THE BEGINNING OF THE LOGICAL PAGE NUMBER
MAD	— MEMORY ADDRESS LINES

Figure 13.8 MEMORY MANAGEMENT

MODIFIED PAGE

This feature indicates to the operating system if a page needs to be "swapped out" or not. If it does not need to be "swapped out" then the new page can be overwritten so saving time. This possibility is indicated by bit 8 (M) which is set to "1" by the MMU whenever a Write operation (Store Instruction) is performed on a specific page.

PAGE FAULT

When an attempt is made to write into a protected page or access is made in user mode to a page that is restricted to system mode only, the MMU signal "Page Fault" initiates an interrupt TRAP Routine at the CPU. The sequence of events is indicated in the following Flow Chart:

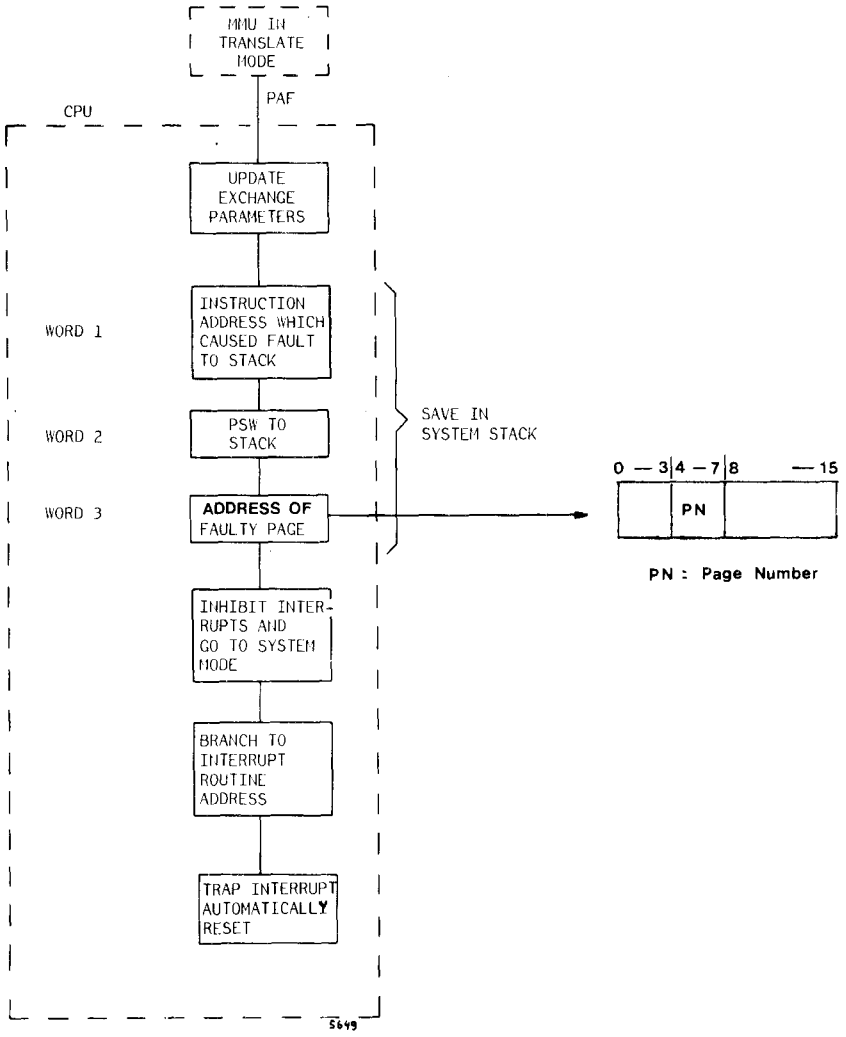


Figure 13.9 PAGE FAULT SEQUENCE

13.7 POWER SWITCH ON AND TEST

At switch-on a sequence of events takes place before the system is ready to go. This sequence of events may be considered as three separate phases.

. Phase 1 Automatic Test
. Phase 2 Microdiagnostic Test (only necessary if problems are expected)
. Phase 3 Load IPL (Initial Program Loader)

The hexadecimal codes of the HHCP and FRCP that are displayed after an event are indicated in the following flowcharts.

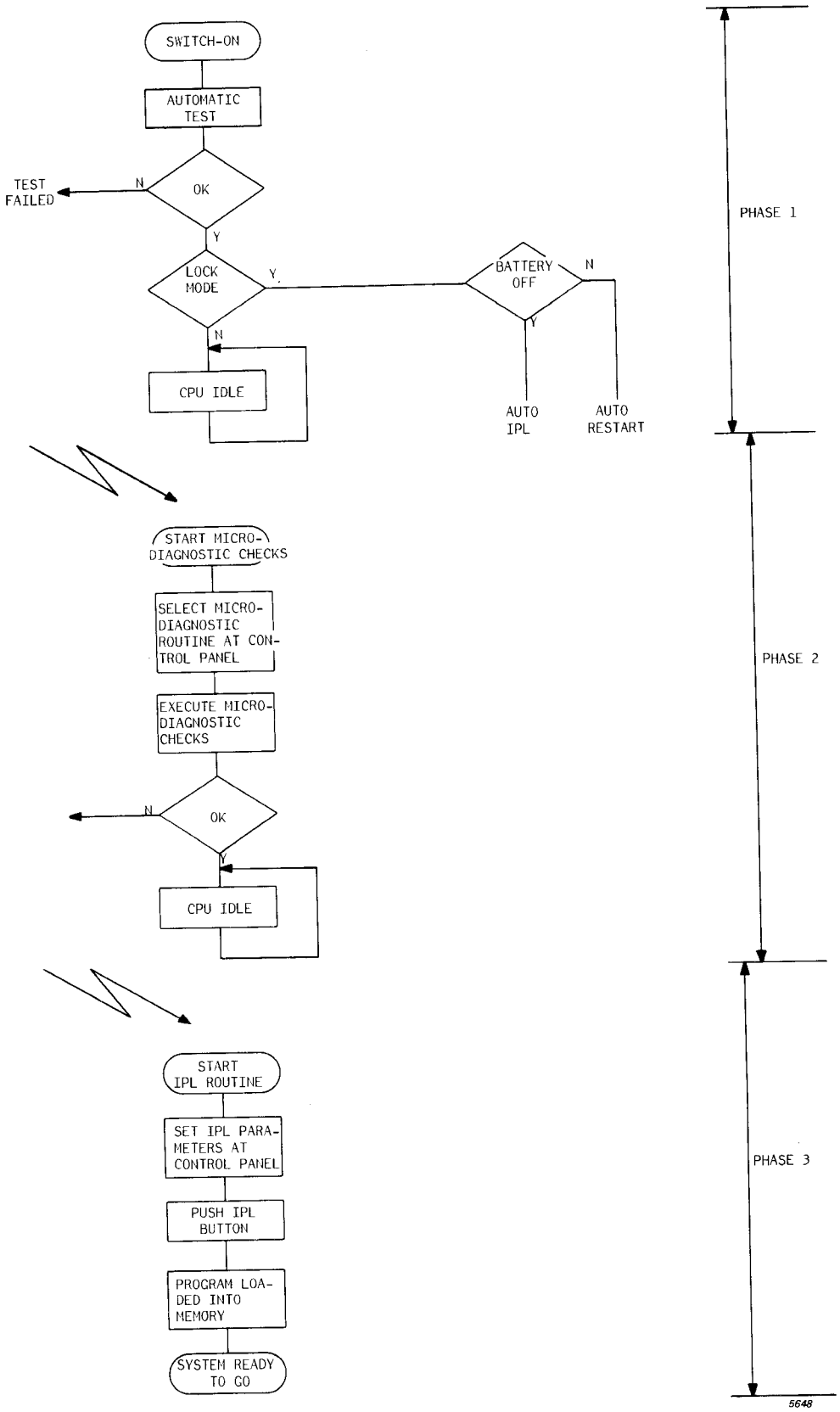


Figure 13.10 START PROCEDURE

13.7.1 AUTOMATIC TEST

An automatic test is executed at the power-on time. It tests the major part of the C.P.U., the Control Panel Interface, a part of the Control Panel itself and its cable. This test is terminated by displaying a code (FFFC) if the panel was not in LOCK state and if the test was O.K.

This automatic part of the test is of "go-no go" type. If the expected code is not displayed it is not possible to distinguish if the problem is due to the C.P.U., to the Control Panel or its cable and it is not possible to run further tests.

But if this first phase runs well and if displaying is possible and correct, in the second phase the C.P.U., C.U. and Memory failures could be distinguished from one another.

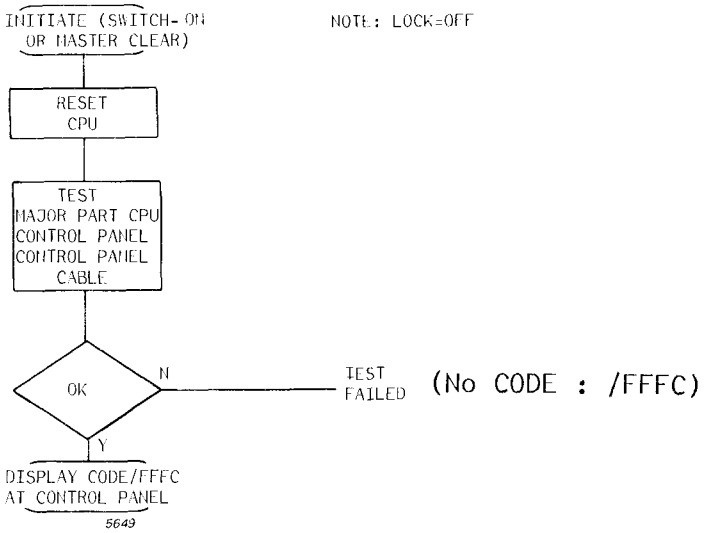


Figure 13.11 AUTOMATIC TEST

13.7.2 MICRODIAGNOSTIC TEST

The second phase is initialized by pressing the 0 and TEST push buttons on the Control Panel and it consists of the end of the C.P.U. test, RAM test (up to 32K), CPU-CU V24 (Address /10) dialogue test and MMU/IOP (MIOP) test.

At the end of this second phase, another code is displayed meaning either the correct end of test or an error.

These codes are:

C.P.U. error : Code 0001
BUS or CU error : Code 0002 or YY02
BUS or RAM error : Code XX03
O.K. : Code YY04
MIOP error : Code YY10

XX = Most significant 8 bits of the memory address causing the error.
YY = Most significant 8 bits of the last memory address.

The operator can read the address causing the error in A1, and the contents of this address read by the CPU in A2.

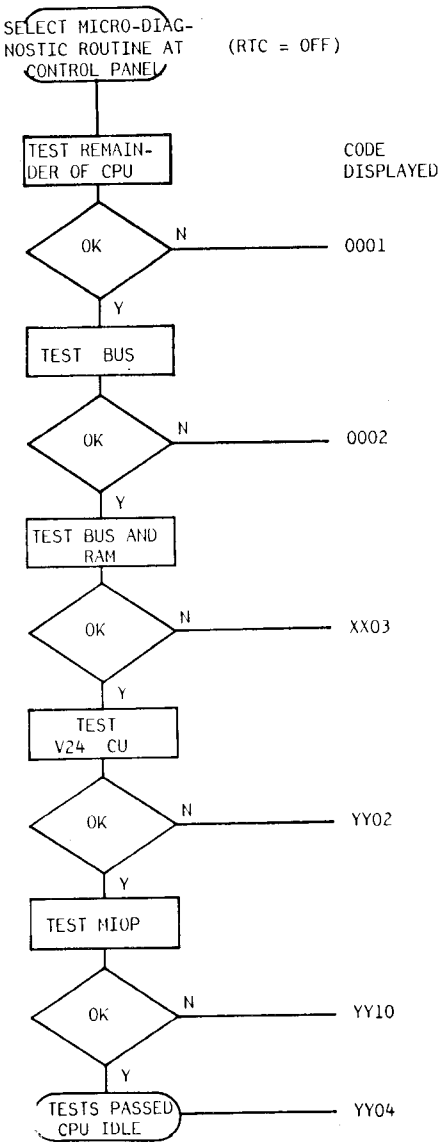


Figure 13.12 MICRODIAGNOSTIC TEST

13.8 SHORT DESCRIPTION OF TESTPROGRAMS

TESTPROGRAM TP 57 RE (PTS-108)

Mem. size 8Kw.
No output on CTW.
No power failure allowed.

Procedure:

. IPL

For this program the number of runs is output in hexadecimal format on sop panel. If an error occurs the count is stopped but no information on the error is done. It is only a GO/NO GO test.
If a parasitic interrupt occurs, its level is output on the sop panel with flashing lamps.

One complete CPU test lasts 1 - 2 seconds.

Tested: all CPU instructions are tested one by one.
I/O instructions and bus controller are not tested.

Procedure 5111 991 11291 = procedure CP57RE 5111 991 10353
with addendum PTS6000 5111 991 11381

Listing 5111 991 11201
Program 5111 991 62531

PROGRAM TEPAF (PTS-110) 32kw mem. min.
test for page fault, RTC also allowed.
test of auto restart

.IPL

- switch on the RTC (LOCK for PF/AR)
- The program loops continuosly.
(one loop lasts about 0.1 sec.)

For this program the number of runs is output in hexadecimal format on sop panel. If an error occurs the count is stopped but no information on the error is done. It is only a GO/NO GO test.
If a parasitic interrupt occurs, its level is output on the sop panel with flashing lamps.

--- for more info: see official description of testprograms ----

- Tested: correct processing of a page fault trap
correct resuming of the instruction, which caused the page fault
correct handling of RTC and Power Failure.

Procedure 5111 991 11311 = Procedure REPAF 5111 991 10371
with PTS6000 addendum 5122 991 11381

Listing 5111 991 11221

Program 5111 199 62511

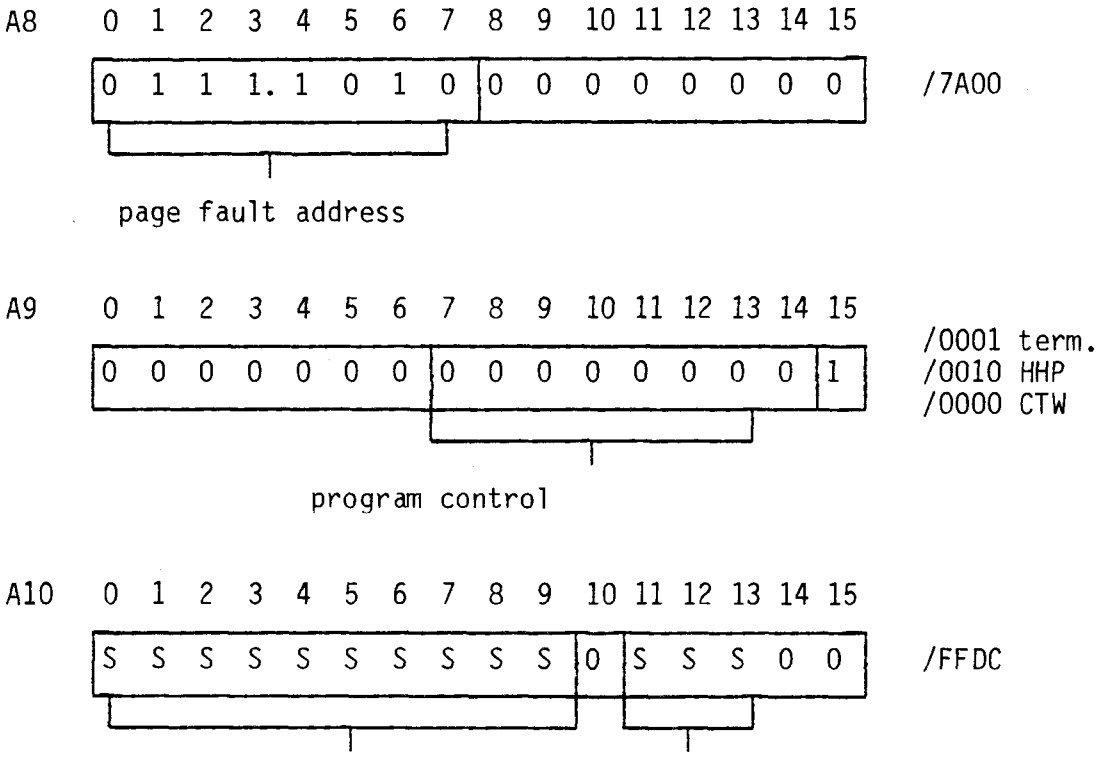
PROGRAM TEMMU1 (PTS-109)

mem. size 32 kw min.
test of MMU in memory size 0 - 32kw.
RTC, PF/AR allowed.

. IPL

. display /700 = restart point = after reception of unexpected interrupt.

- change registers:



- switch on RTC

The check which is executed, is displayed on the terminal.

. /700 normal end

. /5E0 info stop

- /5F0 error stop A1 contains error code.
(see also official description of testprogram).

Note: some checks are in inhibit mode. In such a case the power fail interrupt may be handled too late and auto restart fails.

13.9 SHORT ROUTINES

For CTW see chapter 9.6

13.9.1 SHORT ROUTINE MMU

```
00000                                   IDENT    MMU2
00001                           *
00002                           *
00003                           *PROGRAM TO TEST MMU FUNCTIONS
00004                           *
00005                           *THE USER PART OF THIS PROGRAM WILL BE TRAPPED ON A NOT ALLOWED
00006                           *STORE OPERATION IN PAGE 2.
00007                           *EACH TIME THE CP-INT BUTTON IS PRESSED, THE PROGRAM WILL BE
00008                           *MODIFIED, GIVING TRAPS ON ACCESS PAGE 1 OR WRITE ACCESS PAGE 2
00009                           *WHEN THE PROGRAM IS STOPPED BY A HLT INSTRUCTION IT IS POSSIBLE
00010                           *TO CHECK THE SYSTEM STACK (A15) AND THE SEGMENT TABLE (/300).
00011                           *
00012          0006     CPLEV   EQU      6                    FOR P854: /E IF P858/P859; C IF PTS 6814/24
00013                           AORG     /100
00014  0100    8841     PROGINT TS       /300                 SEGMENT TABLE TO MEMORY
       0102    0300
00015  0104    20F8             RIT      /1D
00016  0106    207F             HLT                           CHECKPOINT:TABLE + STACK
00017  0108    8840             TL       /200                 LOAD SEGMENT TABLE INTO MIOP
       010A    0200
00018  010C    87A0             LDKL     A15,/150             LOAD STACK POINTER
       010E    0150
00019  0110    8120             LDKL     A1,/FFE              PROGRAM COUNTER OF USER
       0112    0FFE
00020  0114    813F             STR      A1,A15               TO THE STACK
00021  0116    8120             LDKL     A1,/4041             PSW OF USER
       0118    4041
00022  011A    813F             STR      A1,A15               TO THE STACK
00023  011C    8120             LDKL     A1,/160              START ADDRESS TRAP ROUT.
       011E    0160
00024  0120    8141             ST       A1,/7A               PAGE FAULT TRAP ENTRY
       0122    007A
00025  0124    8120             LDKL     A1,/100              START ADDRESS PROG.INT ROUT.
       0126    0100
00026  0128    8141             ST       A1,2                 LEVEL 1
       012A    0002
00027  012C    8120             LDKL     A1,/400              START ADDRESS CPINT ROUTINE
       012E    0400
00028  0130    8141             ST       A1,CPLEV             LEVEL:P854=3,P858/9=7
       0132    0006
00029  0134    F03E             RTN      A15                  START USER PROGRAM (LEVEL=/10)
00030                           AORG     /160
00031  0160    8841     TRAP    TS       /300                 SEGMENT TABLE TO MEMORY
       0162    0300
00032  0164    207F             HLT                           CHECKPOINT:TABLE + STACK
00033  0166    8120             LDKL     A1,/200C             RESTART USER
       0168    200C
00034  016A    8141             ST       A1,/150              PROGRAM AT ADDRESS /200C (=/300C)
       016C    0150
00035  016E    813E             LDR*     A1,A15               A15 ADJUSTED +2 AFTER PAGE FAULT TRAP
00036  0170    F03E             RTN      A15
00037                           AORG     /200
00038  0200    0000     SEGTAB  DATA     /0000                SEGMENT TABLE PAGE 0
00039  0202    0400             DATA     /0400                PAGE 1
00040  0204    0D00             DATA     /0D00                PAGE 2
00041                           AORG     /400
00042  0400    8120     CPINT   LDKL     A1,/200              ROUTINE TO CHANGE TABLE :PAGE 1
       0402    0200
00043  0404    8141             XRS      A1,/202              BIT 6 (E) SET OR RESET
       0406    0202
00044  0408    200F             RIT      /0F                  RESET CONTROL PANEL INT.
00045  040A    F03E             RTN      A15                  GO BACK TO USER PROGRAM
00046                           AORG     /FFE
00047  0FFE    013F     USER    LDK      A1,/3F               PAGE 0 IS ACCESSED
00048  1000    1102     PAGE1   ADK      A1,2                 PAGE 1 IS ACCESSED
00049  1002    8F20             ABL      /2000                BRANCH TO PAGE 2 (/3000)
       1004    2000
00050                           AORG     /3000
00051  3000    8141     PAGE2   ST       A1,/500              STORE INTO PAGE 0
       3002    0500
00052  3004    8140             LD       A1,/2200             LOAD FROM PAGE 2
       3006    2200
00053  3008    8141             ST       A1,/2200             STORE INTO PAGE 2 (TRAPPED)
       300A    2200
00054  300C    2804             LKM                           CALL SYSTEM MODE VIA PROG. INT
00055  300E    0000             DATA     0
00056                           END
```