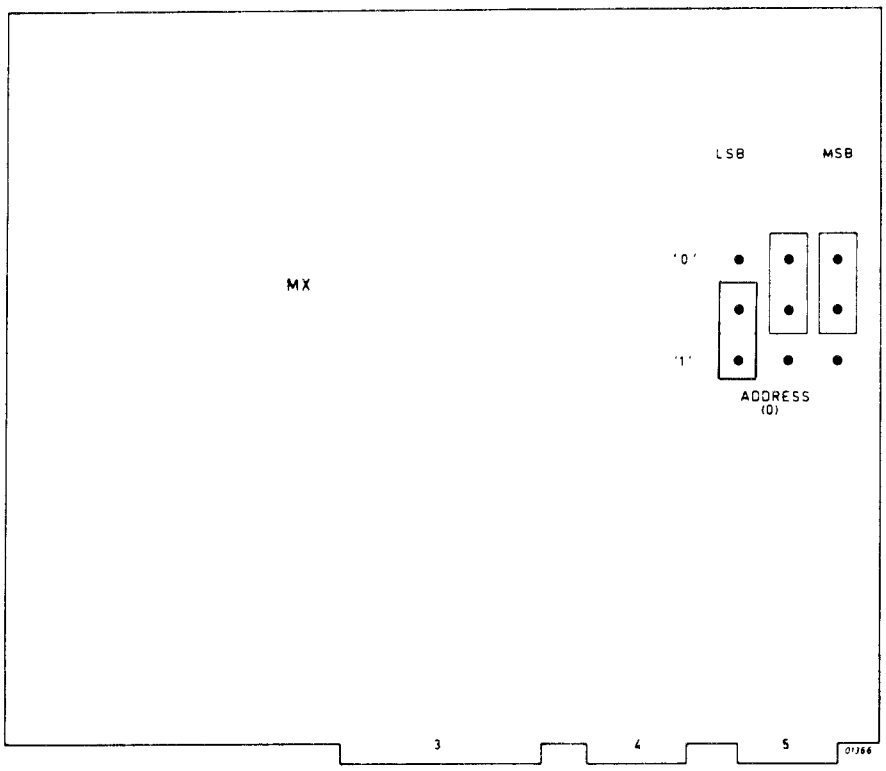
LIST OF ILLUSTRATIONS

LIST OF TABLES

12.1 IOP-IDENTIFICATIONS

Older version	:	MX only for 6810
	:	IOP PTS6827, P843-020
Power consumption	:	+5 Volt, 4 Amp.



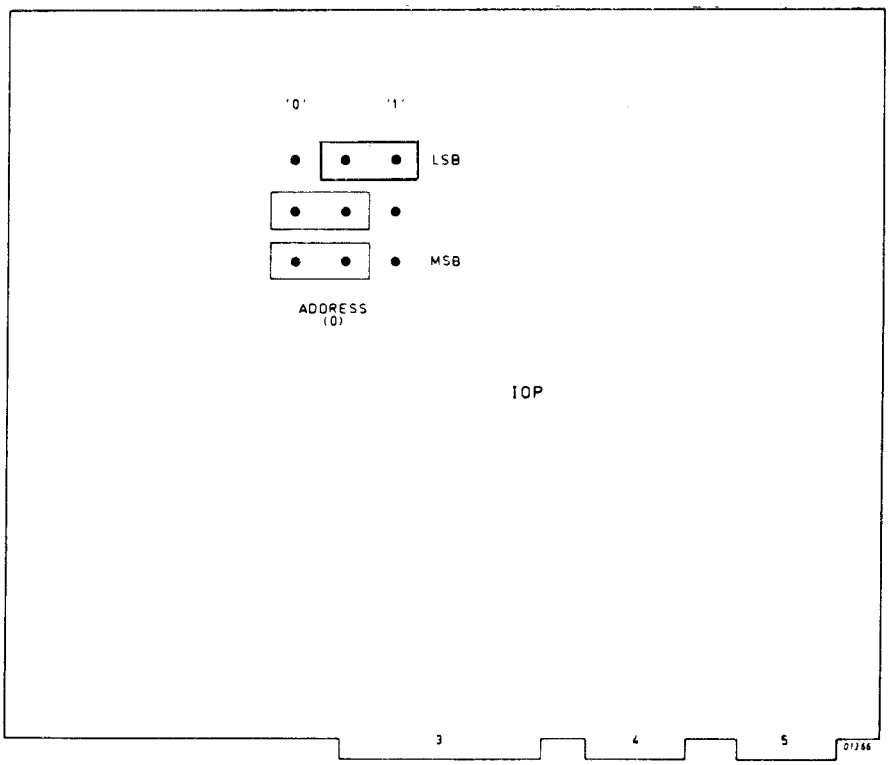


Figure 12.1 IOP/MX ADDRESS STRAPS

12.3 INTERFACE CONNECTIONS

Break Request Connections on I/O Processor Board

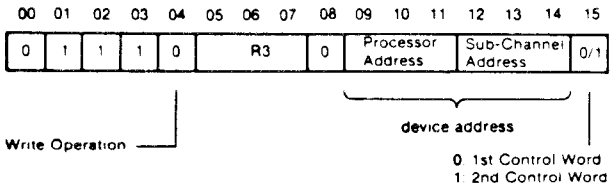
Signal	Pin No.		Signal	Pin No.
	5A01			5B01
	5A02			5B02
	5A03			5B03
	5A04			5B04
	5A05			5B05
BREX07N	5A06		0V	5B06
BREX06N	5A07		0V	5B07
BREX05N	5A08		0V	5B08
BREX04N	5A09		0V	5B09
BREX03N	5A10		0V	5B10
BREX02N	5A11		0V	5B11
BREX01N	5A12		0V	5B12
BREX00N	5A13		0V	5B13

Signal	Pin No.		Signal	Pin No.
BREX07N	4A06		BR07N	4B06
BREX06N	4A07		BR06N	4B07
BREX05N	4A08		BR05N	4B08
BREX04N	4A09		BR04N	4B09
BREX03N	4A10		BR03N	4B10
BREX02N	4A11		BR02N	4B11
BREX01N	4A12		BR01N	4B12
BREX00N	4A13		BR00N	4B13

Table 12.1 BREAK REQUEST CONNECTIONS TO CONNECTOR 4 AND 5

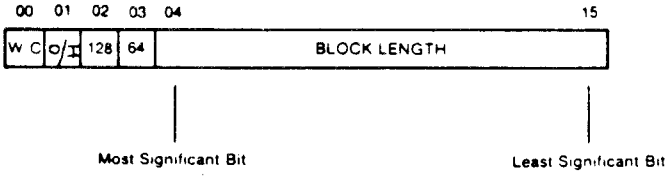
Initialization Operation

This operation is applied before commencing data transfer and the first part is controlled by the use of two write external register instructions WER to transfer two control words to the two working registers of the I/O processor subchannel. The instruction format is as shown below:



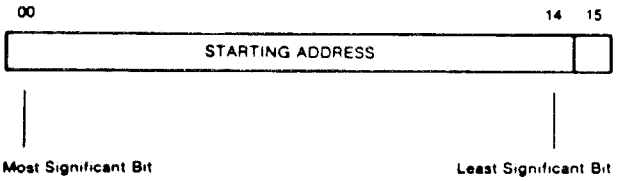
This instruction transfers the contents of the R3 field, previously loaded with a control word, to the external working register of the I/O processor specified by the device address bits 09 to 14.

The format of the first control word loaded is shown below:



Bit 00 = 1	Exchange is in word mode.
= 0	Exchange is in character mode.
Bit 01 = 1	Exchange is from memory to control unit.
= 0	Exchange is from control unit to memory.
Bits 04 to 15	specify the number of characters/words to be transferred.
Bits 02, 03	are positioned to become the two most significant bits of the second control word. (only for P-857)

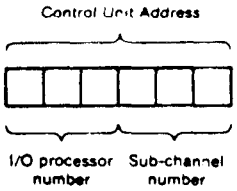
The format of the second control word loaded is as follows:



Bits 00 to 15	specify the starting address in memory.	
Bit 15 = 1	Right character is addressed	If transfer is
= 0	Left character is addressed	in character mode.

12.5 RELATIONSHIP BETWEEN BREAK SIGNAL AND CONTROL UNIT ADDRESS

An I/Q processor is coded with a 3-bit number which may range from 0 to 7 (coded by straps on the I/O processor) and each of the 8 subchannels associated with an I/O processor is also coded with a 3-bit number from 0 to 7. The combined 6-bit number gives the address of the peripheral control unit as shown below:



This address is used by the WER instruction to load the 2 control words into the working register of the I/O processor.

The 8 incoming break request signals BR00 to BR07 to each I/O processor correspond to each subchannel in the I/O processor as follows:

BR00N corresponds to subchannel 0
BR07N corresponds to subchannel 7

BR00N has the highest priority and BR07N the lowest.