10 CPU 857-6813



LIST OF ILLUSTRATIONS



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| 1A03 | CPFN |
| 1A04 | IS02N |
| 1A05 | PFFN |
| 1A06 | BIEC4 |
| 1A07 | BIEC2 |
| 1A08 | BIEC5 |
| 1A09 | IS06N |
| 1A10 | IS03N |
| 1A11 | IS01N |
| 1A12 | INTASRN (INTSERN) |
| 1A13 | |
| 1A14 | |
| 1A15 | |
| 1A16 | |
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| 1A33 | CT106 |
| 1A34 | CT107 |
| 1A35 | CT1082 |
| 1A36 | CT109 |
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| | |
|---|---|
| 1B01 | ASR LINE |
| 1B02 | RTC AN |
| 1B03 | SCEIN |
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| 1B12 | |
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| 1B25 | |
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| 1B28 | 5V |
| 1B29 | |
| 1B30 | |
| 1B31 | 0V |
| 1B32 | 0V |
| 1B33 | 0V |
| 1B34 | 0V |
| 1B35 | 0V |
| 1B36 | 0V |
| 1B37 | 0V |

Table 10.1 CPU B CONNECTOR 1 (V24 CU)

| | |
|---|---|
| 5A01 | |
| 5A02 | |
| 5A03 | |
| 5A04 | |
| 5A05 | |
| 5A06 | |
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| 5A13 | * GFETCH |
| 5A14 | * DONEFN |
| 5A15 | * FLOCR1 |
| 5A16 | |
| 5A17 | * OSCFLO |
| 5A18 | |
| 5A19 | * MMUABS |
| 5A20 | * DONEMN |
| 5A21 | * BOMFN |
| 5A22 | * FU |
| 5A23 | * S01 |
| 5A24 | * S03 |
| 5A25 | * SP02 |
| 5A26 | |
| 5A27 | * 0V |
| 5A28 | * 5V |
| 5A29 | BIOEKEY |
| 5A30 | UNLOCKN |
| 5A31 | RUNN |
| 5A32 | RCP00N |
| 5A33 | LOADRN |
| 5A34 | READSTN |
| 5A35 | RCP03N |
| 5A36 | LOADMN |
| 5A37 | READRN |

| | |
|---|---|
| 5B01 | * SP05 |
| 5B02 | * GBCPFN |
| 5B03 | * PREQN |
| 5B04 | * CPBABS |
| 5B05 | * TESTN |
| 5B06 | |
| 5B07 | |
| 5B08 | |
| 5B09 | |
| 5B10 | * SP04 |
| 5B11 | * SP01 |
| 5B12 | * TMFN |
| 5B13 | * BOFFN |
| 5B14 | * PLOCR0 |
| 5B15 | * FPPABS |
| 5B16 | |
| 5B17 | 0V |
| 5B18 | |
| 5B19 | |
| 5B20 | * MFAULTN |
| 5B21 | |
| 5B22 | * S00 |
| 5B23 | * S02 |
| 5B24 | * TMMN |
| 5B25 | * TMMU |
| 5B26 | |
| 5B27 | * 0V |
| 5B28 | * 5V |
| 5B29 | CPMCN |
| 5B30 | IPL |
| 5B31 | START |
| 5B32 | CPINT |
| 5B33 | RUNFA |
| 5B34 | RCP01N |
| 5B35 | RCP02N |
| 5B36 | READMN |
| 5B37 | INSTN |

Table 10.2 CPU B CONNECTOR 5

Notes: (device interfaces)

| Signal Name | Pin No's (Line Connector P5) | CPU | Conn. P7 |
|---|---|---|---|
| Ready for Receiving | 25 | CT 133 | 1A37 |
| Operational Signal | 19 | | |
| Operational Signal | 18 | | |
| Data Termin. Ready | 20 | CT 108-2 | 1A35 |
| Data Set Ready | 6 | CT 107 | 1A34 |
| Received Data | 3 | CT 104 | 1A32 |
| Transmitted Data | 2 | CT 103 | 1A31 |
| Protective Ground | 1 | CT 101 | |
| Signal Ground | 7 | CT 102 | 1B31-1B37 |

Table 10.3 PER 3100 INTERFACE

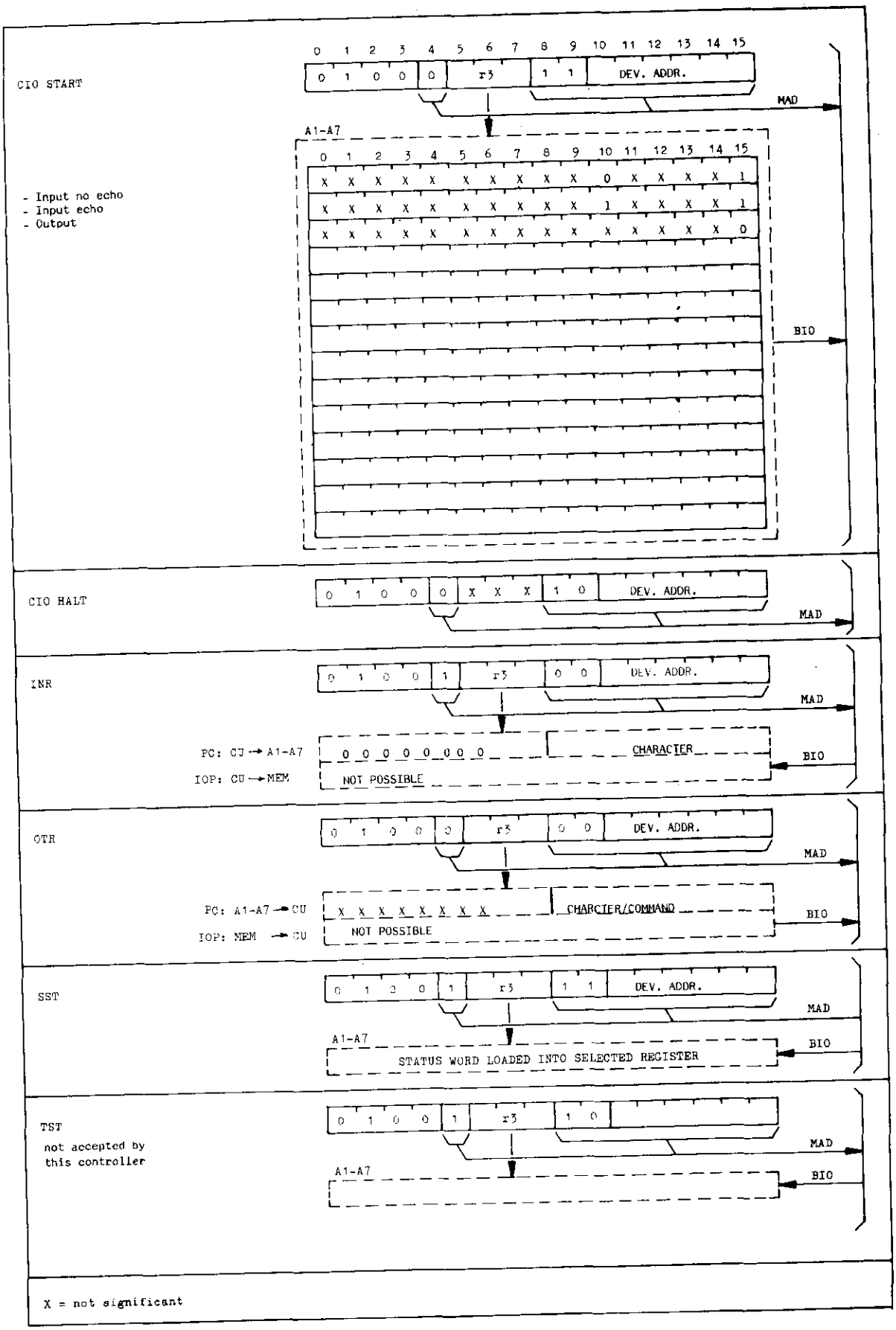
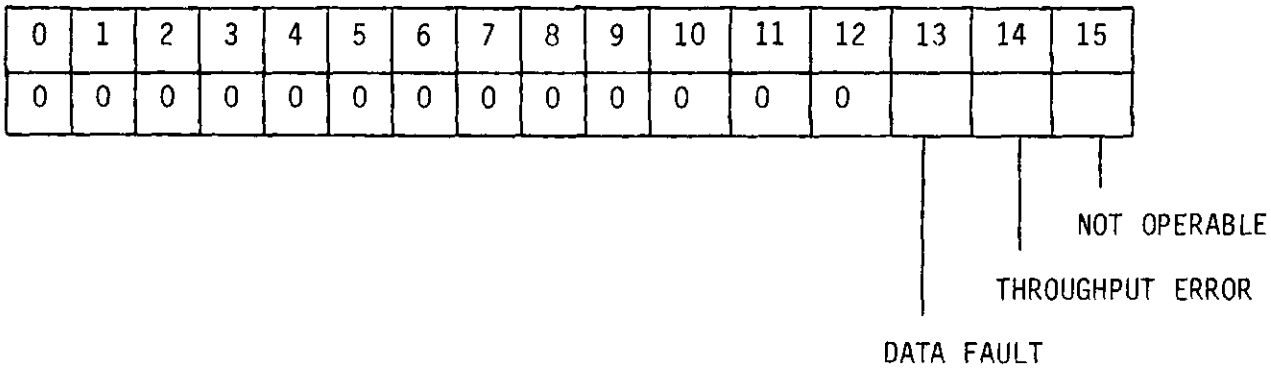



Figure 10.2 INSTRUCTION/COMMAND WORD FORMATS

10.4.1 STATUSWORD:




Not Operable

Bit 15 is set if the device is not connected or not operable.

Through put error

Bit 14 is set during input mode, if the interrupt is not yet answered by the CPU (INR) and the next input character arrives.

Parity error

Bit 13 is set when during input mode the received character has incorrect parity (not as is strapped).

## 10.5 SHORT DESCRIPTION TESTPROGRAMS

### MICRODIAGNOSTICS

The P856M and the P857M contain an automatic testing feature in the form of a microprogrammed diagnostic built into the CPU logic. Sucessful running of the tests indicate that sufficient parts of the CPU function for loading of test programs.

The microdiagnostics for the P856M test the first 4k of memory and for the P857M the first 16k of memory. The prerequisite tool is the FULL CONTROL PANEL or the EXTENDED CONTROL PANEL, as the results of the tests are displayed on the data lamps.

About 100 words are reserved for the microdiagnostic program.
The test can only be performed when the jumper NORM/DIGNOS IS in the DIAGNOS position see figure 4.2-1 and an EFP or CFP is fitted (On 6810 UK and earlier models of PTS 6813 force pin 5B05 on backpanel 1C to ground).

### TEST PROCEDURES

Before starting any test, except for steps A to D included in the Test 2. the user has to set a control unit address on data switches 2 to 7 included to check the dialogue through the Bus between the CPU and the control unit.

*Test 1 Automatic Test*
This is a fast check which automatically goes through a number of operations.
If the tests have been satisfactory special codes are displayed on the data lamps.

- set data switch 0 to 0
- set a control unit address on data switches 2 thru 7
- press RUN button
- wait for display of code no 4
  code 4: data lamp 12 off
  all other lamps lit
  if this code is not displayed go to Test 2
- press LM button and wait for display of code 5
  code 5: all lamps lit
  If the code is not displayed go to Test 2.

*Test 2 Step-by-step testing*
This sequence may be used if Test 1 showed an erroneous display or if the user wishes to perform separate tests. In these tests the user verifies the operation of the control panel up to the memory.

A. Control Panel test
Each data key and the lamp above it are tested by setting the key in the 'up' position after which the lamp must be lit.
Press LR button to go to the next step.

B. L register test
This step includes the GP BUS and the L register in the test. The operator may use the switches in the same way as described under control panel.
Press LR button to go to the M register test.

C. M register test
This step includes the M register (through the C selector and ALU) in the thest. The operator may use the switches in the same way as described under control panel. Press the LR button to go to the Q register test.

D. Q register test
This step includes the Q register in the test. The operator may use the switches in the same way as described under control panel.

From this moment on the operator may choose among three data path tests, an instruction simulation test or a memory test by setting on the data switches a hexadecimal number and a control unit address, followed by pressing the LR button.
If the relevant test is executed without errors the data lamps display a certain code.

It is possible to skip the visual tests A thru D. The user must then set switch 0 to 0, set a control unit address on switches 2 thru 7, and set switch 15 to 1. Next press the LR button 4 times. Then wait for display of code 1. Press LR button and wait for display of code 2. Press LR button and wait for display of code 3. Press LR (or RUN) button for display of code 4. Press LM (or LR) button for display of code 5.

*Test 3 Chained test*
In this mode the hardware is tested in a loop which may be stopped by operation of data switch 0.

- set data switch 0 to 1, a control unit address on switches 2 thru 7, and switch 15 to 1.
- press LR button 4 times. The microprogram starts looping.

To stop the loop:
- set switch 0 to 0.
  One of the 5 codes as listed above is displayed. If it is not code 5 press the LR button as many times until code 5 appears.

To restart the loop set switch 0 to 1.
To restart at the beginning of the test turn the key in the key switch to OFF and next to TEST. Set switch 0 to 1, set the control unit address, and set switch 15 to 1 and continue as described above.

| | Hexa no on data switches | Test functions | Display on data lamps when no fault is found |
|---|---|---|---|
| data path test | /0001 + CU address | - shift left Q reg.<br>- bus A selection<br>- constant 'TWO'<br>- QO test<br>- A or B, A+B and B inverted ALU functions<br>- ALU = 0 | code 1<br>lamp 15 OFF<br>all other lamps lit |
| data path test | /0002 + CU address | - shift right Q reg.<br>- ALUZERO<br>- A-B, A+B and crossed A ALU functions<br>- constant 'TEN'<br>- P reg. P - 2 function | code 2<br>lamp 14 OFF<br>all other lamps lit |
| data path test | /0004 + CU address | - A operand shifted right<br>- 4 x A function<br>- reading and writing scratch pad | code 3<br>lamp 13 OFF<br>all other lamps lit |
| instruction simulation | /0008 + CU address | DLA<br>- K is loaded with DLA code<br>- values loaded in A1 and A2<br>- branch to DLA micro program<br>- return to microdiagnostic program<br>RB<br>K is loaded<br>- RB microprogram next address generated by PLA | code 4<br>lamp 12 OFF<br>all other lamps lit |
| memory test | /0010 + CU address | - bit 15 is set to 1 in all addresses of a 4k/16k block<br>- the block is read and verified<br>- the 1 is shifted left 1 position etc.<br>next:<br>- all words of a 4k/16k block receive their address values as contents these values are verified<br>- tests the TMP-TPM dialogue | code 5<br>all lamps lit |

SHORT DESCRIPTION TESTPROGRAM CPUTSC SEE CHAPTER 9.5

## 10.6 SHORT ROUTINES

SEE CHAPTER 9.6