SECTION II

CPU LOGIC

2.1 GENERAL

The CPU logic is divided into functional sections shown in the block diagram, Figure 2-1. Detailed logic diagrams and a list of all CPU signals are located at the end of this section. A guide to the integrated circuits is provided in Section IV. The CPU logic description is given in the following paragraphs:

2.2 Signal Mnemonics

The signal names used are mnemonics for the function of the signals. The following letters have a special significance when used with the mnemonics:

- F indicates a flip-flop output.
- N suffix indicates an active-low signal (0V=1, 5V=0).
- Y indicates the copying of information.
- Z0, Z1 is used after a flip-flop mnemonic to indicate (respectively) setting to 0 or setting to 1 of the flip-flop.

A complete list of signals is provided at the end of this section (Table 2-14).

2.3 Logic Conventions

In the following logic descriptions, the suffix N indicates only the electrical level of the named signal (NAMEN is 0v when active and NAME is +5v when active). The logic state of the signal is indicated either by saying "active NAME," "inactive NAME," "reset NAME," etc., or by the bar (NAME, $\overline{\text{NAME}}$).

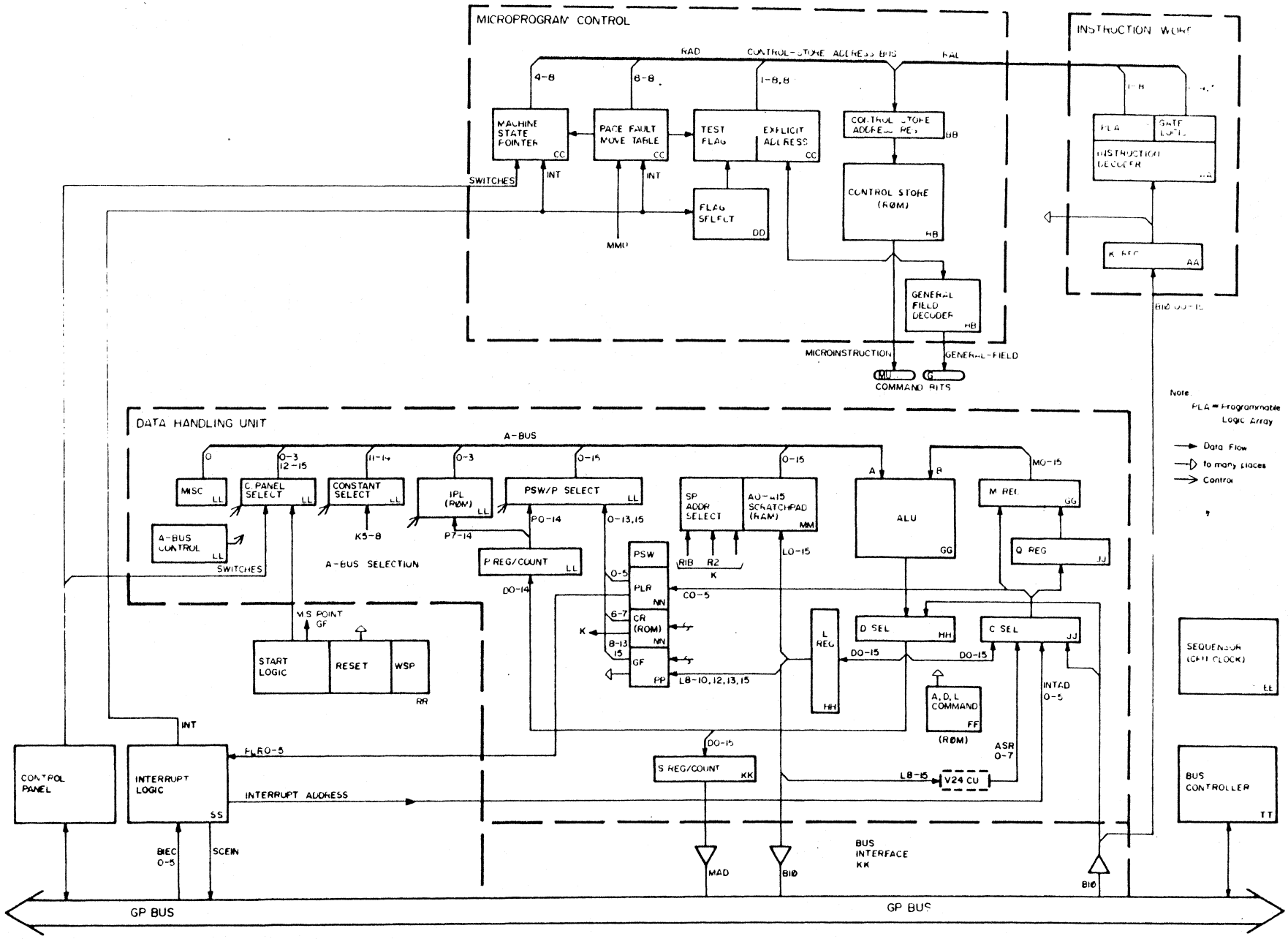
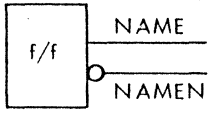


Figure 2-1 P856/857 CPU Block Diagram

Where command bits are used to form a control code, their state may be shown by the equation sign: μBIT0,1,2 = 001. A logic signal is in its True logic state when at the level specified by its name: NAME is True when high (+5v) and NAMEN is True when low (0v). Some examples are:



NAME Active high (+5v) when f/f is set)

NAMEN Active low (0v when f/f is set)

Signals in True logic state	Signals in False logic state
NAME, NAMEN "active NAME," "active NAMEN" μBIT2 = 1, μBIT2N = 1	$\overline{\text{NAME}}$, $\overline{\text{NAMEN}}$ "inactive NAME," "inactive NAMEN" μBIT2 = 0, μBIT2N = 0

2.4 GP BUS

The 57-line General Purpose Bus comprises the following signals:

Control	BUSRN SPYC OKO/OKI MSN BSYN
Timing	TMRN TMPN TMEN TRMN TPMN
Data	BIO00-15N
Address	MAD00-15,64,128
Misc	ACN BIEC0-5 CHA CLEARN PWFN RSLN SCEIN WRITE

2.5 Control Lines

- BUSRN - Bus Request, from master to CPU (bus controller); remains active (low) while master is requesting control of the Bus.
- SPYC - Scan Priority Chain, CPU (bus controller) response to BUSRN; it warns the masters to prepare for the selection of a new master of the bus. SPYC is active low.
- OKO - from CPU (bus controller) to the master with the highest bus priority. If this master does not require the bus, it passes OKO on to the next lower-priority master. If a master requires the bus, it blocks OKO and generates MSN. (The order of priority of the masters is determined by hard wiring at installation time.)
- OKI - is the signal name of OKO at the input of each master.
- MSN - is the Master Selected, generated by the master which accepted OKO to take control of the Bus.
- BSYN - Bus Busy, from the CPU or any other master which has control of the Bus, when an exchange is in progress.

2.6 Timing Signals

- TMRN - from master to register or memory; validates the BIO and MAD lines and controls the exchange timing.
- TMPN - from master to peripheral CU; initializes the CU exchange and validates the CU address on the Bus.
- TMEN - from master to external register; validates the register addresses and the data, and controls the exchange timing.
- TRMN - from register or memory to master, in response to TMEN or TMRN when the slave is ready for the transfer; also terminates the exchange.
- TPMN - from peripheral CU to master, in response to TMPN to validate the response; also terminates the exchange.

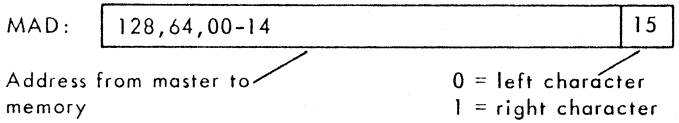
2.7 Data Lines

- BIO00-15 handle both input and output data between all system elements on the GP Bus.

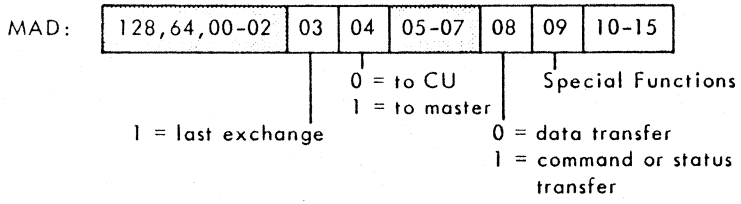
2.8 Address Lines

- MAD128,64,00-15 are the Bus address lines; 128 is the most-significant bit and 15 is the least-significant bit. The meaning of the MAD lines depends on the type of exchange, as follows:

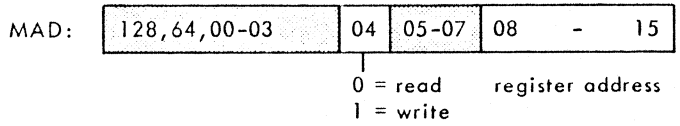
Master←→Memory (TMRN time)



Master←→CU (TMPN time)



Master←→External Register (TMEN time)



Note: Shaded parts not sent on Bus.

2.9 Miscellaneous Lines

- ACN - Accept, from the addressed CU. The CU accepts the command from the master.
- SCEIN — Scan External Interrupts from the CPU: A 2μsec signal sent at the end of every instruction, if the previous SCEIN is finished. After each SCEIN, the CPU compares the BIEC0-5 code with the level of the running program to determine if a program interrupt is required.
- BIEC0-5 - Bus Interrupt Encoded is the priority level of the highest-priority interrupt request pending from an external rack, at SCEIN time.
- CHA - Character, from master to memory indicates exchange is by character (CHA=1) or by word (CHA=0).
- CLEARN - General clear (reset) signal from CPU to all system elements, for initialisation.
- PWFN - Power Failure from the CPU sequences power off at power-failure and switching-off time without losing data, and controls power-on/auto-restart.
- RSLN - Reset Line from the CPU is the power restoration/validation signal.
- WRITE - From master to memory indicates exchange is write (line active) or read (line inactive).

2.10 BUS CONTROLLER

The Bus Controller logic (Figure 2-8TT) regulates access of all system masters to the GP Bus. When the Bus is free, the Controller scans the masters for a Bus-access request.

2.11 Bus Access

Any master requiring Bus access (Figure 2-2) may generate the Bus Request signal BUSRN if MSN is inactive, indicating no other master is being selected. The CPU Bus Controller logic receives BUSRN and, in response, generates Scan Priority Chain (SPYC), which is active low. If the Power Failure signal PWFN is inactive, BUSR sets the OKVAL flip-flop, and OKO is put onto the GP Bus along with SPYC. If PWFN is active, the CPU takes control of the Bus and does not generate OKO.

2.12 The highest-priority master (first master in the series) with a Bus Request blocks OKI and generates Master Selected (MSN). This highest-priority master which has just been selected may not have been the first to generate BUSRN. Active MSN blocks further generation of BUSRN by any master.

2.13 The Bus may be busy with an exchange (BSYN) while a new master is being selected. Once BSYN drops, the newly-selected master takes control of the Bus by generating BSYN and dropping MSN. With MSN inactive, any other master requiring Bus access may generate BUSRN and initiate a new selection sequence.

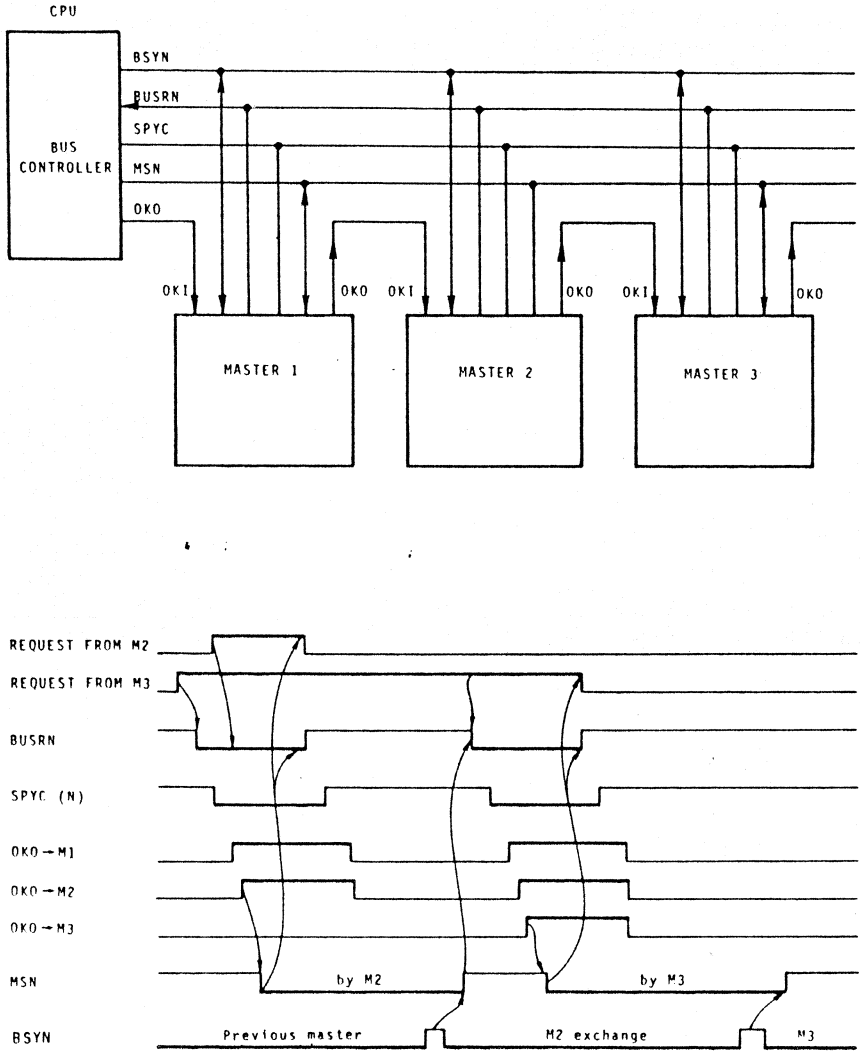


Figure 2-2 Bus Control Block/Timing Diagram

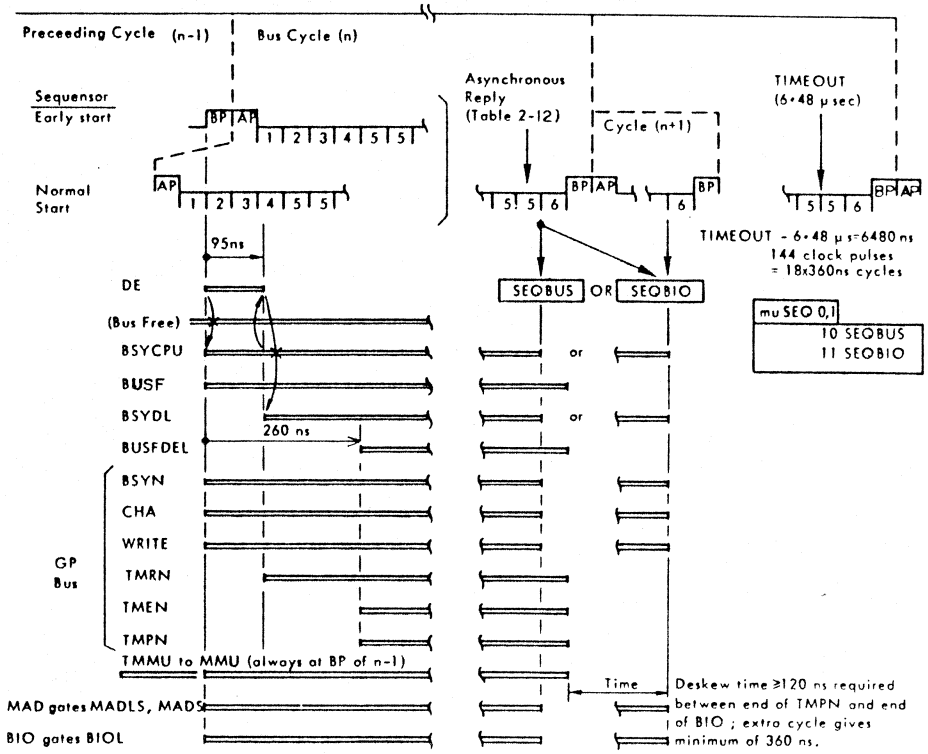


Figure 2-3 CPU Bus Control Timing

2.14 CPU Bus Control

The CPU has lowest priority for Bus access (except for power failure). The Bus-free condition, no other master requesting or using the Bus, is $\overline{BUSRN}$ $\overline{MSN}$.$\overline{BSYN}$.$\overline{TRMN}$.$\overline{TPMN}$. Any of these signals will inhibit BSYZ1N and prevent setting BSYCPU. The CPU takes control of the Bus under microprogram control when μSEQ0,1 = 1x (Sequensor cycles SEQBUS [10] or SEQBIO [11]).

2.15 (Figures 2-3, 2-8TT). If a specific microcycle (n-1) is always followed by a Bus microcycle (n), the Bus access is started early, at BP of the preceeding microcycle (n-1). This reduces the Bus cycle by 135ns if the preceeding cycle is a Sequensor logic cycle; additional time is saved following other sequensor cycles. The early Bus access is initiated by microinstruction-bit μBSR and BP setting the DE flip-flop (if there is no MMU page fault, MFAULTN/PAFN). When not started early, the Bus access is initiated at T2 of the Sequensor Bus cycle: T2 and μSEQ0 set the DE flip-flop if the early-start signal MUBURSRFN is inactive.

2.16 The DE output sets BSYCPU with signal BSYZ1N, if the Bus is free. BSYCPU in turn sets the BUSF flip-flop. If BSYCPU is set, DE resets itself after a 95ns delay. When DE drops, the BSYDL signal is activated; BSYDL and μSEQ0 = 1 select the Sequensor operating cycles for Bus transfers (Table 2-12). BSYCPU also provides the following Bus gating:

- BYSN activated onto the Bus.
- Exchange-parameters CHA and WRITE gated onto the Bus: the CHA and WRITE data are always loaded into the Bus Controller from the microprogram control store at BP of the preceeding cycle (n-1).
- Bus timing signal TMRN, TMEN, or TMPN gated onto the Bus: the conditions for these signals (Table 2-1) are set into the Bus Controller at BP of the preceeding cycle.
- MADS, MADLS gated to the Bus interface logic for gating the MAD lines onto the Bus.
- BIOL gated to the Bus interface logic for gating the BIO lines onto the Bus.

Table 2-1 Bus Timing Signals

Operation	Microinst	Stored at BP	GP Bus Signal	Reply
CPU Exchange Ext. Reg/CU/Memory				
External Register	GBTMEN	TMEF	TMEN	TRMN
CU	GBTMPN	TMPF	TMPN	TPMN
Memory	μTMRN	TMRF	TMRN	TRMN
	GBCP + ($\overline{FU}$ · $\overline{GBEX}$) + MMUABS			
Mem. via MMU translation	μTMRN	TMMU	TMRN from MMU	TRMN or MFAULTN
	$\overline{GBCP}$.(FU + GBEX).$\overline{MMUABS}$			
MMU Operations				
Table Load	GBTMFN	TMMN		DONEMN
Table Store	GBOMN .GCRFNUN	BOMFN		DONEMN
Load P'	GFETCH			
FPP Operations				
Load K'	GFETCH			
Store Operand	GBOFN. GCRFNUN	BOFFN		
Load Operand	GBTMMN	TMFN		DONEFN
Process	GFLOT	FLOACT		DONEFN

P857 only

2.17 Bus Addressing (MAD Lines)

The control of the Bus MAD lines is determined by the MADLCPUN and MADCPUN signals which control MADLS and MADS to the MAD output gates. The gating signal to both MADLS and MADS is BSYCPU (preceeding paragraph). The conditioning logic for setting MADLCPUN and MADCPUN produces the Boolean equations:

for MADLS: ($\overline{GBCP}$+CPBABS).(GBCP+($\overline{GBEX}$.$\overline{FU}$)+MMUABS) = within page

P857 only

for MADS : ($\overline{GBCP}$+CPBABS) = page address

- If GBCP: the control panel validates the MAD lines; the CPU has

control only if control-panel B-half is absent (CPBABS).

- If $\overline{GBCP}$ (P856): the CPU validates MAD128,64,00-15 with MADLS and MADS.
- If $\overline{GBCP}$ (P857): the CPU validates MAD128,64,00-03 with MADS; the MMU validates the MAD04-15 lines if GBEX or FU, and the MMU option is present; the CPU has control only if the MMU is absent or if GBEX and FU.

The following diagram is a resume of the MAD line validation control for memory addressing:

	MAD	128,64,00-03	04	15	
BSYCPU.$\overline{GBCP}$.$\overline{GBEX}$.$\overline{FU}$		CPU			
BSYCPU.GBCP.$\overline{CPBABS}$		CONTROL PANEL			
BSYCPU.GBCP.CPBABS		CPU			
BSYCPU.$\overline{GBCP}$.(GBEX+FU).$\overline{MMUABS}$		CPU	MMU		P857 only
BSYCPU.$\overline{GBCP}$.(GBEX+FU).MMUABS		CPU			

2.18 For memory addressing under CPU control, the S register provides the memory address to the Bus MAD lines, according to the preceeding diagram. For CU or External Register addressing, the CPU logic provides the address via the D-selector and the S-register to the MAD lines.

2.19 Bus Data (BIO Lines)

The Bus data from the CPU are gated onto the BIO lines by the BIOL signal from the Bus Controller. BIOL is generated by microinstruction bit μBIOL, which is loaded at BP of the preceeding microcycle (n-1) as BIOELN.

2.20 Bus Timing Signals

The Bus timing signals (Table 2-1) TMRN, TMEN, TMPN are generated by the master that has control of the Bus. For CPU Bus control, one of these signals is generated by the Bus Controller during the Sequensor Bus cycle (SEQBUS or SEQBIO). For MMU or FPP operation (P857), the Bus Controller sends a special timing signal directly to the MMU or FPP, and this external unit generates the Bus timing signal. The CPU waits at Sequensor clock-pulse T5 until the necessary reply is received to end the Bus cycle. The reply (Table 2-5) is either the Bus response TRMN, TPMN to the CPU or the special reply signal directly from the MMU or FPP to the CPU.

2.21 When the required ending condition is satisfied, including reply received, the Sequensor steps to clock T6. For SEQBUS (μSEQ0,$\overline{1}$) operations, BSYCPU is reset by the T6 and μSEQ1 = 0. The inactive BSYCPU ends the Bus control and data lines BSYN, CHA, WRITE, MAD, and BIO. The timing signals end 45ns later, being reset directly by the BP clock. For SEQBIO (μSEQ0,1) operations, the BIO lines must be prolonged at least 120ns to satisfy CIO timing requirements. In this case, μSEQ1 = 1 and BSYCPU is not reset. The Bus control and data lines, including BIO, are continued into the next Sequensor cycle (n+1) while the timing signal TMPN is reset normally by BP at the end of the BUS cycle. The microcycle after the Bus cycle (n+1) will have μSEQ1 = 0 so that BSYCPU is reset at T6 of that cycle.

2.22 Timeout

A timeout circuit (Figure 2-8TT) is used to release the Bus and set the condition register to 3 (CR = 11_2) if the addressed slave doesn't respond within 6.48usec. The basic clock for timeout is derived from the 45ns OSC signal (Figure 2-8EE) divided-by-2 by the OSC90 (90ns), and then divided-by-9 by the TC810 counter. The counter initially (following RSLBN -- 0) counts from 0 to 15; each TC810 output pulse (at count 15) then resets the counter to 7 so that the counting cycles continuously from 7 through 15. The resultant TC810 pulse (810ns period) drives the Timeout counter (Figure 2-8TT).

2.23 Timeout is held reset by the four inactive Bus-Control signals to the MR input. At the beginning of a bus cycle, (Figure 2-3), BSYCPUN or any master command goes active and the counter begins counting the TC810 input pulses. During the bus cycle, one of the TM... timing signals will also be activated. When the addressed slave responds, the bus cycle is terminated and the timing signal TM... and signal BSYCPUN are deactivated, and the Timeout counter is again reset. If there is no response by the time eight TC810 pulses have been counted

(6480ns), the counter produces TIMEOUT. TIMEOUT activates the required response signal on the Bus (TPMN or TRMN) to stop the exchange and unblock the system, generates sequensor pulse T6 to end the bus cycle, and sets CR bit 0.

2.24 MICROPROGRAM CONTROL

Each CPU instruction or operating sequence (paragraph 1.67) is controlled by a selection of microinstruction control words stored in a read only memory (Control ROM). The different microinstruction control words are accessed by the instructions or sequences (at each AP clock pulse time). The words are addressed partly by the instruction content (K register) and partly by the currently-accessed control word. Various CPU or system conditions may also modify or change the selection of the next microinstruction control word.

2.25 The microinstruction control words are used directly by the CPU logic as command bits (μ...). Each 48-bit microinstruction is divided into 14 command fields (Table 2-2). The five-bit general-field section of the control word is decoded to produce 28 general field command bits for further microinstruction control. Both the micro-command bits (μ...) and the general-field command bits (G...), listed in Table 2-3, are used by the CPU logic as direct command bits. These command bits are shown on the logic diagram (Figure 2-8BB) with their destinations listed; they are shown throughout the logic as command inputs, and identified by being enclosed in boxes.

Table 2-2 Microinstruction Command Bits

	Field	Bit	CPU section controlled by the command field
Next Word Control	μSNA 0-1	0-1	Select Source of Next Address
	μNA 0-8N	2-10	Next Address, Explicit
Data Path Control	μA 0-4	11-15	A-Bus Selector
	μADL 0-4	16-20	ALU, D, L Command Decoder
	μC 0-1	21-22	C Multiplexer
	μMLOAD, MSEL	23-24	M Register
	μQ 0-1	25-26	Q Register
	μS 0-1	27-28	S Register
	μP 0-1	29-30	P Register
	μCT	31	CT Counter: loops, shifts
	μSEQ 0-1	35-36	Sequensor (CPU clock). Bus Controller
	μTMRN, BIOL, WRITE, BUSR	32-34 37	Bus Controller
	μCR 0-2	43-45	Condition Register
	(not used)	46-47	
	μGP 0-4	38-42	GENERAL FIELD SELECTION

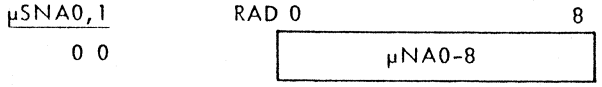
2.26 Microinstruction Addressing

The Next-Address mode for the microinstruction word determines which of four types of microprogram addressing is to be used. The mode is selected by bits μSNA0 and μSNA1 from the current microinstruction word, as follows:

μSNA 0 1	Mode	Function
0 0	Explicit	Explicit address is μNA0-8.
0 1	Flag	Flag from execution-pointer tests (selected by μNA6-8) sets RAD8; μNA0-7 to RAD0-7.
1 0	Instruction Word (PLA)	Instruction word (K-reg, decoder) provides address RAD1-8; μNA7 modifies the decoder for fetch or execution.
1 1	Machine-State	The machine-state pointer provides address RAD4-8; μNA0-3 to RAD0-3.
x x	Move Table/Fault: an interrupt or a page fault during a Move Table instruction force a special microinstruction address with bits RAD6-8.	

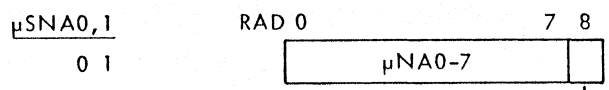
The Next-Address mode selectes a set of open-collector gates onto the control-store address bus (Figures 2-8AA,CC). This control-store address is loaded into the RA register by the AP clock pulse.

2.27 Explicit Address. The next address is explicit in the current micro-instruction μNA0-8 field.



The explicit-address gates (Figure 2-8CC) invert the μNA0N-8N onto the RAD0-8 lines. All eight gates (and the flag gate) are blocked (forced high) by NARDT during a Move Table/fault. Other gates are blocked selectively by next-address modes which use some of the μNA bits.

2.28 Flag. The next address is explicit in the current microinstruction μNA0-7 field, with the least significant bit being selected by the Flag test. Any one of eight different execution-pointer tests can be performed during Flag mode, as selected by the bits μNA6-8.



μNA6,7,8N	Flag	Use
0 0 0	Q00N	Display, C.Panel, IPL, Trap, End of TL-TS (P857), Execute, DIV correction.
0 0 1	IRN	Move Jump.
0 1 0	PM1	End of ML, MS, Move
0 1 1	K08	Shifts, Move
1 0 0	FNU	C.Panel test, IPL, Wait-C2, Trap in EX-T2.
1 0 1	NORM	End of normalized shifts.
1 1 0	DIV	Remainder correction.
1 1 1	FU15R2	Privileged test; Trap for SLN, SRN; Move.

The Flag mode uses explicit-address gates 0 to 7 (Figure 2-8CC) onto the RAD0-7 lines. The eighth explicit gate is blocked by NAEXPL while the flag gate is enabled by NAFLG. The signal FLAGN sets bit RAD8. FLAGN is selected by a type 74151A eight-input multiplexer (Figure 2-8DD) which is controlled by μNA6N,7N,8N. The eight tests selected for the FLAGN bit are described in the following paragraphs.

2.29 Flag Q00N is used as a general test condition for various commands and instruction.

2.30 Flag IRN is the interrupt request. During a page fault or an interruption of a Move-instruction/execution, flag IR enables the separation of the exit subroutine. If the Move instruction was interrupted, the last exchange was executed. These subroutines save the parameters necessary for resuming the Move execution.

2.31 Flag PM1 is used to detect the last word transfer during a Multiple Load or Store (ML,MS) or Move instruction. PM1 is taken from the un-used (most-significant) bit position of the P counter when it is used as an auxiliary

counter. The P counter is normally used as a 14-bit counter for program aadresses. When used as an auxiliary counter, PM1 is set by the first decrementing clock after P0-14 has counted down to zero.

2.32 Flag K08 is taken directly from the instruction word to differentiate between different types of shift and Move instructions, as follows:

Shifts: K08-0 = SLA, SLL, SRA, DLA, DRA
K08-1 = SLN, SLC, SRN, DLN, DRN

Move: K08-0 = MVF, MVB
K08-1 = MVSU, MVUS

2.33 Flag FNU stores the zero contents of the ALU. FNU is stored in one bit of a four-bit register (74175). The other three bits of this register have no relationship with FNU.

2.34 Flag NORM defines the end of a shift normalize execution. The end-of-shift signal is GOSH (Figure 2-8DD) which is controlled by a 74151A chip. The inputs to the multiplexer chip are held at 1 or 0 (+5v or 0v) so that the selection and enable inputs provide direct control of GOSH as follows:
Q15+(L00 ⊕ L01)+P09 = $\overline{GOSH}$ = NORM

- Shift Right Normalize ends when Q15 sets. The active Q15N selects the low 74151A inputs 10-14 to generate a low GOSH. The P counter is used as an auxiliary counter to count 32 shifts (the program address is saved). If P09 sets before Q15, it means the constant to shift is equal to zero and GOSH goes low. L0⊕L1 never sets.
- Shift Left Normalize ends when L00⊕L01 is true. Since Q15N is not used (held high), L00,01 select 74151A inputs 14-17 as an EXclusive-OR, and GOSH is low when L00⊕L01 is true. The P counter is used in the same manner as in Shift Right Normalize.
- Shift without normalizing. The number of shifts to be executed is contained in K11 - K15. This number is loaded in complement into the Scratchpad CT counter. The counter is incremented to 31 in a single microinstruction (CT+1, Repeat), and the shifting is ended when the microinstruction is finished.

2.35 Flag DIV enables the remainder correction according to test DIVA or DIVB, selected by μQ1. Test DIVA (μQ1) is true if the remainder sign is opposite to the dividend sign. Test DIVB (μQ1N) is true if both the remainder and dividend are <0, but the absolute remainder value is greater than the absolute divisor value. The select inputs and data inputs of a 74151A multiplexer chip are used together to generate the FLAGDIV signal when either test is true.

- DIVA: μQ1 FSIGDIV FSIG (input 14)
  FSIGDIV FNU (input 16,17)
- DIVB: μQ1 FSIGDIV FSIG FNUN (input 13)

2.36 Flag FU15R2 tests for System-Mode reserved instructions which can modify the stack pointer contents. When the stack pointer is indicated (R2E15) and User Mode is set (FU), the active FU15R2N signal is inverted to a high FLAGN, and the bit RAD8 = 0 to cause a trap.

2.37 Instruction Word. The next address is decoded directly from the instruction word.

μSNA0,1	RAD 0		8
1 0	0	K-reg decoding	

This is used as the first address of an instruction microprogram. The instruction-word addressing mode operates in one of four sub-modes, selected by the signals PLA0, PLA1 :

PLA0,1	Sub-Mode	Purpose
0 0	Inhibit	Instruction-word outputs held inactive (high).
1 0	Add Master	Fetch operand for types T1-T7; execute for type T8; Trap if illegal.
1 1	Add User	Fetch operand for types T1-T7; execute for type T8; Trap if privileged.
0 1	Execution	Used for first microinstruction word after the fetch-operand routine.

The PLA selection logic is shown on Figure 2-8AA. The sub-mode inhibit is set by the inactive validate signal (PLAVALN high). PLAVALN is held high

by μSNA0 = 0 (Explicit mode or Flag mode) or an active PAFN. PLAVALN is activated by μSNA0 = 1 (Instruction-Word or Machine-State modes). The conditioning for PLA is as follows:

	μSNA 0,1	PLAVALN	FU μNA7	PLA 0,1	Sub-Mode
	0 0, 0 1	h		0 0	Inhibit
Explicit	1 0	L	0 0	1 0	Add Master
Implicit	1 1		1 0	1 1	Add User
	.RADETPLN		- 1	0 1	Execution

Microprogram bit μNA7 selects a fetch sub-mode (Add Master or User) or the execution sub-mode. If fetch is selected, the FU signal indicates either User mode (FU = 1) or Master mode (FU = 0). For all three of the active sub-modes, the instruction-word addressing may be explicit (μSNA1 = 0) or implicit (μSNA1 = 1). The explicit addressing is used for instruction execution and the execution pointers. The implicit addressing is part of the machine-state-pointer control of the microprogram.

2.38 Instruction-word addressing of the microinstruction store is controlled by the instruction-word decoder (Figure 2-8AA). The decoding is done mainly by a programmable logic array (PLA) which provides address codes for 96 different input combinations. In many cases, the output address codes are the same for various different input combinations. The PLA decoding is shown in Table 2-6, Instruction Decoder. Some instruction-word decoding is done by logic gates operating in parallel with the PLA.

2.39 The external instruction-word logic gates are used for an ineffective branch (NOJUMP) or, with P857, a floating-point instruction without an attached FPP (NOFLO). For both instructions, PLA0 is high, and the external gates for RAD1-4 are enabled; also, either NOFLON or NOJUMPN generates NACND which activates the four gates to force RAD1 through 4 low. For No Jump, active NOJUMPN generates NACNDAD; RAD7 is selected by DWIN (double-word) and address /001 or /002 is selected. For No FPP, inactive NOJUMPN blocks NACNDAD; RAD7 is forced high and address /007 is selected. Bit 8 is PLA selected.

		0	1	2	3	4	5	6	7	8	
No Jump	RAD	0	0	0	0	0	0	0	0	1	/001
									1	0	/002
No FFP	RAD	0	1	2	3	4	5	6	7	8	
		0	0	0	0	0	0	0	1	1	/003

2.40 Machine-State Pointer. The Next Address is determined by machine-state pointers, such as RUNF and control-panel switches. (See also Figure 1-9 for general flow). The machine-state pointer logic is shown on Figure 2-8CC. The instruction-word decoder (Figure 2-8AA) is also used for one sub-mode of the machine-state pointer microprogram control. There are four sub-modes of machine-state pointer address selection, as follows:

Instruction			RAD	0	1						8	
				0								
				PLA Decoder								
Interrupt	RUNF.IR.$\overline{\text{PUP}}$.		RAD	0	1	2	3	4	5	6	7	8
(RUNF.PUP		KRY		0	0	0	0	1	0	1	0	1 (/015)
=RADET6)		$\overline{\text{KRY}}$		0	0	0	0	1	0	1	0	0 (/014)
C.Panel	RUNF.PUP		RAD	0	1	2	3	4	5	6	7	8
				0	0	0	0	1	0	0	0	0 (/010)
Program End	$\overline{\text{RUNF}}$.$\overline{\text{IR}}$.$\overline{\text{PUP}}$.		RAD	0	1	2	3	4	5	6	7	8
(RUNF.μNA8		KRY		0	0	0	0	0	0	1	0	1 (/005)
=RADET6)		$\overline{\text{KRY}}$		0	0	0	0	0	0	1	0	0 (/004)

In all cases, the control-panel TEST key will set RAD bit 0 to 1, via ETATEST and VALNA0 on Figure 2-8CC. The Instruction sub-mode generates the signal RADETPLN (Figure 2-8CC) which activates the instruction-word decoder PLA via signal PLAVALN on sheet AA. Refer to paragraph 2.37. The Interrupt sub-mode selects address /014 or /015 for the interrupt routines. The Control-Panel sub-mode selects address /010 if any of the control-panel command signals are active (PUP signal active). The control-panel command switches operate through the A-bus of the Data Handling logic. The Program-End sub-mode selects a branch to address /004 or /005.

2.41 Move Table/Fault (P857). An interrupt or a page fault during a Move Table instruction force the RAD bits to a special control-store address, as follows:

	Address	RAD	0	1	2	3	4	5	6	7	8
Interrupt. MVB read	1F8		1	1	1	1	1	1	0	0	0
MVB write	1F9		1	1	1	1	1	1	0	0	1
MVF read	1FA		1	1	1	1	1	1	0	1	0
MVF write	1FB		1	1	1	1	1	1	0	1	1
Page Fault	1FF		1	1	1	1	1	1	1	1	1

The move table/fault logic is shown on Figure 2-8CC. Either the page fault (PAFN) or the interrupt during Move Table (MOVEIRN) cause the signal NARDT. NARDT blocks all the control-store addressing gates on the machine-state-pointer, explicit-address, and test-flag logic, which puts the address bits high. The move table/fault logic then forces bits RAD6-8 low according to its control inputs to obtain the address code shown in the above table.

2.42 RA -- Microinstruction Address Register

The 9-bit RA register holds the address of a single 48-bit microinstruction word. This is actually a 10-bit buffer register comprising one 6-bit 74s174 and one 4-bit 74s175. The tenth bit position, however, is used to store the command-bit-derived signal FETCH, which is re-generated as FTDEL.

2.43 The 9-bit address code RAD0-8 is loaded from the control-store address bus at the leading-edge of clock pulse AP. The address code is produced by the Instruction Word logic or the Microprogram Control logic; the source is selected by gating (from the source selector) within that logic. The reset signal RSLBN resets the RA register to all zeros so that control-store address 000 is selected by the RA output. The signal RSLBN is derived from the GP-Bus reset-line signal RSLN, via RSLF.

2.44 Microinstruction Store (Control ROM)

This section is composed of six type 8205 read only memory (ROM) ICs. Each IC contains 512 eight-bit words which are accessed by nine addressing inputs. Addressing from the RA register is applied in parallel to the six ICs to obtain 512 48-bit words of store.

2.45 The enabling inputs of the control ROM are tied high; the outputs thus display continuously the content of whatever word is addressed by the RA register. When RA is reset by RSLN, the control-ROM address zero is selected (Idle state). A listing of all control-ROM microinstructions is provided in Table 2-4B. The binary contents of the control ROM are provided in Table 2-5.

2.46 Microinstruction Decoding

Two groups of command bits (Table 2-2) are used by the CPU logic as direct command bits. The micro-command bits (μ...) are the actual bit contents of the currently-addressed micro-instruction word. The general-field section of these bits (μGP0-4) are decoded to produce a further 28 command bits (G...).

2.47 The general-field command bits (Figure 2-8BB) are decoded by four type 74s138 ICs. The signals μGP4,3,2 are connected in parallel to the A, B, C inputs. The gating inputs G1, G2A, G2B are connected as follows:

Bits:	1-7	9-15	16-23	24-29
G1	+5V	μGP1	μGP0	μGP0
G2A/	μGP0	μGP0	0V	$\overline{\mu GP1}$
G2B/	μGP1	BPN	μGP1	0V

The three gate inputs must all be active (G1-high; G2A, B-low) to enable the three A, B, C inputs. The resultant output for the different input combinations are listed in Table 2-3. Seven of the general-field commands are valid during BP for use as set/reset commands. Ten other general-field commands are stored at BP time and updated on the following BP; these are used as parameters for next-cycle exchange.

Table 2-3a General Field Command Bit Codes

µGP 01234	Command Bit	Clocked by BP	Stored on BP	Function	Application
00000	---				
00001	GIDLEN	--	--	Resynchro. Sequensor	Display, Tests.
00010	GCTLDN	--	--	Load Counter	Shift, DAR, DSR.
00011	GCRDSRN	--	--	Set OVF if Divide Error and DOOD	Shift right, Test Divide.
00100	GCRFNUN	--	--	Store OALU in FNU	IPL, PUP, Arith. Oper.
00101	GCRVMLN	--	--	Set CR if OVF; Branch for ML.	ML, Divide correction, Shift LA.
00110	GCSELN	--	--	ASR or INTAD on sel.C; data Q15	DLL, DLC, INR, Interrupt.
00111	GMOVEN	--	--	Branch during Move	Move read/write cycles.
01000	---				
01001	GFSYSN	Ys	--	Reset ENBF, ARF, PAF, FU.	System operations: INT, IPL, PAF, etc.
01010	GFENBN	Ys	--	Set ENBF	RTN with R2=15.
01011	GFSTOV	Ys	--	Allows set PIF if Stack OVF.	Update A15.
01100	GFPLR/ CLPLR	Ys	--	Loads PLR,FU by C	INT, AR, RTN Master
01101	GFRZO	Ys	--	Reset RUNF	Control-panel operations
01110	GFKYZON	Ys	--	Reset K Ready	INT, PAF, AR, LR, RR
01111	GCRVZON	Ys	--	Reset OVF; Divided Sign Store	Shift LA, DIV.
10000	GBCHN	--	Ys	Character Mode	Character instructions.
10001	GBCPN	--	Ys	C.Panel-B memory address	LM,RM.
10010	GBEXN	--	--	MMU translation to System Mode	EL,ES,MVUS,MVSU.
10011	GBOKN	--	Ys	(keys) on BIO	IPL, C.Panel, Tests.
10100	GBOFN	--	Ys	(FPP) on BIO	FPP store, FIX.
10101	GBOMN	--	Ys	(MMU) on BIO	TS, PAF.
10110	GBTMEN	--	Ys	Ext. Register Cmnd.	RER, WER.
10111	GBTMPN	--	Ys	Prog. Channel Cmnd.	I/O instructions.
11000	GBTMMN	--	Ys	MMU command	TL
11001	GBTMFN	--	Ys	FPP command	FL, FO, FOS.
11010	GFLOTN	--	Ys	FPP activation	Wait for FPP execution.
11011	GAEXLN	--	--	Execute double word	Trap for EX, MV, 15R2, OPC=15.
11100	GFETCHN	--	--	Load K; set CT to 16	Fetch,EX,LR,RR,Tests.
11101	GMULTIN	--	--	D selection; OVF set for Multi	Last cycle of Multi.
11110	---				
11111	---				

Ys = Yes

Table 2-3b contd.

```
* REGISTRE M
*
MYC     EQU     2
MYQ     EQU     3
*
* REGISTRE Q
*
SRQ     EQU     2
SLQ     EQU     1
QYC     EQU     3
*
* COMPTEUR S
*
SYD     EQU     1
SM2     EQU     3
SP2     EQU     2
*
* COMPTEUR P
*
PYD     EQU     1
PM2     EQU     2
PP2     EQU     3
*
*COMPTEUR CT
*
CTP1    EQU     1
        EJECT
*
* ECHANGE SUR LE BUS
*
RMEM    EQU     0       TMR
WMEM    EQU     3       TMR  BIO=L
RBUS    EQU     4       PAS DE TMR
WBUS    EQU     7       NO TMR   BIO=L   WRITE=1
WEXM    EQU     1       EXTRN WRITE MEMORY
*
* SEQUENSEUR
*
REPEAT  EQU     1
SEQBUS  EQU     2
SEQBIO  EQU     3       BSYZ0  IN T6 OF NEXT CYCLE
*
* DEMANDE DE BUS ANTICIPEE
*
BUSR    EQU     1
        EJECT
*
* DECODAGES DIVERS
*

BIDLE   EQU     1       LONG CYCLE IF TEST
GCTLD   EQU     2       CTYSPA PAFZO
GCRDSR  EQU     3       OVFZ1 SI ERREUR DIVI; ENTREE GAUCHE DE D
GCRENU  EQU     4       ENU Y QALU

GCRVML  EQU     5       CRZ3 SI OVF; DEROUTEMENT ML
GCSEL   EQU     6       C=ASR OU INTAD;Q15D=ALU00,K08
GMOVE   EQU     7       DEROUTEMENT EN MOVE TABLE
GFSYS   EQU     9       ENBFZ0 ARFZ0 FUZ0
GFENB   EQU     10      ENBFZ1
GFSTOV  EQU     11      PIFZ1 SI STKOV
GFPLR   EQU     12      PLR Y C; FU Y C15
GFRZ0   EQU     13      RUNFZ0
GFKYZ0  EQU     14      KRYZ0
GCRVZ0  EQU     15      OVFZ0 ; MEMO SIGNE DU DIVIDENDE
GBCH    EQU     16      MODE CARACTERE
GBCP    EQU     17      MAD=REG D ADRESSE PUPITRE B
GBEX    EQU     18      PASSER PAR MMU MEME EN MODE SYSTEME
GBOK    EQU     19      BIO = KEY
GBOF    EQU     20      BIO = FLOTTANT
GBOM    EQU     21      BIO = MMU
GBTME   EQU     22      TME
GBTMP   EQU     23      TMP
GBTMM   EQU     24      TMM
GBTMF   EQU     25      TMF
GFLOT   EQU     26      ACTIVATION DU PROCESSEUR FLOTTANT
GAEXL   EQU     27      A= SOUS EXECUTE DOUBLE MOT
GFETCH  EQU     28      CTZ16, KYBIO
GMULTI  EQU     29      INHIBITS DSHR AT 16TH PASS;ALLOWS OVF MUL
*
* REGISTRE DE CONDITION
*
CRRTN   EQU     4
CRIO    EQU     8
CRFLO   EQU     12
CRLOG   EQU     16
CRADD   EQU     20
CRSUB   EQU     24
CRCMP   EQU     28
        EJECT
BUFFER  DATA    0
```

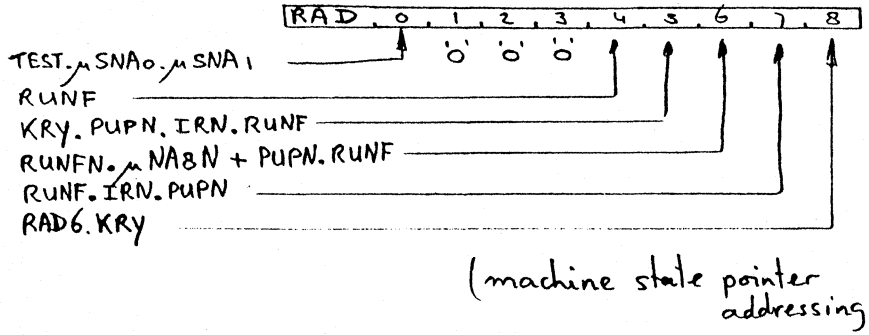


Table 2-3 General Field Command Bit Codes

μGP 01234	Command Bit	Clocked by BP	Stored on BP	Function	Application
00000	---				
00001	GIDLEN	--	--	Resynchro. Sequensor	Display, Tests.
00010	GCTLDN	--	--	Load Counter	Shift, DAR, DSR.
00011	GCRDSRN	--	--	Set OVF if Divide Error and DOOD	Shift right, Test Divide.
00100	GCRFNUN	--	--	Store OALU in FNU	IPL, PUP, Arith. Oper.
00101	GCRVMLN	--	--	Set CR if OVF; Branch for ML.	ML, Divide correction, Shift LA.
00110	GCSELN	--	--	ASR or INTAD on sel.C; data Q15	DLL, DLC, INR, Interrupt.
00111	GMOVEN	--	--	Branch during Move	Move read/write cycles.
01000	---				
01001	GFSYSN	Ys	--	Reset ENBF, ARF, PAF, FU.	System operations: INT, IPL, PAF, etc.
01010	GFENBN	Ys	--	Set ENBF	RTN with R2=15.
01011	GFSTOV	Ys	--	Allows set PIF if Stack OVF.	Update A15.
01100	GFPLR/ CLPLR	Ys	--	Loads PLR, FU by C	INT, AR, RTN Master
01101	GFRZO	Ys	--	Reset RUNF	Control-panel operations
01110	GFKYZON	Ys	--	Reset K Ready	INT, PAF, AR, LR, RR
01111	GCRVZON	Ys	--	Reset OVF; Divided Sign Store	Shift LA, DIV.
10000	GBCHN	--	Ys	Character Mode	Character instructions.
10001	GBCPN	--	Ys	C.Panel-B memory address	LM, RM.
10010	GBEXN	--	--	MMU translation to System Mode	EL, ES, MVUS, MVSU.
10011	GBOKN	--	Ys	(keys) on BIO	IPL, C.Panel, Tests.
10100	GBOFN	--	Ys	(FPP) on BIO	FPP store, FIX.
10101	GBOMN	--	Ys	(MMU) on BIO	TS, PAF.
10110	GBTMEN	--	Ys	Ext. Register Cmnd.	RER, WER.
10111	GBTMPN	--	Ys	Prog. Channel Cmnd.	I/O instructions.
11000	GBTMMN	--	Ys	MMU command	TL
11001	GBTMFN	--	Ys	FPP command	FL, FO, FOS.
11010	GFLOTN	--	Ys	FPP activation	Wait for FPP execution.
11011	GAEXLN	--	--	Execute double word	Trap for EX, MV, 15R2, OPC=15.
11100	GFETCHN	--	--	Load K; set CT to 16	Fetch, EX, LR, RR, Tests.
11101	GMULTIN	--	--	D selection; OVF set for Multi	Last cycle of Multi.
11110	---				
11111	---				

Ys = Yes

```
ADD.
000 ROM ./1E8.AR15,ALUB,CALU,MYC,QYC,...,WBUS....0                    IDLE
001 FTA ..0                                                          NO JUMP
002 ROM ./1E9......,SP2,PP2....,BUSR,.0                              INCR P
003 ROM FLAG,/ODO,AZ,ALUA,CALU..QYC,.....,GAEXL,0                    NO FLOT PROC
004 ROM FLAG,/1F8,ASYS,TWOA,CALU..QYC,.....,0                        TEST DISPLAY
005 ROM ./1F8......SM2,PM2,....,GFKYZO,0                             DECR BEFORE VISU
006 ROM ./1FF.AEP,ALUA,CALU,MYC,.....,0                              VISUA
007 ROM ./1FF..DBIO,CBIO,MYC,.....SEQBUS...0                         VISUB
008 FTA AWR1,ALUB,CRLOG                                              LD
009 ROM ./1E9...ALUB....SYD,PYD,...,BUSR,,CRLOG                      LD P
00A ROM ./16D.ASYS,ALUA,.....,WBUS,...0          RCP IN L REG.       LR OR RR
00B ROM ./1FF.ARAO,ALUA,.MYC,.....,0                                 ERRONEOUS START
00C ROM ./101,ARR1,ALUA,.....,WMEM,.BUSR,.0                          ST
00D ROM ./101,AEP,ALUA,.....,WMEM,.BUSR,.0                           ST P
00E ROM ./0E6,ATWO,ALUA,CALU,MYC,.....,0                             STD
00F ROM ./0E5,ATWO,ALUA,CALU,MYC,.....,0                             STD P
010 ROM FLAG,/1DO,ASYS,ALUA,CALU,.QYC,.....,0                        TEST AUTOREST
011 ROM ./1E9.,ALUB,...,SYD,PYD,...BUSR,.0                           AB
012 ROM FLAG,/0E0,AWAO,ALUB,.....,RBUS...GBOK,0  SAVE P TEST IF L/R R
013 ROM ./0E0,ARAO,ALUA,...SYD,PYD,.....,0          LOAD P AND S LR
014 ROM ./1D8,ATWO,TWOA,CALU,MYC,.....,0                             INT
015 ROM ./1D8,ATWO,TWOA,CALU,MYC,,PM2,....GFKYZO,0                   INT DECR
016 FTA ..0                                                          FETCH
017 ROM ETAT,/1FE.....,SEQBUS,.GIDLE,0                              VISU IDLE
018 ROM FLAG,/193,AEP,ALUA,CALU,MYC,.....,GCRVZO,0      SLASLN SAVE P
019 ROM FLAG,/158,AEP,ALUA,CALU,MYC,SLQ,.....,GCRVZO,0  DLADLN SAVE P
01A ROM FLAG,/17B,ARR1,ALUA,CALU,.QYC,.....,0                        SLL SLC
01B ROM ./0CE,AWA1,ASHL...SLQ,..CTP1,.REPEAT,.GCSEL,0                DLL DLC
01C ROM FLAG,/16B,AEP,ALUA,CALU,MYC,.....,0                          SRA SRN
01D ROM FLAG,/14B,AEP,ALUA,CALU,MYC,SLQ.....,0                       DRA DRN
01E ROM ./0DD,ARR1,ALUA,CALU,.QYC,.....,0                            SRL SRC
01F ROM ./0CE,AWA1,ASHR,..SRQ,..CTP1,.REPEAT..GCRDSR,0               DRL DRC
020 FTA AWR1,APB,CRADD                                               AD
021 ROM ./1E9,AEP,APB,...SYD,PYD,...BUSR,.CRADD                      AD P
022 ROM ./0EC,ARR2,ALUA,...SYD,....,BUSR,.0                          RT3
023 ROM ./0E8,ARR2,ALUA,...SYD,....,BUSR,.0                          RT3S
024 ROM ./101,ARR1,APB,.....,WMEM,.BUSR,.CRADD                       AD S
025 ROM ./101,AZ,APLB1,.....,WMEM,.BUSR,,CRADD                       IM
026 ROM ./077,ATWO,TWOA,CALU,MYC,.....,0                             RTN MASTER
027 ROM ./19E,AW15,AMB,...SYD,.....,GFSTOV,0                         INT UPDATE A15
028 ROM FLAG,/0DO,AZ,ALUA,CALU,.QYC,.....,GAEXL,0                    TRAP SLN
029 ROM ./0E3,ATEN,TWOA,CALU,MYC,QYC,.PYD.....0                      SLN
02A ROM ./159,ATEN,ACR,CALU,MYC,QYC,.....,0                          IPL SET
02B ROM ./145,AEP,ALUA,...SYD...RBUS,.BUSR,GBOK,0                    IPL END
02C ROM FLAG,/1D2,AWCT,DBIO,,MYQ,.SM2,PM2,CTP1,.SEQBUS...0           MLRI
020 ROM ./0DC..ALUB,...SYD,PYD,...,BUSR..0                           MLRI
02E ROM ./134...CLUR,MYC,.....,GCSEL,0                               AUTO RESTART
02F ROM FLAG,/1CO,APUP,ALUA,CALU..QYC,.....,0                        TEST IPL
030 FTA AWR1,AMB,CRSUB                                               SU
031 ROM ./1E9,AEP,AMB,...SYD,PYD,...BUSR,.CRSUB                      SU P
032 ROM SNPLA,/100,..CBIO,MYC,QYC,SP2,PP2...SEQBUS...0               RT2
033 ROM SNPLA,/100...CBIO,MYC,QYC,,PP2...SEQBUS...0                  RT2S
034 ROM ./101,ARR1,AMB,.....,WMEM,.BUSR,.CRSUB                       SU S
035 ROM FLAG,/0BC,AEN,ALUA,.....,GCRFNU,0                            C2 OR NGR
036 ROM ./077,ATWO,TWOA,CALU,MYC,.....,0                             RTN USER
037 FTA AWR1,A0B,0                                          1NH,RTN A15 AND LC END
038 ROM FLAG,/0DO,AZ,ALUA,CALU..QYC,.....,GAEXL,0                    TRAP SRN
039 ROM ./0DE,ARR1,ALUA,CALU,.QYC,.....,0                            SRN
03A ROM FLAG,/1C4,.BSHR,CALU,MYC,.....,GCRFNU,0                      WAIT IO
03B ROM ETAT,/1FF,AEP,ALUA,...SYD,.....,0                            WAIT IO
03C ROM FLAG,/1C2,AWCT,DBIO,...SP2,PM2,CTP1,.SEQBUS,,GCRVML,0        ML LOOP
030 ROM ./0DC..ALUB,...SYD,PYD,...BUSR..0                            ML END
03E ROM ./15F,ATWO,ACR,.....,PYD,.....,0                             IPL
03F ROM FLAG,/180.....SLQ,...RBUS...GBOK,0                TEST LOADM

ADD.
040 FTA AWR1,AANDB,CRLOG                                             AN
041 ROM FLAG,/1C8,APSW,AHNDB,CALU,MYC,.....,BUSR,.0 HLT,RIT,INH,RT&1S
042 ROM ./0FD...CBIO,MYC...PP2...SEQBUS...0                          RT5
043 ROM ./0F5,..CBIO,MYC,..PP2...SEQBUS...0                          RT5S
044 ROM ./101,ARR1,AANDB,.....,WMEM,.BUSR,.CRLOG                     AN S
045 ROM ./101..ZERO,.....,WMEM,.BUSR,.0                              CM
046 FTA ARR1,AANDB,CRLOG                                             TM
047 ROM ./1E9,.....,BUSR,.CRFLO                        FPP WAIT EXEC.
048 ROM FLAG,/1A6,ARA1,DIVALU,.....,GCRFNU,0  DIV TEST COR.REM.
049 ROM FLAG,/140,ARA1,AXB,CALU,MYQ,QYC,.....,0  DIV TEST QUOT.
04A ROM ./0E2,AEP,AMB,CALU,MYC,.....,0                               SLN
04B ROM FLAG,/1B5,AWR1,TWOA,.....,PP2,.....,0                        SLN LOOP
04C ROM FLAG,/1B2,ARCT,ALUA,...SP2,PM2,CTP1,WMEM,SEQBUS...0          MS LOOP
04D ROM ./1E9,.ALUB,...SYD,PYD,...BUSR,.0                            MS END
04E ROM FLAG,/1A8,.....SLQ,.....,GFRZO,0                  TEST READM
04F ROM ./172..DBIO,CBIO,MYC,....WMEM,SEQBUS,.GBCP,0         LOAD M
050 FTA AWR1,A0B,CRLOG                                               OR
051 ROM FLAG,/188,APSW,A0B,CALU,MYC,.....,0                  ENB SM0 LKM
052 ROM ./0EC..DBIO,...SYD,PP2...SEQBUS,BUSR,.0                      RT4
053 ROM ./0E8..DBIO,...SYD,PP2...SEQBUS,BUSR,.0                      RT4S
054 ROM ./101,ARR1,A0B,.....,WMEM,.BUSR..CRLOG                       OR S
055 ROM ./0A8,AWAO,BSHR,.MYQ,.....,0                                 INR
056 ROM FLAG,/1AO.....SLQ,.....,0                         TEST READST
057 ROM FLAG,/19O,ASYS,TWOA,CALU,.QYC,.....,GBCP,0           READ M
058 ROM ./1A6,AWA1,DIVALU,.....,0                  DIV  CORR.REM.
059 ROM FLAG,/140,ARA1,AXB,CALU,MYQ,QYC,.....,0    DIV  TEST QUOT.
05A ROM ./0E2,AEP,AMB,CALU,MYC,.....,0                               SRN
05B ROM FLAG,/1A5,AWR1,ASHR,,SRQ,.PP2,....GCRDSR,0                   SRN LOOP
05C ROM FLAG,/1A2,ARCT,ALUA,...SM2,PM2,CTP1,WMEM,SEQBUS...0 MSRD LOOP
05D ROM ./0BE..ALUB,.MYQ,.SYD,PYD,.....,0                    MSRD END
05E ROM ./198.....SLQ,.....,0                                        PUP
05F ROM ./1FF.APSW,ALUA,CALU,MYC,.....,0                  READ STATUS
060 FTA AWR1,AXB,CRLOG                                               XR
061 ROM ./047,APSW,ALUA,CALU,MYC..SP2,.....GFSYS,0                   INT
062 ROM ./0FC...CBIO,MYC,.....SEQBUS...0                             RT2
063 ROM ./0F4...CBIO,MYC,.....SEQBUS...0                             RT2S
064 ROM ./101,ARR1,AXB,.....,WMEM,.BUSR,.CRLOG                       XR S
065 FTA AWA2,BSHR,0                                         DLN END
066 FTA ARR1,AXB,CRLOG                                               TNM
067 ROM ./180,AWAO,ALUB,.MYQ,.....,0                                 PUP
068 ROM FLAG,/0DO,AZ,ALUA,CALU,.QYC,.....,GAEXL,0        MVF 1SR2 TRAP
069 ROM ./05F,ARR2,ALUA,CALU,.QYC,.PYD,.....,0           MVF  1SR2N
06A ROM ./0D6,AWAO,ALUB,....,PM2,.....,0                 DLNDRN END
06B ROM FLAG,/195,AWA1,ASHL...SLQ,.PP2,.....,0           DLN LOOP
06C ROM ./0E4,AWR1,TWOA,.....,CTP1,.REPEAT,..0                       SLA
060 ROM FLAG,/1D7,AWAO,ALUB,.....,0                                  SLN
06E ROM ./1FF..DBIO,CBIO,MYC,.SP2,PP2,..SEQBUS,..0       READ M PUP A
06F ROM ./1FF..DBIO,CBIO,MYC,.....,SEQBUS...0            READM  PUP B
070 ROM SNPLA,/100,AR1215,.....,GCTLD,0                  SH DSH
071 ROM ./18F,ARA2,ALUA,CALU,.QYC,.....,GFKYZO,0                     DSH
072 ROM ./1AD..DBIO,...SYD,...SEQBUS,BUSR,.0                         RT6
073 ROM ./1AC..DBIO,...SYD,...SEQBUS,BUSR,.0                         RT6S
074 FTA ARR1,ALUA,CRLOG                                              SHZERO
075 ROM ./0DC,ARA2,ALUA,.....,BUSR,GCRFNU,0                          DSHZERO
076 ROM ./092,AWA1,DSUB,.....,BUSR,.CRSUB                            DS
077 ROM ./1C5,ATWO,ALUA,CALU,MYC,.....,0                             WAIT
078 ROM ./0C7,AEP,ALUA,CALU,MYC,...,CTP1,....0                       ML
079 ROM ./150,ATWO,ASHR,CALU,.QYC,.....,GBTMM,0                      TL
07A ROM ./195,AWA1,ASHL...SLQ,.....,0                                DRN
07B ROM FLAG,/185,AWA1,ASHR,..SRQ,.PP2,....,GCRDSR,0      DRN LOOP
07C ROM ./0C5,AEP,ALUA,CALU,MYC,...,CTP1,....0                       MS
07D ROM ./148,ATWO,ASHR,CALU..QYC,...WEXM...GBOM,0                   TS
07E ROM ./0C3,AEP,ALUA,CALU,MYC,...,CTP1,....0                       MSRD
07F ROM FLAG,/1F4,.BCR,CALU,.QYC,.....,GCRFNU                        PUP

ADD.
080 ROM ./008..ALUB,...SYD,.....,0                                   CIO OTR
081 ROM ./100.....,0                                    GO TO TRAP (WMP)
082 ROM ./182,AWA2,DBIO,.....,RBUS,SEQBIO...0                        FFX LD A2
083 ROM SNPLA,/100,ARR2,ALUA,CALU,MYC,QYC,.....,0                    RT1
084 ROM ./18B,AWR1,TWOA,.....,CTP1,.REPEAT...0                       SLL
085 ROM ./18B,AWR1,ASHL...SLQ,..CTP1,.REPEAT..GCSEL,0                SLC
086 ROM ./169.....,CTP1,....,0                                       RTID
087 ROM ./179,ARR2,ALUA,CALU,.QYC,.....,GCTLD,0                      RTID
088 ROM FLAG,/0B3,.ZERO,CALU,MYC,.....,BUSR,GBTMF,0      FPP LOAD
089 ROM ./08A,AWA1,ZERO,CALU..QYC,.....,GCRVZO,0  MUL-RESET PART.PROD
08A ROM ./130,ARAO,ALUA,.....,WBUS,.BUSR,.0                EX  T1 OR T3
08B ROM FLAG,/0DO,AZ,ALUA,CALU,.QYC,.....,GAEXL,0          EX  T2 TRAP
08C ROM FLAG,/0AB,ATEN,ACR,CALU,MYC,QYC,...WEXM...GBOF,0   FPP STORE
08D ROM ./1A8.....,SEQBUS,.GFRZO,0                          LOAD M
08E ROM FLAG,/104,AEP,ALUA,...SP2,..,SEQBUS,.GCRFNU,0       IPL LOOP
08F ROM ./159..BSHR,CALU,MYC,SLQ,.....,0                    IPL LOOP
090 ROM ./1AA,ATEN,ACR,CALU,MYC,.....,0                              INR
091 ROM SNPLA,/103,AEP,ALUA,...SYD,.....,0          EX BSYZO,RESTORE S
092 ROM ./1ED,AEP,ALUA,CALU,MYC,...,RBUS,SEQBIO..GFETCH,0 K-RCP  L/RR
093 ROM SNPLA,/100,AEP,ALUA,CALU,MYC,QYC,.....,0                     RT1P
094 ROM ./18B,AWR1,ASHR,.....,CTP1,.REPEAT..GCRDSR,0                 SRA
095 ROM FLAG,/1C7,AWAO,ALUB,.....,0                                  SRN
096 ROM SNPLA,/100,ARC1,ALUA,CALU,MYC,.....,0               RT1D END
097 ROM ./169,AEP,ALUA,CALU..QYC,..CTP1,....0                RT1DP
098 ROM FLAG,/0B3,..ZERO,CALU,MYC,.....,BUSR,GBTMF,0        FPP OPER
099 ROM ./0A5,ARA2,TWOA,CALU..QYC,.....,0                    DIV
09A ROM ./095,ARA1,ALUA,.....,WBUS,.BUSR,GBTMF,0             FFL
09B ROM ./0FE,AWR2,ALUB,.....,0                          DLN,DRN END
09C ROM FLAG,/0B3,ATWO,ASHR,CALU,MYC,.....,BUSR,GBTMF,0      FPP OP/S
09D ROM ./143,AEP,ALUA,CLUR,MYC..SP2,..WMEM,SEQBUS,BUSR,GCSEL,0  INT
09E ROM ./160,AEP,ALUA,CALU,MYC,.....,GFLOT,0                FFX
09F ROM ./09B,.....,RBUS...GBOF,CRFLO                   FFX UPD CR
0A0 ROM ./105..ZERO,...SYD,.....,GFSYS,0                     IPL
0A1 ROM ./1E9,AEP,APB,...SYD,PYD,...BUSR,.0                  RF
0A2 ROM ./0E7,ATWO,ALUA,CALU,MYC,.....,0                     RT3B
0A3 ROM SNPLA,/100,ARR2,ALUA,CALU..QYC,SYD.....0             RT3C
0A4 ROM ./0DB,AWA1,ASHL...SLQ,..CTP1,.REPEAT...0             DLA
0A5 ROM FLAG,/01F,ATWO,ALUA,....,PYD.....,0                  DLN
0A6 ROM ./155,.BSHR,CALU,MYC,..PM2,.....0                IPL LOOP
0A7 ROM ./0CB,AEP,ALUA,CALU,.QYC,.....,0                     RT3BM
0A8 ROM ./0B0,.....,BUSR,GBEX,0                              EL
0A9 ROM ./0BE...CBIO,.QYC,SP2,...SEQBUS,BUSR,.0              DA
0AA ROM ./14F,.BSHR,CALU,MYC,.....,0                     IPL LOOP
0AB ROM ./152...CBIO,MYC,.SP2,PP2,..SEQBUS...0               DAK
0AC ROM ./101,ARR1,ALUA,.....,WMEM,.BUSR,GBEX,0              ES
0AD ROM ./094,AWA2,APB,CALU,MYQ,QYC,.....,0                  DA
0AE ROM ./1E9,AEP,ALUA,...SYD,...SEQBUS...0                  TL END
0AF ROM FLAG,/150,....SLQ,SP2,...SEQBUS,BUSR,GBTMM,0     TL LOOP
0B0 ROM ./140..BSHR,CALU,MYC,.....,0                     IPL LOOP
0B1 ROM ./1E9,AEP,AMB,...SYD,PYD,...BUSR,.0                  RB
0B2 ROM FLAG,/170,AIPL,APB,CALU,MYC,....WMEM,....0       IPL NEW QUART
0B3 ROM SNPLA,/100,.....PP2,.....,0                          RT2C
0B4 ROM ./0D2,AWA1,ASHR,..SRQ,..CTP1,.REPEAT..GCRDSR,0       DRA
0B5 ROM FLAG,/00F,ATWO,ALUA,....,PYD,.....,0                 DRN
0B6 ROM ./1E9,AEP,ALUA,...SYD,...SEQBUS,.0               TS END
0B7 ROM FLAG,/148,.....SLQ,SP2,..WEXM,SEQBUS,BUSR,GBOM,0 TS LOOP
0B8 ROM FLAG,/0DO,AZ,ALUA,CALU,.QYC,.....,GAEXL,0            TRAP
0B9 ROM ./0BA,..CBIO,.QYC,SP2,...SEQBUS,BUSR,.0              DS
0BA ROM ./1E9,AW15,DBIO,.....,SEQBUS,...0                IPL END
0BB ROM ./142 ..CBIO,MYC,.SP2,PP2,..SEQBUS...0               DSM
0BC ROM ./130..BSHR,...SYD,...SEQBUS,..0                     INT
0BD ROM ./08B,AWA2,AMB,CALU,MYQ,QYC,.....,0                  DS
0BE ROM ./09E,AZ,APLB1,CALU,MYC,.....,BUSR,GCRVML,CRADD  DIV COR,QUOT
0BF ROM ./1E9,AWA2,ALUB,.....,BUSR,GCRVML,CRLOG          DIV QUOT OK
```

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Table 2-4A contd.

ADD		
0C0	FTA AWR1,ALUB,0	LDK
0C1	ROM ./1E9..ALUB....SYD,PYD....BUSR.,0	LDK P
0C2	ROM ./135..BCR.........BUSR,GFPLR,0	AR PAF INT
0C3	ROM ./0EE...CBIO,MYC...PP2...SEQBUS...0	RT5C
0C4	ROM ./094F,AWA2,APB,.....,0	MVF DEST IN A2
0C5	ROM ./1E9,ARA0,ALUA,...SYD,PYD....BUSR..0	MOVE END SLN REST,P
0C6	ROM ./088,ARR1,ALUA,CALU.,QYC.....,0	CA
0C7	FTA ARR1,AMB,CRCMP	CA
0C8	ROM ./086,ARR1,ACR,CLUR,MYC.....BUSR,GBCH,0	LC
0C9	FTA AWR1,BCR,0	ECR
0CA	ROM ./1E9..DBIO...,SYD,PYD...SEQBUS,BUSR..0	AR PAF INT TRAP
0CB	ROM ./132.....GFSYS,0	AR END
0CC	ROM ./101,ARR1,ALUA.....WMEM..BUSR,GBCH,0	SC
0CD	ROM ./130..BSHR,...SYD.....GFKYZO,0	PAGE FAULT AR
0CE	ROM FLAG,/128,ARA0,APB,CLUR,MYC,SLQ.....,0 EX T&N TEST K1	
0CF	ROM ./16E...CIOR,MYC,QYC....WBUS,SEQBIO..GFETCH,0 EX LOAD K	
0D0	ROM FLAG,/0D0,AZ,ALUA,CALU..QYC.....GAEXL,0	TRAP
0D1	ROM FLAG,/0D0,AZ,ALUA,CALU..QYC.....GAEXL,0	TRAP
0D2	ROM ./125,AWR2,ALUB,.....,0	PAGE FAULT ML
0D3	ROM SNPLA,/100..DBIO,CBIO,..QYC,SYD,PP2...SEQBUS...0	RT4C
0D4	ROM FLAG,/11B,AWA2,AMB,CBIO,MYC..SYD,...SEQBUS..GMOVE,0 MVF READ	
0D5	ROM ./056,AWA1,APB,.....,0 MVF REST A1	
0D6	ROM FLAG,/120.....SLQ.....,0 EX K1 TEST K2	
0D7	ROM FLAG,/0F8..BCR,CALU..QYC.....,0 EX K1N TEST MD	
0D8	FTA ARR1,AMB,CRCMP	CW
0D9	FTA AEP,AMB,CRCMP	CWP
0DA	ROM ./124,APSW,ALUA,CALU,MYC.....GFSYS,0	PAGE FAULT
0DB	ROM ./122,AR15,ALUA,...SYD...WEXM..BUSR,GBOM,0	PAGE FAULT
0DC	ROM ./08C,ARR1,ALUA,CLUR,MYC.....BUSR,GBCH,0	CC
0DD	ROM ./11D..ALUB.,MYQ.,SM2...WMEM,SEQBUS,BUSR.,0	PAGE FAULT
0DE	ROM FLAG,/118.....SLQ.....,0 EX K1K2 TEST K3	
0DF	ROM FLAG,/0F8..BCR,CALU..QYC.....,0 EX K1K2N TEST MD	
0E0	ROM ./078..ALUB,...SYD.....,0	WER
0E1	ROM FLAG,/197,AEP,ALUA,CALU,MYC.....,0	MVF
0E2	ROM ./117,ATW0,APB,CALU,MYC..SM2...WEXM,SEQBUS,BUSR,GBOM,0 PAF	
0E3	ROM ./0ED...CBIO,MYC.....SEQBUS...0	RT7C
0E4	ROM ./057,.ALUB..MYQ...PM2,.WMEM..BUSR.,0 MVF PREP WRITE	
0E5	ROM ./057,.ALUB..MYQ...PM2,.WMEM..BUSR,GBEX,0 MVSU PREP WRITE	
0E6	ROM FLAG,/108.....SLQ.....,0 EX K1K2K3 TEST K4	
0E7	ROM FLAG,/0F8..BCR,CALU..QYC.....,0 EX K1K2K3N TEST MD	
0E8	ROM ./132,AW15,AMB,CIOR,MYC.....RBUS,SEQBIO..GFSTOV,0 PAGE FAULT	
0E9	ROM ./1E9,AEP,ALUA,...SYD....SEQBUS,BUSR.,CRRTN RTN 15R2N	
0EA	ROM ./110,ATEN,TWOA,CALU.,QYC..PM2.....0	TRAP
0EB	ROM ./073,AEP,ALUA,CBIO,MYQ,QYC,SYD....SEQBUS..GFPLR,CRRTN RTNA15	
0EC	ROM ./02E,ATW0,TWOA,CALU,MYC.....0	CF
0ED	ROM FLAG,/130,AWA0,ALUB,.....WBUS....0	EX
0EE	ROM ./068,ATW0,TWOA,CALU,MYC.....0	CF 15R1
0EF	ROM ./100,AW15,AMB...SLQ,SYD.....GFSTOV,0	TRAP
0F0	ROM ./04E,ATEN,ACR,CALU,MYC.....0	RER
0F1	ROM FLAG,/0F7,AEP,ALUA,CALU,MYC.....0	MVB
0F2	ROM ./105,APSW,ALUA...SLQ,SP2...WMEM..BUSR,GFSYS,0	TRAP
0F3	ROM ./12C..DBIO....SYD....SEQBUS,BUSR.,0	RT6C
0F4	ROM ./0EB,ARA1,ALUA....SYD.....BUSR.,0 MVB PREP 1ST A0	
0F5	ROM ./0EB,ARA1,ALUA....SYD.....BUSR,GBEX,0 MVUS PREP 1ST A0	
0F6	ROM FLAG,/0F8..BCR,CALU..QYC.....,0 EX K1K2K3K4 TEST MD	
0F7	ROM FLAG,/0D0,AZ,ALUA,CALU,.QYC.....GAEXL,0 EX 150PC TRAP	
0F8	ROM ./0C8,AEN,ALUA,CALU,MYC...PM2.....0	MLK
0F9	FTA AWR1,BINV,CRL06	C1
0FA	ROM ./104,AEP,ALUA..MYQ..SP2...WMEM,SEQBUS,BUSR..0	TRAP
0FB	ROM ./103,.ALUB....SYD....SEQBUS...0	TRAP
0FC	ROM ./135.....SM2.....BUSR.,0	TRAP
0FD	ROM ./101..BINV.....WMEM..BUSR..CRL06	C1S
0FE	ROM ./1E9,AEP,ALUA,...SYD....SEQBUS,BUSR.,0	STORE RESULT
0FF	ROM FLAG,/0D0,AZ,ALUA,CALU,.QYC.....GAEXL,0	TRAP

ADD.		
100	ROM ./03F.....GFSYS,0	VERIF MAN. PUPIT
101	ROM ./19A,ARA0,ALUA,.MYQ...PYD....BUSR..0	DLN,DRN END
102	ROM ./0EC,ARR2,APB,...SYD.....BUSR..0	RT5
103	ROM ./1A0,ARR2,APB,...SYD.....BUSR..0	RT7
104	ROM ./0D3...CBIO,MYC.....RBUS,SEQBIO...0	TMP TEST RD KEYS
105	ROM FLAG,/0D4,ARA0,ALUA.....GCRFNU,0	TEST RETURN
106	ROM FLAG,/0D0,AZ,ALUA,CALU,.QYC.....GAEXL,0 EX OPER T4T7 TRAP	
107	ROM ./066..BSHR,CALU,MYC.....0 EX OPER T1,T2,T3	
108	ROM FLAG,/0D0,AZ,ALUA,CALU..QYC.....GAEXL,0 MVB 15R2FU TRAP	
109	ROM ./04B,ARR2,ALUA,....PYD.....0 MVB 15R2FUN	
10A	ROM ./0E8,ARR2,APB,...SYD.....BUSR..0	RT5S
10B	ROM ./1AC,ARR2,APB,...SYD.....BUSR..0	RT7S
10C	ROM ./04A,ATW0,ALUA,CALU,MYC,QYC.....,0 MVB LENGTH>0	
10D	ROM ./1E9,ARA0,ALUA,...SYD,PYD....BUSR..0 MVB LENGTH=0	
10E	ROM ./1EB,ARA0,AMB,....PYD.....0 INT MOVE	
10F	ROM ./125,ATW0,TWOA,CALU,.QYC.....,0 PAF MOVE	
110	ROM ./0DF.....GFRZO,0	VERIF MAN. REG L
111	ROM SNPLA./100,ARR2,APB,CALU..QYC,SYD.....0	RT5C
112	ROM ./12C,ARR2,APB,...SYD.....BUSR,,0	RT7C
113	ROM SNPLA./100,AEP,ALUA,CBIO,MYC,QYC,SYD,...SEQBUS,,,0	RT3
114	ROM ./048,AWA2,APB,CBIO,MYC..SYD,...SEQBUS,,GMOVE,0 MVB READ	
115	ROM ./056,AWA2,APB,.....,0 MVB CORRECT A2	
116	ROM ./0AE,ATEN,ALUA,.MYC,.....GFRZO,0 TEST DLA	
117	ROM SNPLA./100...CBIO,MYC,QYC.....SEQBUS,,,0	RT3S
118	ROM ./0EC,AWR2,APB,...SYD.....BUSR,,0 RT3B UPDATE STACK	
119	ROM ./1F3,AWR2,AMB,.....GFSTOV,0	STD
11A	ROM ./1F2,AWR2,AMB,.....GFSTOV,0	STDP
11B	ROM ./1E9,ARR1,ALUA,.....BUSR,GCRVML,CRL06	SLA CR
11C	ROM FLAG,/185,ARR1,ALUA,.....,0	SLN TEST NORM
11D	ROM ./13A,AWR2,BSHR,.....,0	SLN RESULT
11E	ROM ./1EC,AW1215,DBIO,.....RBUS,SEQBIO,..0 KEYS IN (RCP) LR	
11F	ROM ./1FF,AR1215,ALUA,.MYC,.....GFKYZO,0 LOAD OR READ R	
120	ROM ./009.....RBUS...GBOK,0	VERIF MAN. REG L
121	ROM FLAG,/1A5,ATEN,TWOA,CALU,MYC...PYD.....,0	SRM
122	ROM ./188,AWR1,ASHR...SR0...CTP1..REPEAT,,GCRDSR,0	SRLC
123	FTA ARA1,ALUA,CRL06	ML DSH
124	ROM ./0DA....MYQ.....,0	DLA END
125	ROM ./0D7,AWA2,BSHR,CALU,MYC.....,GCRFNU,0	DLA END
126	ROM ./019..BINV..MYC.....,0	ROUT,AFFICH,INCR
127	ROM ETAT,/07E..ALUB,CALU,.QYC.....SEQBUS...0	DISPLAY INCR
128	ROM ./1E9,ARA1,ALUA.....,BUSR,GCRVML,CRL06	DLA END
129	ROM ./164,AEP,ASHR,CALU,MYC.....,0	DLN,DRN END
12A	ROM ./041,ARA1,ACR,CLUR,MYC.....,0	TEST RB
12B	ROM FLAG,/034,ARA2,ALUA.....,GCRFNU,0	TEST DLA
12C	ROM ./043,.BCR....SYD...WBUS,...0	TEST TMP-TPM
12D	ROM ./0CE..ZERO...SR0.....,0	DRA
12E	ROM ./115,ATW0,TWOA,CALU,MYC,.,PM2.....0	TRAP CORR LONG EX.
12F	ROM ./115,ATW0,TWOA,CALU,MYC.....0	TRAP
130	ROM ./0BF.....GFRZO,0	VERIF MAN. REG M
131	ROM ./0CD....MYQ.....,0	DSH
132	ROM ./0DC,AWA2,ALUB,.....BUSR,GCRFNU,0	DSH
133	ROM ./038....MYQ.....,0	TEST Q.CHARG NO.
134	ROM ./0CA,AEN,ALUA,CALU,MYC..,PYD,CTP1.....0	MLRI
135	ROM ./1D3,AWR2,APB,...SYD,PM2,...BUSR..0	MLRI
136	ROM ./0E9.....,0	TEST DLA
137	ROM ./0C7,AEP,APB,CALU,MYC....CTP1.....0	MLK
138	ROM ./0C6,AEN,ALUA,....PYD.....0	ML
139	ROM ./1C3,ARR2,ALUA,CALU,.QYC,.PM2....BUSR.,0	ML
13A	ROM ./0C4,AEN,ALUA,....,PYD.....0	MS
13B	ROM ./1B3,ARC1,ALUA.....PM2,CTP1,WMEM,.BUSR,,0	MS
13C	ROM ./0C2,AEN,ALUA,CALU,.QYC,.PYD.....0	MSRD
13D	ROM ./1A3,ARC1,ALUA.....PM2,CTP1,WMEM,.BUSR,,0	MSRD
13E	ROM FLAG,/00A,AEP,ALUA.....,WMEM,...,0	TEST MEMOIRE NO2
13F	ROM ./053,ARA1,TWOA,.MYC,QYC,SM2,PM2,.WMEM,...,0	TEST MEMOIRE NO1

ADD.		
140	ROM ./07E.....,RBUS,..GBOK,0	TEST MAN REG M
141	ROM ./1E9,AWR2,AMB,.....BUSR,GFSTOV,0	UPD STK MSRD
142	ROM ./1CF,AWR1,ZERO,.....,BUSR.,0	NGR
143	ROM ./101,AZ,AMB,.....,WMEM,.BUSR.,CRSUB	C2
144	ROM ./188..ALUA,.....WBUS,SEQBIO...CRIO	CIO OTR
145	ROM ./0B7,ARA2,ALUA,CALU..QYC.....,0 MU- MUL.TOR IN Q REG.	
146	ROM FLAG,/01C,ATW0,APB,.MYC.....,GCRFNU,0	TEST NO 1
147	ROM ./018,....SLQ.....,0	TEST NO 1
148	ROM ./086,AWA1,MULTI...SR0...CTP1..REPEAT...0 MU- ALGORITHM	
149	ROM ./085,AWA1,MULTI..,MYQ.....,GMULTI,0	MULTI 16TH PASS
14A	ROM ./084,AWA2,BSHR,.....,0 MULTI STORE LSB OF PROD.	
14B	ROM ./0D7,ARA2,ALUA,.....GCRFNU,0	MULTI UPDATE FNU
14C	ROM ./0AD,.ALUB,..SR0,SP2,...SEQBUS,BUSR,GBTMF,0 FPP SINGLE RD MA	
14D	ROM ./042.....SP2....SEQBUS,BUSR,GBTMF,0 FPP OP/S DOUBLE READ M1	
14E	ROM ./053,ATW0,ASHR..MYC,QYC,SM2,PM2..WMEM,...0 T. MEMOIRE NO1	
14F	ROM ./06C,AWA1,ALUB....SM2,PM2.....0	TEST MEMOIRE NO1
150	ROM ./09F.....GFRZO,0	TEST Q.CHARG NO
151	ROM ./0A1,AWA1,BCR..MYC,QYC.....,0	TEST DLA
152	ROM FLAG,/030....MYQ..SP2,...SEQBUS,BUSR,GBTMF,0 FPP READ LAST MA	
153	ROM ./173,ARA0,TWOA,...SYD.....0 FPP OPS WAIT,LD S WITH 1ST A0,	
154	ROM ./010..BINV,CALU.,QYC,SP2...WEXM,SEQBUS,BUSR,GBOF,0 FPP/S SI.	
155	ROM ./010.....SP2,..WEXM,SEQBUS,BUSR,GBOF,0 FPP/S DOUBLE ST M1	
156	ROM ./0E9.....,0	TEST DLA
157	ROM ./0A7,ARA0,A0B...,SYD...ABUS..BUSR,GBTMP,0	INR
158	ROM ./0A6,AWR1,DBIO,CIOR,MYC.....,SEQBUS..GCSEL,CRIO	INR
159	ROM ./188,AWR1,A0B...SLQ.....,0	INR TST SST
15A	ROM ./0A4,AWA1,ALUA,.....,GCRVZO,0 DIV MEMO SIGNE DIVD	
15B	ROM ./0A3,AWA1,DIVSH...SL0...,CTP1,...,GCRDSR,0 DIV 1ST PASS	
15C	ROM ./0A2,AWA1,DIVSH,..SL0...,CTP1,.REPEAT...0 DIV PROCESS	
15D	ROM FLAG,/1B6,AWA1,DIVALU...SL0.....,GCRFNU,0 DIV 16TH PASS	
15E	ROM ./0A0,ATW0,APB,CLUR,MYC,..PYD.....0	TEST DLA
15F	ROM ./091,AWA2,BCR,..SR0.....,0	TEST DLA
160	ROM ./039.....,RBUS,..GBOK,0	TEST Q.CHARG NO.
161	FTA AWA2,ALUB,0	DIV ST CORTD QUOT
162	ROM ./09F.....,0	TMP TEST
163	ROM ./033,AZ,ALUA,.MYC.....,0	TMP TEST
164	ROM ./09A,AWA1,DBIO.....,RBUS,SEQBIO..,GBOF,0	FFX LD A1
165	ROM ./17D.....,RBUS,.BUSR,GBOF,0	FFX RESET BSY
166	ROM ./022,AWCT,ALUB.....,CTP1.....0	TEST NO 3
167	ROM ./023,AWCT,ALUB...SL0...,CTP1.....0	TEST NO 3
168	ROM ETAT,/0DE.....,SEQBUS,..0	VERIF MAN REG L
169	ROM FLAG,/09C,APSW,AANDB.....,GCRFNU,0	TEST TMP-TPM
16A	ROM ./030,ARA2,ALUA.....WBUS,SEQBUS,BUSR,GBTMF,0 FFL LD M1	
16B	ROM ./093,AWA2,TWOA,.....,GCRFNU,0	DA
16C	ROM ./092,AWA1,DADD.....,BUSR.,CRADD	DA
16D	FTA AWA2,ASHR,0	DAS END
16E	ROM ./090,AEP,TWOA..MYC.....,0	TEST DLA
16F	ROM ./081,AEP,APB,.MYQ,..PYD.....,0	TEST DLA
170	ROM ./019..BSHR,CALU,MYC.....,0	ROUT,AFFICH,INCR
171	ROM ./152,AEP,ALUA,CBIO,MYC..SYD....SEQBUS,..0	DAR* DA
172	ROM ./1F7,AEP,ALUA,CBIO,MYC..SYD....SEQBUS,BUSR,..0	EL
173	ROM ./088,AEP,ALUA,CIOR..GYC,SYD....SEQBUS,..0	CC
174	ROM ./189,AWA2,TWOA.....,GCRFNU,0	DS
175	ROM ./142,AEP,ALUA,CBIO,MYC..SYD,...SEQBUS,..0	DSR
176	ROM ./0E9.....,0	TEST DLA
177	ROM ./0B7,AWA0,ALUB..MYQ.....,BUSR.,0	CW CA
178	FTA ARA0,AMB,CRCMP	CW CA
179	ROM ./083,AWR1,BCR,CIOR,MYC.....SEQBUS...0	LC
17A	ROM ./027..ZERO..MYQ,SR0.....,0	TEST NO 2
17B	ROM ./026..ALUB..MYQ,,PYD.....0	TEST NO 2
17C	ROM ./1C8,AEP,ALUA,...SYD.....BUSR.,0	LC
17D	FTA AWR1,A0B,0	LC END
17E	ROM ./080,AEP,APB,....,PYD,.WBUS,...0	TEST DLA
17F	ROM ./18E,AWA0,ZERO.....,SEQBIO..GFETCH,0	TEST DLA

Table 2-4A contd.

ADD		
180	ROM ./028....MYQ.....RBUS...GBOK.0	DISPLAY INCR
181	ROM ./020...CBIO.MYC.....SEQBUS...0	VERIF MAN REGM
182	ROM ./050....MYQ.........0	ROUT.AFFICH.INCR
183	ROM ./0E9.............0	ROUT.AFFICH.INCR
184	ROM ./07A.ARR1.ALUA.....WBUS..BUSR.GBTME:0	WER
185	ROM ./188.ARR1.ALUA.....WBUS.SEQBUS...0	WER
186	ROM FLAG./054.AR15.AMB...SRQ.....GCRFNU.0	TEST NO 3
187	ROM FLAG./064.ARCT.AMB...SLQ...CIP1....GCRFNU.0	TEST NO 3
188	ROM ./076.AWR2.APB.....SYD.....BUSR..0	RTN
189	ROM SNPLA./100..DBIO....SM2.PYD...SEQBUS.BUSR..0	RTN
18A	ROM ./09F.............0	TEST NO 2
18B	ROM ./018..ZERO...SRQ..PM2.....0	TEST NO 2
18C	ROM ./072.ATWO.APB.CALU.MYC.....GFENB.0	COMPUTE MASK RTNAIS
18D	ROM ./06E.AWA0.BINV..MYQ.....0	COMPUTE MASK RTNAIS
18E	ROM FLAG./024.ARA1.AXB.....GCRFNU.0	TEST DLA
18F	ROM ./061.ATWO.APLB1..MYC.....0	TEST RB
190	ROM ./019..BINV..MYC.....0	ROUT.AFFICH.INCR
191	ROM ./18E.ARA0.A0B.CLUR.MYC.QYC.....0	MASK STACK PSW RTNAIS
192	ROM ./09F.............0	TEST MEMOIRE NO1
193	ROM FLAG./002...CBIO.MYC.....SEQBUS...0	TEST MEMOIRE NO1
194	ROM ./06A.AWR1.AMB....SYD.....GFSTOV.0	CF.15R2
195	ROM ./068.APSW.ALUA....SP2...WMEM.BUSR..0	CF
196	ROM ./0E9.............0	TEST DLA
197	ROM ./0A7.AEP.ALUA..MYQ..SP2...WMEM.SEQBUS.BUSR..0	CF
198	ROM ./1E9..ALUB....SYD.PYD...SEQBUS.BUSR..0	CF END
199	ROM ./05E..BSHR.CALU.MYC.....0	EX
19A	ROM ./09F.............0	TEST NO 3
19B	ROM FLAG./078....MYQ.....0	TEST NO 3
19C	ROM FLAG./05C.AEP.AXB....SM2.PM2.....GCRFNU.0	TEST MEMOIRE NO2
19D	ROM ./0FB.....RBUS...GBOK.0	TMP TEST
19E	ROM ./060.AWA0.BCR..MYC.....0	TEST RB
19F	ROM ./051.AEP.APB..MYC...PYD..WBUS....0	TEST RB
1A0	ROM FLAG./13A.AWA0.ALUB..MYQ...PM2.....0	MVF TEST LGHT=0
1A1	ROM FLAG./174.ATEN.AXB.....GCRFNU.0	EX TEST IF T2
1A2	ROM ./09F.............0	TEST MEMOIRE NO2
1A3	ROM FLAG./062...CBIO.MYC.....SEQBUS...0	TEST MEMOIRE NO2
1A4	ROM ./05A.ARR2.AMB.CALU.MYC.....0	MVF LGHT-2 IN M
1A5	ROM ./128.AWA1.APB..MYQ..SYD.....BUSR..0	MVF A1=SOURCE
1A6	ROM ./096.ATWO.ACR.CALU.MYC.....WBUS.SEQB10..GFKYZO.CRIO	TMP T.
1A7	ROM FLAG./058.....SLQ....WBUS...GBTMP.0	TEST TMP-TPM
1A8	ROM FLAG./12A.AWA1.AMB....SYD....SEQBUS..GMOVE.0	MVF WRITE DEST
1A9	ROM ./13A.AWR2.ZERO.....0	MVF CLEAR LGHT
1AA	ROM ./09F.............0	TEST NO 3
1AB	ROM ./013.AWA2.FORA.....0	TEST NO 3
1AC	ROM FLAG./052..ALUB....SM2.PM2..WMEM.SEQBUS...0	TEST MEMOIRE NO1
1AD	ROM ./080.ARA0.ALUA....SYD.PYD.....0	TEST MEMOIRE NO1
1AE	ROM SNPLA./1FF.AWA1.ALUB.C10R.MYC.QYC..PM2...SEQB10.	GFETCH.0 TRB
1AF	ROM ./081.AWA0.ALUB....SYD.PYD.....GFRZO.0	TEST MEMOIRE NO1
1B0	ROM ./058.ATWO.ALUA.CALU.MYC.QYC.....0	MVF
1B1	ROM ./046.AWA0.BSHR..MYQ.....0	RER
1B2	ROM FLAG./03C..BSHR..MYC.....CCRFNU.0	ROUT.AFFICH.INCR
1B3	ROM FLAG./088.ATWO.A0B..MYC.QYC.....GFRZO.0	TEST NO 1
1B4	ROM FLAG./0F2.AWA0.ALUB.....PM2.....0	MVB TEST LENGTH
1B5	ROM FLAG./108.AWA2.AMB.....0	MVB PREPARE A2
1B6	ROM ETAT./0BE.....SEQBUS...0	VERIF MAN. REG M
1B7	ROM FLAG./028..ALUB..MYQ...PM2..WMEM [illegible]	WRITE
1B8	ROM ./162..ALUB.....WMEM..BUSR..0	INT
1B9	ROM ./03A.ARA0.A0B....SYD...RBUS..BUSR.GBTME.0	RER
1BA	ROM ./09F.............0	TEST NO 3
1BB	ROM ./01A..ZERO...SRQ.....0	TEST NO 3
1BC	ROM ./058.ATEN.ALUA.CALU..QYC....WBUS.SEQB10.	GFETCH.0 TEST TMP
1BD	ROM ./083.....SP2....SEQBUS.BUSR.GBTMP.0	FPP DOUBLE LD 2ND WORD
1BE	ROM ./040..BCR..MYC.....GFKYZO.0	TEST RB
1BF	ROM FLAG./014.AEP.AXB..MYQ.....GCRFNU.0	TEST RB

ADD		
1C0	ROM ./1E8.....RBUS...GBOK.0	VERIF MAN. PUPIT
1C1	ROM ./037.AWA1.AMB.....0	DER MVF REST A1
1C2	ROM FLAG./02C..BSHR..MYC.QYC.....GCRFNU.0	ROUT.AFFICH.INCR
1C3	ROM ./085.ATWO.ACR..MYC.QYC.....GFRZO.0	TEST NO 2
1C4	ROM FLAG./0F1.AWR2.ALUB..MYQ.....0	DER MOVE REST R2
1C5	ROM ./188.AWR1.DBIO.CBIO.....SEQBUS...CRRTN	RER
1C6	ROM ./0CC...CBIO..QYC.....SEQBUS...0	TEST Q.CHARG NO.
1C7	ROM ./029..ALUB.CLUR.MYC.....WBUS.....0	TEST Q.CHARG NO.
1C8	ROM ./036.AWA2.AMB.....0	DER MVF REST A2
1C9	ROM ./038.ATWO.APB.CALU.MYC.....0	DER MOVE M=LGTH
1CA	ROM ./09F.............0	TEST DLA
1CB	ROM ./071.ATWO.ASHR..MYC.....0	TEST DLA
1CC	ROM ./07F...BINV...QYC.....0	TEST NO 2
1CD	ROM ./098.ATWO.ASHR..MYC.QYC.....GFRZO.0	TEST NO 3
1CE	ROM ./0AC.AWA0.ALUB.....SEQBUS..GFLOT.0	FPP OP/S LD EXP
1CF	ROM ./188.AEP.ALUA....SYD....SEQBUS..GFLOT.0	FPP OP LD EXP
1D0	ROM ./02F.............0	NOT USED
1D1	ROM ./06A.AWR1.AMB....SYD.....0	CF.15R2N
1D2	ROM FLAG./07C..BSHR..MYC.SRQ.....GCRFNU.0	ROUT.AFFICH.INCR
1D3	ROM ./032.ARA0.....GCTLD.0	TEST NO 3
1D4	ROM FLAG./0EA.AWA1.APB....SYD....SEQBUS..GMOVE.0	MVB WRITE
1D5	ROM FLAG./0EA.AWA1.APB....SYD....SEQBUS..GBEX.0	MVUS WRITE
1D6	ROM ETAT./09E.....SEQBUS...0	TEST Q.CHARC NO.
1D7	ROM FLAG./0D8..ALUB.CBIO..QYC....WBUS.SEQBUS...0	ROUT.AFFICH.INCR
1D8	ROM FLAG./084.ATEN.AXB.....GCRFNU.0	TEST NO 2
1D9	ROM ./017.AEP.AMB.....PYD.....0	TEST NO 2
1DA	ROM ./09F.............0	TEST DLA
1DB	ROM ./070.ATEN.TWOA..MYC.....0	TEST RB
1DC	ROM FLAG./09A....MYQ.....0	TEST NO 3
1DD	ROM ./078.ATWO.ASHR..MYC.QYC.....0	TEST NO 3
1DE	ROM FLAG./0DC..BINV.....0	TEST NO 1
1DF	ROM ./049..ALUB.....WBUS....0	VERIF MAN. REG M
1E0	ROM ./100..ALUB.....PYD.....0	TRAP DLN
1E1	ROM FLAG./195.ARA1.ALUA.....0	DLN
1E2	ROM ./09F.............0	TEST NO 1
1E3	ROM ./021..BINV..MYC.....0	TEST NO 1
1E4	ROM FLAG./01A.....PM2.....0	TEST NO 2
1E5	ROM ./033....MYQ.....0	TEST NO 2
1E6	ROM FLAG./04C..BSHR..MYC.....GCRFNU.0	ROUT.AFFICH.INCR
1E7	ROM ./04C....MYQ.....0	TEST NO 1
1E8	ROM ./016.AEP.APB.CALU.MYC.SRQ.....0	TEST NO 2
1E9	ROM FLAG./074.ATEN.AXB.....GCRFNU.0	TEST NO 2
1EA	ROM ./09F.............0	TEST RB
1EB	ROM ./033.ATEN.ASHR.CALU.MYC.....0	TEST RB
1EC	ROM ./012.ATEN.ALUA..MYC.QYC.....0	TEST NO 3
1ED	ROM FLAG./044.ARA2.AMB...SRQ.....GCRFNU.0	TEST NO 3
1EE	ROM ./1E9.AEP.ALUA....SYD....SEQBUS...CRFLO	FPP STORE ST EXP
1EF	ROM FLAG./010.....SLQ.SP2...WEXM.SEQBUS.BUSR.GB0F.0	FPP ST MANTI.
1F0	ROM ./100..ALUB.....PYD.....0	TRAP DRN
1F1	ROM FLAG./185.AWA1.ASHR...SRQ.....GCRDSR.0	DRN
1F2	ROM ./09F.............0	TEST NO 1
1F3	ROM ./07F.............0	TEST NO 1
1F4	ROM ./0C1.....SM2.PM2..SEQBUS...0	TEST MEMOIRE NO2
1F5	ROM ./063..ALUB....SYD.PYD.....0	TEST MEMOIRE NO2
1F6	ROM ./097..DBIO.....WBUS.SEQBUS...0	VERIF MAN REG L
1F7	ROM ./0BB.ARR1.ALUA.CALU.MYC.....WBUS..BUSR.GBTMP.0	CIO OTR
1F8	ROM ./036.AEP.ALUA.CALU.MYC.....GCTLD.0	DER MVB READ
1F9	ROM ./007.AWA1.AMB.....PP2.....GCTLD.0	DER MVB WRITE
1FA	ROM ./03E.AEP.ALUA.CALU.MYC.....GCTLD.0	DER MVF READ
1FB	ROM ./005.AWA1.APB.....PP2.....GCTLD.0	DER MVF WRITE
1FC	ROM FLAG./06C.ARA1.AXB....SM2.PM2.....GCRFNU.0	TEST MEMOIRE NO1
1FD	ROM FLAG./0C0.ARA0.ALUA.CALU.MYC..SYD.PYD.....0	TEST MEMOIRE NO1
1FE	ROM ./120.ATWO.TWOA.CALU.MYQ.QYC.....GCTLD.0	PAGE FAULT ML
1FF	ROM ./125.ATWO.TWOA.CALU..QYC.....GCTLD.0	PAGE FAULT

Table 2-4B Control-ROM Microinstruction Listing 2856

ADD		
000	ROM ./1E8.AR15.ALUB.CALU.MYC.GYC....WBUS...,0	IDLE
001	FTA ..0	NO JUMP
002	ROM ./1E9.....SP2.PP2....BUSR..0	INCR P
003	ROM FLAG./0D0.AZ.ALUA.CALU..GYC.....GAEXL.0	NO FLOT PROC
004	ROM FLAG./1F8.ASYS.TWOA.CALU..GYC.....0	TEST DISPLAY
005	ROM ./1FB.....SM2.PM2.....GFKYZO.0	DECR BEFORE VISU
006	ROM ./1FF.AEP.ALUA.CALU.MYC.....0	VISUA
007	ROM ./1FF..DBIO.CBIO.MYC.....SEQBUS...0	VISUB
008	FTA AWR1.ALUB.CRLOG	LD
009	ROM ./1E9..ALUB....SYD.PYD....BUSR..CRLOG	LD P
00A	ROM ./160.ASYS.ALUA.....WBUS....0 RCP IN L REG.	LR OR RR
00B	ROM ./1FF.ARA0.ALUA..MYC.....0	ERRONEOUS START
00C	ROM ./101.ARR1.ALUA,.....WMEM..BUSR..0	ST
00D	ROM ./101.AEP.ALUA.....WMEM..BUSR..0	ST P
00E	ROM ./0E6.ATW0.ALUA.CALU.MYC.....0	STD
00F	ROM ./0E5.ATW0.ALUA.CALU.MYC.....0	STD P
010	ROM FLAG./1D0.ASYS.ALUA.CALU..GYC.....0	TEST AUTOREST
011	ROM ./1E9..ALUB....SYD.PYD....BUSR..0	AB
012	ROM FLAG./0E0.AWA0.ALUB.....RBUS...GBOK.0	SAVE P TEST IF L/R R
013	ROM ./0E0.ARA0.ALUA....SYD.PYD.....0	LOAD P AND S LR
014	ROM ./1D8.ATW0.TWOA.CALU.MYC.....0	INT
015	ROM ./1D8.ATW0.TWOA.CALU.MYC...PM2.....GFKYZO.0	INT DECR
016	FTA ..0	FETCH
017	ROM ETAT./1FE.....SEQBUS..GIDLE.0	VISU IDLE
018	ROM FLAG./193.AEP.ALUA.CALU.MYC.....GCRVZO.0	SLASLN SAVE P
019	ROM FLAG./158.AEP.ALUA.CALU.MYC.SLQ.....GCRVZO.0	DLADLN SAVE P
01A	ROM FLAG./17B.ARR1.ALUA.CALU..GYC.....0	SLL SLC
01B	ROM ./0CE.AWA1.ASHL...SLQ...CTP1..REPEAT..GCSEL.0	DLL DLC
01C	ROM FLAG./16B.AEP.ALUA.CALU.MYC.....0	SRA SRN
01D	ROM FLAG./14B.AEP.ALUA.CALU.MYC.SLQ.....0	DRA DRN
01E	ROM ./0D0.ARR1.ALUA.CALU..GYC.....0	SRL SRC
01F	ROM ./0CE.AWA1.ASHR...SRQ...CTP1..REPEAT..GCRDSR.0	DRL DRC
020	FTA AWR1.APB.CRADD	AD
021	ROM ./1E9.AEP.APB....SYD.PYD....BUSR..CRADD	AD P
022	ROM ./0EC.ARR2.ALUA,...SYD.,...BUSR..0	RT3
023	ROM ./0E8.ARR2.ALUA,...SYD.....BUSR..0	RT3S
024	ROM ./101.ARR1.APB.....WMEM..BUSR..CRADD	AD S
025	ROM ./101.AZ.APLB1.....WMEM..BUSR..CRADD	IM
026	ROM ./077.ATW0.TWOA.CALU.MYC.....0	RTN MASTER
027	ROM ./19E.AW15.AMB....SYD.....GFSTOV.0	INT UPDATE A15
028	ROM FLAG./0D0.AZ.ALUA.CALU..GYC.....GAEXL.0	TRAP SLN
029	ROM ./0E3.ATEN.TWOA.CALU.MYC.GYC..PYD.....0	SLN
02A	ROM ./159.ATEN.ACR.CALU.MYC.GYC.....0	IPL SET
02B	ROM ./145.AEP.ALUA....SYD...RBUS..BUSR.GBOK.0	IPL END
02C	ROM FLAG./1D2.AWCT.DBIO..MYC..SM2.PM2.CTP1..SEQBUS...0	MLRI
02D	ROM ./0DC..ALUB....SYD.PYD....BUSR..0	MLRI
02E	ROM ./134...CLUR.MYC.....GCSEL.0	AUTO RESTART
02F	ROM FLAG./1C0.APUP.ALUA.CALU..GYC.....0	TEST IPL
030	FTA AWR1.AMB.CRSUB	SU
031	ROM ./1E9.AEP.AMB....SYD.PYD....BUSR..CRSUB	SU P
032	ROM SNPLA./100...CBIO.MYC.GYC.SP2.PP2...SEQBUS...0	RTZ
033	ROM SNPLA /100...CBIO.MYC.GYC..PP2...SEQBUS...0	RT2S
034	ROM ./101.ARR1.AMB.....WMEM..BUSR..CRSUB	SU S
035	ROM FLAG./0BC.AEN.ALUA.....GCRFNU.0	C2 OR NGR
036	ROM ./077.ATW0.TWOA.CALU.MYC.....0	RTN USER
037	FTA AWR1.A0B.0 INH.RTN A15 AND LC END	
038	ROM FLAG./0D0.AZ.ALUA.CALU..GYC.....GAEXL.0	TRAP SRN
039	ROM ./0DE.ARR1.ALUA.CALU..GYC.....0	SRN
03A	ROM FLAG./1C4..BSHR.CALU.MYC.....GCRFNU.0	WAIT IO
03B	ROM ETAT./1FF.AEP.ALUA....SYD.....0	WAIT IO
03C	ROM FLAG./1C2.AWCT.DBIO....SP2.PM2.CTP1..SEQBUS..GCRVML.0	ML LOOP
03D	ROM ./0DC..ALUB....SYD.PYD....BUSR..0	ML END
03E	ROM ./15F.ATW0.ACR.....PYD.....0	IPL
03F	ROM FLAG./1B0.....SLQ....RBUS...GBOK.0	TEST LOADM

ADD		
040	FTA AWR1.AANDB.CRLOG	AN
041	ROM FLAG./1C8.APSW.AANDB.CALU.MYC.....BUSR..0	HLT.RIT.INH.RTA15
042	ROM ./0FD...CBIO.MYC...PP2...SEQBUS...0	RT5
043	ROM ./0F5...CBIO.MYC...PP2...SEQBUS...0	RT5S
044	ROM ./101.ARR1.AANDB.....WMEM..BUSR..CRLOG	AN S
045	ROM ./101..ZERO.....WMEM..BUSR..0	CM
046	FTA ARR1.AANDB.CRLOG	TM
047	ROM ./1E9.....BUSR..CRFLO FPP WAIT EXEC.	
048	ROM FLAG./1A6.ARA1.DIVALU.....GCRFNU.0	DIV TEST COR.REM.
049	ROM FLAG./140.ARA1.AXB.CALU.MY0.GYC.....0	DIV TEST QUOT.
04A	ROM ./0E2.AEP.AMB.CALU.MYC.....0	SLN
04B	ROM FLAG./185.AWR1.TWOA....PP2.....0	SLN LOOP
04C	ROM FLAG./182.ARCT.ALUA,...SP2.PM2.CTP1.WMEM.SEQBUS...0	MS LOOP
04D	ROM ./1E9..ALUB....SYD.PYD....BUSR..0	MS END
04E	ROM FLAG./1A8.....SLQ.....GFRZO.0 TEST READM	
04F	ROM ./172..DBIO.CBIO.MYC.....WMEM.SEQBUS..GBCP.0	LOAD M
050	FTA AWR1.A0B.CRLOG	OR
051	ROM FLAG./188.APSW.A0B.CALU.MYC.....0	END SMD LKM
052	ROM ./0EC..DBIO....SYD.PP2...SEQBUS.BUSR..0	RT4
053	ROM ./0E8..DBIO....SYD.PP2...SEQBUS.BUSR..0	RT4S
054	ROM ./101.ARR1.A0B.....WMEM..BUSR..CRLOG	OR S
055	ROM ./0A8.AWA0.BSHR..MY0.....0	INR
056	ROM FLAG./1A0.....SLQ.....0 TEST READST	
057	ROM FLAG./190.ASYS.TWOA.CALU..GYC.....GBCP.0	READ M
058	ROM ./1A6.AWA1.DIVALU.....0 DIV CORR.REM.	
059	ROM FLAG./140.ARA1.AXB.CALU.MY0.GYC.....0	DIV TEST QUOT.
05A	ROM ./0E2.AEP.AMB.CALU.MYC.....0	SRN
05B	ROM FLAG./1A5.AWR1.ASHR...SRQ..PP2.....GCRDSR.0	SRN LOOP
05C	ROM FLAG./1A2.ARCT.ALUA....SM2.PM2.CTP1.WMEM.SEQBUS...0	MSRD LOOP
05D	ROM ./0BE..ALUB..MY0..SYD.PYD.....0	MSRD END
05E	ROM ./198.....SLQ.....0	PUP
05F	ROM ./1FF.APSW.ALUA.CALU.MYC.....0	READ STATUS
060	FTA AWR1.AXB.CRLOG	XR
061	ROM ./047.APSW.ALUA.CALU.MYC..SP2.....GFSYS.0	INT
062	ROM ./0FC...CBIO.MYC.....SEQBUS...0	RT7
063	ROM ./0F4...CBIO.MYC.....SEQBUS...0	RT7S
064	ROM ./101.ARR1.AXB.....WMEM..BUSR..CRLOG	XR S
065	FTA AWA2.BSHR.0	DLN END
066	FTA ARR1.AXB.CRLOG	TNM
067	ROM ./180.AWA0.ALUB..MY0.....0	PUP
068	ROM FLAG./0D0.AZ.ALUA.CALU..GYC.....GAEXL.0	MVF 15R2 TRAP
069	ROM ./0DF.ARR2.ALUA.CALU..GYC..PYD.....0	MVF 15R2N
06A	ROM ./0D6.AWA0.ALUB.....PM2.....0	DLNDRN END
06B	ROM FLAG./195.AWA1.ASHL...SLQ..PP2.....0	DLN LOOP
06C	ROM ./0E4.AWR1.TWOA.....CTP1..REPEAT...0	SLA
06D	ROM FLAG./1D7.AWA0.ALUB.....0	SLN
06E	ROM ./1FF..DBIO.CBIO.MYC..SP2.PP2...SEQBUS...0	READ M PUP A
06F	ROM ./1FF..DBIO.CBIO.MYC.....SEQBUS...0	READM PUP B
070	ROM SNPLA./100.AR1215.....GCTLD.0	SH DSH
071	ROM ./18F.ARA2.ALUA.CALU..GYC.....GFKYZO.0	DSH
072	ROM ./1A0..DBIO....SYD....SEQBUS.BUSR..0	RT6
073	ROM ./1AC..DBIO....SYD....SEQBUS.BUSR..0	RT6S
074	FTA ARR1.ALUA.CRLOG	SHZERO
075	ROM ./0DC.ARA2.ALUA,.....BUSR.GCRFNU.0	DSHZERO
076	ROM ./092.AWA1.DSUB.....BUSR..CRSUB	DS
077	ROM ./1C5.ATW0.ALUA.CALU.MYC.....U	WAIT
078	ROM ./0C7.AEP.ALUA.CALU.MYC....CTP1.....U	ML
079	ROM ./150.ATW0.ASHR.CALU..GYC.....GBTMM.0	TL
07A	ROM ./195.AWA1.ASHL...SLQ.....0	DRN
07B	ROM FLAG./185.AWA1.ASHR...SRQ..PP2.....GCRDSR.0	DRN LOOP
07C	ROM ./0C5.AEP.ALUA.CALU.MYC....CTP1.....0	MS
07D	ROM ./148.ATW0.ASHR.CALU..GYC....WEXM...GBOM.0	TS
07E	ROM ./0C3.AEP.ALUA.CALU.MYC....CTP1.....0	MSRD
07F	ROM FLAG./1F4..BCR.CALU..GYC.....GCRFNU	PUP

ADD		
080	ROM ./008..ALUB....SYD.....0	CIO QTR
081	ROM ./100.....0	GO TO TRAP (WMP)
082	ROM ./182.AWA2.DBIO.....RBUS,SEQBIO...0	FFX LD A2
083	ROM SNPLA./100.ARR2.ALUA.CALU.MYC.GYC.....0	RT1
084	ROM ./18B.AWR1.TWOA.....CTP1..REPEAT...0	SLL
085	ROM ./18B.AWR1.ASHL...SLQ...CTP1..REPEAT..GCSEL.0	SLC
086	ROM ./169.....CTP1,....0	RT1D
087	ROM ./179.ARR2.ALUA.CALU..GYC.....GCTLD.0	RT1D
088	ROM FLAG./0B3..ZERO.CALU.MYC.....BUSR.GBTMF.0	FPP LOAD
089	ROM ./0BA.AWA1.ZERO.CALU..GYC.....GCRVZO.0	MUL-RESET PART.PROD
08A	ROM ./130.ARA0.ALUA.....WBUS..BUSR..0	EX T1 OR T3
08B	ROM FLAG./0D0.AZ.ALUA.CALU..GYC.....GAEXL.0	EX T2 TRAP
08C	ROM FLAG./0AB.ATEN.ACR.CALU.MYC.GYC....WEXM...GBOF.0	FPP STORE
08D	ROM ./1A8.....SEQBUS..GFRZO.0	LOAD M
08E	ROM FLAG./1D4.AEP.ALUA,...SP2....SEQBUS..GCRFNU.0	IPL LOOP
08F	ROM ./159..BSHR.CALU.MYC.SLQ.....0	IPL LOOP
090	ROM ./1AA.ATEN.ACR.CALU.MYC.....0	INR
091	ROM SNPLA./103.AEP.ALUA...SYD.....0	EX BSYZO.RESTORE S
092	ROM ./1ED.AEP.ALUA.CALU.MYC.....RBUS.SEQBIO..GFETCH.0	K=RCP L/RR
093	ROM SNPLA./100.AEP.ALUA.CALU.MYC.GYC.....0	RT1P
094	ROM ./18B.AWR1.ASHR.....CTP1..REPEAT..GCRDSR.0	SRA
095	ROM FLAG./1C7.AWA0.ALUB.....0	SRN
096	ROM SNPLA./100.ARCT.ALUA.CALU.MYC.....0	RT1D END
097	ROM ./169.AEP.ALUA.CALU..GYC...CTP1,....0	RT1DP
098	ROM FLAG./0B3..ZERO.CALU.MYC.....BUSR.GBTMF.0	FPP OPER
099	ROM ./0A5.ARA2.TWOA.CALU..GYC.....0	DIV
09A	ROM ./095.ARA1.ALUA.....WBUS..BUSR.GBTMF.0	FFL
09B	ROM ./0FE.AWR2.ALUB.....0	DLN.DRN END
09C	ROM FLAG./0B3.ATW0.ASHR.CALU.MYC.....BUSR.GBTMF.0	FPP OP/S
09D	ROM ./143.AEP.ALUA.CLUR.MYC..SP2...WMEM.SEQBUS.BUSR.GCSEL.0	INT
09E	ROM ./160.AEP.ALUA.CALU.MYC.....GFLOT.0	FFX
09F	ROM ./098.....RBUS...GBOF.CRFLO	FFX UPD CR
0A0	ROM ./105..ZERO....SYD.....GFSYS.0	IPL
0A1	ROM ./1E9.AEP.APB,...SYD.PYD....BUSR..0	RF
0A2	ROM ./0E7.ATW0.ALUA.CALU.MYC.....0	RT3B
0A3	ROM SNPLA./100.ARR2.ALUA.CALU..GYC.SYD.....0	RT3C
0A4	ROM ./0DB.AWA1.ASHL...SLQ...CTP1..REPEAT...0	DLA
0A5	ROM FLAG./01F.ATW0.ALUA,....PYD.....0	DLN
0A6	ROM ./155..BSHR.CALU.MYC...PM2.....0	IPL LOOP
0A7	ROM ./0C8.AEP.ALUA.CALU..GYC.....0	RT3BM
0A8	ROM ./08D.....BUSR.GBEX.0	EL
0A9	ROM ./08E...CBIO..GYC.SP2....SEQBUS.BUSR..0	DA
0AA	ROM ./14F..BSHR.CALU.MYC.....0	IPL LOOP
0AB	ROM ./152...CBIO.MYC..SP2.PP2...SEQBUS...0	DAK
0AC	ROM ./101.ARR1.ALUA.....WMEM..BUSR.GBEX,0	ES
0AD	ROM ./094.AWA2.APB.CALU.MY0.GYC.....0	DA
0AE	ROM ./1E9.AEP.ALUA,...SYD...SEQBUS...0	TL END
0AF	ROM FLAG./150.....SLQ.SP2....SEQBUS.BUSR.GBTMM.0	TL LOOP
0B0	ROM ./140..BSHR.CALU.MYC.....0	IPL LOOP
0B1	ROM ./1E9.AEP.AMB,...SYD.PYD....BUSR..0	RB
0B2	ROM FLAG./170.AIPL.APB.CALU.MYC.....WMEM....0	IPL NEW QUART
0B3	ROM SNPLA./100.....PP2.....0	RT2C
0B4	ROM ./0D2.AWA1.ASHR...SRQ...CTP1..REPEAT..GCRDSR.0	DRA
0B5	ROM FLAG./0DF.ATW0.ALUA.....PYD.....0	DRN
0B6	ROM ./1E9.AEP.ALUA....SYD...SEQBUS...0	TS END
0B7	ROM FLAG./148.....SLQ.SP2...WEXM.SEQBUS.BUSR.GBOM.0	TS LOOP
0B8	ROM FLAG./0D0.AZ.ALUA.CALU..GYC.....GAEXL.0	TRAP
0B9	ROM ./08A...CBIO..GYC.SP2....SEQBUS.BUSR..0	DS
0BA	ROM ./1E9.AW15.DBIO.....SEQBUS...0	IPL END
0BB	ROM ./142...CBIO.MYC..SP2.PP2...SEQBUS...0	DSK
0BC	ROM ./13D..BSHR.....SYD....SEQBUS...0	INT
0BD	ROM ./08B.AWA2.AMB.CALU.MY0.GYC.....0	DS
0BE	ROM ./09E.AZ.APLB1.CALU.MYC.....BUSR.GCRVML.CRADD	DIV COR.QUOT
0BF	ROM ./1E9.AWA2.ALUB.....BUSR.GCRVML.CRLOG	DIV QUOT OF

ADD		
0C0	FTA AWR1.ALUB.0	LDK
0C1	ROM ./1E9..ALUB....SYD.PYD....BUSR..0	LDK F
0C2	ROM ./135..BCR.........BUSR.GFPLR.0	AR PAF INT
0C3	ROM ./0EE...CBIO.MYC...PP2...SEQBUS...0	RTSC
0C4	ROM ./04F.AWA2.APB...........0	MVF DEST IN A2
0C5	ROM ./1E9.ARA0.ALUA....SYD.PYD....BUSR..0	MOVE END SLN REST.P
0C6	ROM ./088.ARR1.ALUA.CALU..QYC........0	CA
0C7	FTA ARR1.AMB.CRCMP	CA
0C8	ROM ./086.ARR1.ACR.CLUR.MYC.......BUSR.GBCH.0	LC
0C9	FTA AWR1.BCR.0	ECR
0CA	ROM ./1E9..DBIO....SYD.PYD...SEQBUS.BUSR..0	AR PAF INT TRAP
0CB	ROM ./132.............GFSYS.0	AR END
0CC	ROM ./101.ARR1.ALUA.......WMEM..BUSR.GBCH.0	SC
0CD	ROM ./130..BSHR....SYD......GFKYZ0.0	PAGE FAULT AR
0CE	ROM FLAG./128.ARA0.APB.CLUR.MYC.SLQ........0	EX T8N TEST K1
0CF	ROM ./16E...CIOR.MYC.QYC....WBUS.SEQBIO..GFFTCH.0	EX LOAD K
0D0	ROM FLAG./0D0.AZ.ALUA.CALU..QYC.......GAEXL.0	TRAP
0D1	ROM FLAG./0D0.AZ.ALUA.CALU..QYC.......GAEXL.0	TRAP
0D2	ROM ./125.AWR2.ALUB...........0	PAGE FAULT ML
0D3	ROM SNPLA./100..DBIO.CBIO..QYC.SYD.PP2...SEQBUS...0	RT4C
0D4	ROM FLAG./118.AWA2.AMB.CBIO.MYC..SYD....SEQBUS..GMOVE.0	MVF READ
0D5	ROM ./056.AWA1.APB...........0	MVF REST A1
0D6	ROM FLAG./120.....SLQ........0	EX K1 TEST K2
0D7	ROM FLAG./0F8..BCR.CALU..QYC........0	EX K1N TEST MD
0D8	FTA ARR1.AMB.CRCMP	CW
0D9	FTA AEP.AMB.CRCMP	CWP
0DA	ROM ./124.APSW.ALUA.CALU.MYC........GFSYS.0	PAGE FAULT
0DB	ROM ./122.AR15.ALUA....SYD...WEXM..BUSR.GBOM.0	PAGE FAULT
0DC	ROM ./08C.ARR1.ALUA.CLUR.MYC.......BUSR.GBCH.0	CC
0DD	ROM ./11D..ALUB..MYQ..SM2...WMEM.SEQBUS.BUSR..0	PAGE FAULT
0DE	ROM FLAG./118.....SLQ........0	EX K1K2 TEST K3
0DF	ROM FLAG./0F8..BCR.CALU..QYC........0	EX K1K2N TEST MD
0E0	ROM ./078..ALUB....SYD.......0	WER
0E1	ROM FLAG./0D0.AZ.ALUA.CALU..QYC.......GAEXL.0	TRAP
0E2	ROM ./117.ATWO.APB.CALU.MYC..SM2...WEXM.SEQBUS.BUSR.GBOM.0	PAF
0E3	ROM ./0ED...CBIO.MYC......SEQBUS...0	RT7C
0E4	ROM ./057..ALUB..MYQ...PM2..WMEM..BUSR..0	MVF PREP WRITE
0E5	ROM ./057..ALUB..MYQ...PM2..WMEM..BUSR.GBEX.0	MVSU PREP WRITE
0E6	ROM FLAG./108.....SLQ........0	EX K1K2K3 TEST K4
0E7	ROM FLAG./0F8..BCR.CALU..QYC........0	EX K1K2K3N TEST MD
0E8	ROM ./132.AW15.AMB.CIOR.MYC.....RBUS.SEQBIO..GFSTOV.0	PAGE FAULT
0E9	ROM ./1E9.AEP.ALUA....SYD....SEQBUS.BUSR..CRRTN	RTN 15R2N
0EA	ROM ./110.ATEN.TWOA.CALU..QYC..PM2......0	TRAP
0EB	ROM ./073.AEP.ALUA.CBIO.MYQ.QYC.SYD....SEQBUS..GFPLR.CRRTN	RTNA15
0EC	ROM ./02E.ATWO.TWOA.CALU.MYC.........0	CF
0ED	ROM FLAG./130.AWA0.ALUB.......WBUS....0	EX
0EE	ROM ./068.ATWO.TWOA.CALU.MYC.........0	CF 15R1
0EF	ROM ./100.AW15.AMB...SLQ.SYD......GFSTOV.0	TRAP
0F0	ROM ./04E.ATEN.ACR.CALU.MYC.........0	RER
0F1	ROM FLAG./0D0.AZ.ALUA.CALU..QYC.......GAEXL.0	TRAP
0F2	ROM ./105.APSW.ALUA...SLQ.SP2...WMEM..BUSR.GFSYS.0	TRAP
0F3	ROM ./12C..DBIO....SYD....SEQBUS.BUSR..0	RT6C
0F4	ROM ./0E8.ARA1.ALUA....SYD.....BUSR..0	MVB PREP 1ST AD
0F5	ROM ./0EB.ARA1.ALUA....SYD.....BUSR.GBEX.0	MVUS PREP 1ST AC
0F6	ROM FLAG./0F8..BCR.CALU..QYC........0	EX K1K2K3K4 TEST MD
0F7	ROM FLAG./0D0.AZ.ALUA.CALU..QYC.......GAEXL.0	EX 150PC TRAP
0F8	ROM ./0C8.AEN.ALUA.CALU.MYC...PM2......0	MLK
0F9	FTA AWR1.BINV.CRLOG	C1
0FA	ROM ./104.AEP.ALUA..MYQ..SP2...WMEM.SEQBUS.BUSR..0	TRAP
0FB	ROM ./103..ALUB....SYD....SEQBUS...0	TRAP
0FC	ROM ./135......SM2.....BUSR..0	TRAP
0FD	ROM ./101..BINV.......WMEM..BUSR..CRLOG	C1S
0FE	ROM ./1E9.AEP.ALUA....SYD....SEQBUS.BUSR..0	STORE RESULT
0FF	ROM FLAG./0D0.AZ.ALUA.CALU..QYC.......GAEXL.0	TRAP

ADD		
100	ROM ./03F.............GFSYS.0	VERIF MAN. PUPIT
101	ROM ./19A.ARA0.ALUA..MYQ...PYD....BUSR..0	DLN.DRN END
102	ROM ./0EC.ARR2.APB....SYD.....DUSR..0	RTS
103	ROM ./1AD.ARR2.APB....SYD.....BUSR..0	RT7
104	ROM ./003...CBIO.MYC.....RBUS.SEQBIO...0	TMP TEST RD KEYS
105	ROM FLAG./004.ARA0.ALUA..........GCRFNU.0	TEST RETURN
106	ROM FLAG./0D0.AZ.ALUA.CALU..QYC.......GAEXL.0	EX OPER T4T7 TRAP
107	ROM ./066..BSHR.CALU.MYC.........0	EX OPER T1.T2.T3
108	ROM FLAG./0D0.AZ.ALUA.CALU..QYC.......GAEXL.0	MVB 15R2FU TRAP
109	ROM ./048.ARR2.ALUA.....PYD......0	MVB 15R2FUN
10A	ROM ./0E8.ARR2.APB....SYD.....BUSR..0	RT5S
10B	ROM ./1AC.ARR2.APB....SYD.....BUSR..0	RT7S
10C	ROM ./04A.ATWO.ALUA.CALU.MYC.QYC........0	MVB LENGTH>0
10D	ROM ./1E9.ARA0.ALUA....SYD.PYD....BUSR..0	MVB LENGTH=0
10E	ROM ./1E8.ARA0.AMB.....PYD......0	INT MOVE
10F	ROM ./125.ATWO.TWOA.CALU..QYC........0	PAF MOVE
110	ROM ./0DF.............GFRZ0.0	VERIF MAN. REG L
111	ROM SNPLA./100.ARR2.APB.CALU..QYC.SYD.......0	RT5C
112	ROM ./12C.ARR2.APB....SYD.....BUSR..0	RT7C
113	ROM SNPLA./100.AEP.ALUA.CBIO.MYC.QYC.SYD....SEQBUS...0	RT3
114	ROM ./048.AWA2.APB.CBIO.MYC..SYD....SEQBUS..GMOVE.0	MVB READ
115	ROM ./056.AWA2.APB...........0	MVB CORRECT A2
116	ROM ./0AE.ATEN.ALUA..MYC........GFRZ0.0	TEST DLA
117	ROM SNPLA./100...CBIO.MYC.QYC.....SEQBUS...0	RT3S
118	ROM ./0EC.AWR2.APB....SYD.....BUSR..0	RT3B UPDATE STACK
119	ROM ./1F3.AWR2.AMB..........GFSTOV.0	STD
11A	ROM ./1F2.AWR2.AMB..........GFSTOV.0	STDP
11B	ROM ./1E9.ARR1.ALUA.........BUSR.GCRVML.CRLOG	SLA CR
11C	ROM FLAG./1B5.ARR1.ALUA...........0	SLN TEST NORM
11D	ROM ./13A.AWR2.BSHR...........0	SLN RESULT
11E	ROM ./1EC.AW1215.DBIO.......RBUS.SEQBIO...0	KEYS IN (RCP) LR
11F	ROM ./1FF.AR1215.ALUA..MYC........GFKYZ0.0	LOAD OR READ R
120	ROM ./009.........RBUS...GBOK.0	VERIF MAN. REG L
121	ROM FLAG./1A5.ATEN.TWOA.CALU.MYC...PYD......0	SRN
122	ROM ./18B.AWR1.ASHR...SRQ...CTP1..REPEAT..GCRDSR.0	SRLC
123	FTA ARA1.ALUA.CRLOG	ML DSH
124	ROM ./0DA....MYQ.........0	DLA END
125	ROM ./0D7.AWA2.BSHR.CALU.MYC........GCRFNU.0	DLA END
126	ROM ./019..BINV..MYC.........0	ROUT.AFFICH.INCR
127	ROM ETAT./07E..ALUB.CALU..QYC.....SEQBUS...0	DISPLAY INCR
128	ROM ./1E9.ARA1.ALUA.........BUSR.GCRVML.CRLOG	DLA END
129	ROM ./164.AEP.ASHR.CALU.MYC.........0	DLN.DRN END
12A	ROM ./041.ARA1.ACR.CLUR.MYC.........0	TEST RB
12B	ROM FLAG./034.ARA2.ALUA..........GCRFNU.0	TEST DLA
12C	ROM ./043..BCR....SYD...WBUS....0	TEST TMP-TPM
12D	ROM ./0CE..ZERO...SRQ.........0	DRA
12E	ROM ./115.ATWO.TWOA.CALU.MYC...PM2......0	TRAP CORR LONG EX.
12F	ROM ./115.ATWO.TWOA.CALU.MYC.........0	TRAP
130	ROM ./0BF.............GFRZ0.0	VERIF MAN. REG M
131	ROM ./0CD....MYQ.........0	DSH
132	ROM ./0DC.AWA2.ALUB.........BUSR.GCRFNU.0	DSH
133	ROM ./038....MYQ.........0	TEST Q.CHARG NO.
134	ROM ./0CA.AEN.ALUA.CALU.MYC...PYD.CTP1.....0	MLRI
135	ROM ./103.AWR2.APB....SYD.PM2....BUSR..0	MLRI
136	ROM ./0E9.............0	TEST DLA
137	ROM ./0C7.AEP.APB.CALU.MYC....CTP1.....0	MLK
138	ROM ./0C6.AEN.ALUA.....PYD......0	ML
139	ROM ./1C3.ARR2.ALUA.CALU..QYC..PM2....BUSR..0	ML
13A	ROM ./0C4.AEN.ALUA.....PYD......0	MS
13B	ROM ./1B3.ARCT.ALUA.....PM2.CTP1.WMEM..BUSR..0	MS
13C	ROM ./0C2.AEN.ALUA.CALU..QYC..PYD......0	MSRD
13D	ROM ./1A3.ARCT.ALUA.....PM2.CTP1.WMEM..BUSR..0	MSRD
13E	ROM FLAG./00A.AEP.ALUA.......WMEM....0	TEST MEMOIRE NO2
13F	ROM ./053.ARA1.TWOA..MYC.QYC.SM2.PM2..WMEM....0	TEST MEMOIRE NO1

ADD		
140	ROM ./07E.........RBUS...GBOK.0	TEST MAN REG M
141	ROM ./1E9.AWR2.AMB.........BUSR.GFSTOV.0	UPD STK MSRD
142	ROM ./1CF.AWR1.ZERO.........BUSR..0	NGR
143	ROM ./101.AZ.AMB.......WMEM..BUSR..CRSUB	C2
144	ROM ./188..ALUB.......WBUS.SEQBIO...CRIO	CIO OTR
145	ROM ./087.ARA2.ALUA.CALU..QYC........0	MU- MUL.TOR IN Q REG.
146	ROM FLAG./01C.ATWO.APB..MYC........GCRFNU.0	TEST NO 1
147	ROM ./018.....SLQ.........0	TEST NO 1
148	ROM ./086.AWA1.MULTI...SRQ...CTP1..REPEAT...0	MU- ALGORITHM
149	ROM ./085.AWA1.MULTI..MYQ........GMULTI.0	MULTI 16TH PASS
14A	ROM ./084.AWA2.BSHR...........0	MULTI STORE LSB OF PROD.
14B	ROM ./007.ARA2.ALUA..........GCRFNU.0	MULTI UPDATE FNU
14C	ROM ./0AD..ALUB...SRQ.SP2....SEQBUS.BUSR.GBTMF.0	FPP SINGLE RD MA
14D	ROM ./042......SP2....SEQBUS.BUSR.GBTMF.0	FPP OP/S DOUBLE READ M1
14E	ROM ./053.ATWO.ASHR..MYC.QYC.SM2.PM2..WMEM....0	T. MEMOIRE NO1
14F	ROM ./06C.AWA1.ALUB....SM2.PM2......0	TEST MEMOIRE NO1
150	ROM ./09F.............GFRZ0.0	TEST Q.CHARG.NO
151	ROM ./0A1.AWA1.BCR..MYC.QYC........0	TEST DLA
152	ROM FLAG./030....MYQ..SP2....SEQBUS.BUSR.GBTMF.0	FPP READ LAST MA
153	ROM ./173.ARA0.TWOA....SYD.......0	FPP OPS WAIT.LD S WITH 1ST AD.
154	ROM ./010..BINV.CALU..QYC.SP2...WEXM.SEQBUS.BUSR.GBOF.0	FPP/S SI.
155	ROM ./010......SP2...WEXM.SEQBUS.BUSR.GBOF.0	FPP/S DOUBLE ST M1
156	ROM ./0E9.............0	TEST DLA
157	ROM ./0A7.ARA0.AOB....SYD...RBUS..BUSR.GBTMP.0	INR
158	ROM ./0A6.AWR1.DBIO.CIOR.MYC......SEQBUS..GCSEL.CRIO	INR
159	ROM ./188.AWR1.AOB...SLQ........0	INR TST SST
15A	ROM ./0A4.AWA1.ALUA..........GCRVZ0.0	DIV MEMO SIGNE DIVD
15B	ROM ./0A3.AWA1.DIVSH...SLQ...CTP1....GCRDSR.0	DIV 1ST PASS
15C	ROM ./0A2.AWA1.DIVSH...SLQ...CTP1..REPEAT...0	DIV PROCESS
15D	ROM FLAG./1B6.AWA1.DIVALU...SLQ.......GCRFNU.0	DIV 16TH PASS
15E	ROM ./0A0.ATWO.APB.CLUR.MYC...PYD......0	TEST DLA
15F	ROM ./091.AWA2.BCR...SRQ........0	TEST DLA
160	ROM ./039.........RBUS...GBOK.0	TEST Q.CHARG NO.
161	FTA AWA2.ALUB.0	DIV ST CORTD QUOT
162	ROM ./09F..............0	TMP TEST
163	ROM ./033.AZ.ALUA..MYC.........0	TMP TEST
164	ROM ./09A.AWA1.DBIO.......RBUS.SEQBIO?.GBOF.0	FFX LD A1
165	ROM ./17D.........RBUS..BUSR.GBOF.0	FFX RESET BSY
166	ROM ./022.AWCT.ALUB......CTP1.....0	TEST NO 3
167	ROM ./023.AWCT.ALUB...SLQ...CTP1.....0	TEST NO 3
168	ROM ETAT./0DE..........SEQBUS...0	VERIF MAN REG L
169	ROM FLAG./09C.APSW.AANDB..........GCRFNU.0	TEST TMP-TPM
16A	ROM ./030.ARA2.ALUA.......WBUS.SEQBUS.BUSR.GBTMF.0	FFL LD M1
16B	ROM ./093.AWA2.TWOA..........GCRFNU.0	DA
16C	ROM ./092.AWA1.DADD.........BUSR..CRADD	DA
16D	FTA AWA2.ASHR.0	DAS END
16E	ROM ./090.AEP.TWOA..MYC.........0	TEST DLA
16F	ROM ./081.AEP.APB..MYQ...PYD......0	TEST DLA
170	ROM ./019..BSHR.CALU.MYC.........0	ROUT.AFFICH.INCR
171	ROM ./152.AEP.ALUA.CBIO.MYC..SYD....SEQBUS...0	DAR* DA
172	ROM ./1F7.AEP.ALUA.CBIO.MYC..SYD....SEQBUS.BUSR..0	EL
173	ROM ./088.AEP.ALUA.CIOR..QYC.SYD....SEQBUS...0	CC
174	ROM ./189.AWA2.TWOA..........GCRFNU.0	DS
175	ROM ./142.AEP.ALUA.CBIO.MYC..SYD....SEQBUS...0	DSR
176	ROM ./0E9.............0	TEST DLA
177	ROM ./087.AWA0.ALUB..MYQ.......BUSR..0	CW CA
178	FTA ARA0.AMB.CRCMP	CW CA
179	ROM ./083.AWR1.BCR.CIOR.MYC......SEQBUS...0	LC
17A	ROM ./027..ZERO..MYQ.SRQ........0	TEST NO 2
17B	ROM ./026..ALUB..MYQ...PYD......0	TEST NO 2
17C	ROM ./1C8.AEP.ALUA....SYD.....BUSR..0	LC
17D	FTA AWR1.AOB.0	LC END
17E	ROM ./080.AEP.APB.....PYD..WBUS....0	TEST DLA
17F	ROM ./18E.AWA0.ZERO........SEQBIO..GFETCH.0	TEST DLA

Table 2-4b contd.

ADD		
180	ROM ./028....MYQ.....RBUS...GBOK.0	DISPLAY INCR
181	ROM ./020...CBIO.MYC.....SEQBUS...0	VERIF MAN REGM
182	ROM ./050.ATEN.TWOA.CALU.MYC.....0	(P856 ROUT AFFICH)
183	ROM ./0E9.....0	ROUT.AFFICH.INCR
184	ROM ./07A.ARR1.ALUA.....WBUS..BUSR.GBTME.0	WER
185	ROM ./188.ARR1.ALUA.....WBUS.SEQBUS...0	WER
186	ROM FLAG./054.AR15.AMB...SRQ.....GCRFNU.0	TEST NO 3
187	ROM FLAG./064.ARCT.AMB...SLQ...CTP1....GCRFNU.0	TEST NO 3
188	ROM ./076.AWR2.APB....SYD.....BUSR..0	RTN
189	ROM SNPLA./100..DBIO....SM2.PYD...SEQBUS.BUSR..0	RTN
18A	ROM ./09F.....0	TEST NO 2
18B	ROM ./018..ZERO...SRQ..PM2.....0	TEST NO 2
18C	ROM ./072.ATWO.APB.CALU.MYC.....GFENB.0	COMPUTE MASK RTNA15
18D	ROM ./06E.AWA0.BINV..MYQ.....0	COMPUTE MASK RTNA15
18E	ROM FLAG./024.ARA1.AXB.....GCRFNU.0	TEST DLA
18F	ROM ./061.ATWO.APLB1..MYC.....0	TEST RB
190	ROM ./019..BINV..MYC.....0	ROUT.AFFICH.INCR
191	ROM ./18E.ARA0.A0B.CLUR.MYC.QYC.....0	MASK STACK PSW RTNA15
192	ROM ./09F.....0	TEST MEMOIRE NO1
193	ROM FLAG./002...CBIO.MYC.....SEQBUS...0	TEST MEMOIRE NO1
194	ROM ./06A.AWR1.AMB....SYD.....GFSTOV.0	CF.15R2
195	ROM ./068.APSW.ALUA....SP2...WMEM..BUSR..0	CF
196	ROM ./0E9.....0	TEST DLA
197	ROM ./067.AEP.ALUA..MYQ..SP2...WMEM.SEQBUS.BUSR..0	CF
198	ROM ./1E9..ALUB....SYD.PYD..SEQBUS.BUSR..0	CF END
199	ROM ./05E..BSHR.CALU.MYC.....0	EX
19A	ROM ./09F.....0	TEST NO 3
19B	ROM FLAG./078....MYQ.....0	TEST NO 3
19C	ROM FLAG./05C.AEP.AXB....SM2.PM2.....GCRFNU.0	TEST MEMOIRE NO2
19D	ROM ./0FB.....RBUS...GBOK.0	TMP TEST
19E	ROM ./060.AWA0.BCR..MYC.....0	TEST RB
19F	ROM ./051.AEP.APB..MYC...PYD..WBUS....0	TEST RB
1A0	ROM FLAG./13A.AWA0.ALUB..MYQ...PM2.....0	MVF TEST LGHT=0
1A1	ROM FLAG./174.ATEN.AXB.....GCRFNU.0	EX TEST IF T2
1A2	ROM ./09F.....0	TEST MEMOIRE NO2
1A3	ROM FLAG./062...CBIO.MYC.....SEQBUS...0	TEST MEMOIRE NO2
1A4	ROM ./05A.ARR2.AMB.CALU.MYC.....0	MVF LGHT-2 IN M
1A5	ROM ./128.AWA1.APB..MYQ..SYD.....BUSR..0	MVF A1=SOURCE
1A6	ROM ./096.ATWO.ACR.CALU.MYC.....WBUS.SEQBIO..GFKYZO.CRIO	TMP T
1A7	ROM FLAG./058.....SLQ....WBUS...CBTMP.0	TEST TMP TPM
1A8	ROM FLAG./12A.AWA1.AMB....SYD....SEQBUS..GMOVE.0	MVF WRITE DEST
1A9	ROM ./13A.AWR2.ZERO.....0	MVF CLEAR LGHT
1AA	ROM ./09F.....0	TEST NO 3
1AB	ROM ./013.AWA2.FORA.....0	TEST NO 3
1AC	ROM FLAG./052..ALUB....SM2.PM2..WMEM.SEQBUS...0	TEST MEMOIRE NO1
1AD	ROM ./0B0.ARA0.ALUA....SYD.PYD.....0	TEST MEMOIRE NO1
1AE	ROM SNPLA./1FF.AWA1.ALUB.CIOR.MYC.QYC..PM2..SEQBIO..GFETCH.0	TRB
1AF	ROM ./0B1.AWA0.BCR....SYD.PYD.....GFRZO.0	(P856 TEST MEM NO1)
1B0	ROM ./058.ATWO.ALUA.CALU.MYC.QYC.....0	MVF
1B1	ROM ./046.AWA0.BSHR..MYQ.....0	RER
1B2	ROM FLAG./03C..BSHR..MYC.....GCRFNU.0	ROUT.AFFICH.INCR
1B3	ROM FLAG./0B8.ATWO.A0B..MYC.QYC.....GFRZO.0	TEST NO 1
1B4	ROM FLAG./0F2.AWA0.ALUB.....PM2.....0	MVB TEST LENGTH
1B5	ROM FLAG./10B.AWA2.AMB.....0	MVB PREPARE A2
1B6	ROM ETAT./0BE.....SEQBUS...0	VERIF MAN. REG M
1B7	ROM FLAG./02B..ALUB..MYQ...PM2..WMEM..BUSR..0	MVB PREPARE WRITE
1B8	ROM ./162..ALUB.....WMEM..BUSR..0	INT
1B9	ROM ./03A.ARA0.A0B....SYD...RBUS..BUSR.GBTME.0	RER
1BA	ROM ./09F.....0	TEST NO 3
1BB	ROM ./01A..ZERO...SRQ.....0	TEST NO 3
1BC	ROM ./058.ATEN.ALUA.CALU..QYC....WBUS.SEQBIO..GFETCH.0	TEST TMP
1BD	ROM ./083.....SP2....SEQBUS.BUSR.GBTMF.0	FPP DOUBLE LD 2ND WORD
1BE	ROM ./040..BCR..MYC.....GFKYZO.0	TEST RB
1BF	ROM FLAG./014.AEP.AXB..MYQ.....GCRFNU.0	TEST RB

ADD		
1C0	ROM ./1E8.....RBUS...GBOK.0	VERIF MAN. PUPIT
1C1	ROM ./037.AWA1.AMB.....0	DER MVF REST A1
1C2	ROM FLAG./02C..BSHR..MYC.QYC.....GCRFNU.0	ROUT.AFFICH.INCR
1C3	ROM ./085.ATWO.ACR..MYC.QYC.....GFRZO.0	TEST NO 2
1C4	ROM FLAG./0F1.AWR2.ALUB..MYQ.....0	DER MOVE REST R2
1C5	ROM ./188.AWR1.DBIO.CBIO.....SEQBUS...CRRTN	RER
1C6	ROM ./0CC...CBIO..QYC.....SEQBUS...0	TEST 0.CHARG NO.
1C7	ROM ./029..ALUB.CLUR.MYC.....WBUS....0	TEST 0.CHARG NO.
1C8	ROM ./036.AWA2.AMB.....0	DER MVF REST A2
1C9	ROM ./038.ATWO.APB.CALU.MYC.....0	DER MOVE M=LGTH
1CA	ROM ./09F.....0	TEST DLA
1CB	ROM ./071.ATWO.ASHR..MYC.....0	TEST DLA
1CC	ROM ./07F..BINV...QYC.....0	TEST NO 2
1CD	ROM ./098.ATWO.ASHR..MYC.QYC.....GFRZO.0	TEST NO 3
1CE	ROM ./0AC.AWA0.ALUB.....SEQBUS..GFLOT.0	FPP OP/S LD EXP
1CF	ROM ./186.AEP.ALUA....SYD...SEQBUS..GFLOT.0	FPP OP LD EXP
1D0	ROM ./02F.....0	NOT USED
1D1	ROM ./06A.AWR1.AMB....SYD.....0	CF.15R2M
1D2	ROM FLAG./07C..BSHR..MYC.SRQ.....GCRFNU.0	ROUT.AFFICH.INCR
1D3	ROM ./032.ARA0.....GCTLD.0	TEST NO 3
1D4	ROM FLAG./0EA.AWA1.APB....SYD...SEQBUS..GMOVE.0	MVB WRITE
1D5	ROM FLAG./0EA.AWA1.APB....SYD...SEQBUS..GBEX.0	MVUS WRITE
1D6	ROM ETAT./09E.....SEQBUS...0	TEST 0.CHARG NO.
1D7	ROM FLAG./0D8..ALUB.CBIO..QYC...WBUS.SEQBUS...0	ROUT.AFFICH.INCR
1D8	ROM FLAG./084.ATEN.AXB.....GCRFNU.0	TEST NO 2
1D9	ROM ./017.AEP.AMB.....PYD.....0	TEST NO 2
1DA	ROM ./09F.....0	TEST DLA
1DB	ROM ./070.ATEN.TWOA..MYC.....0	TEST RB
1DC	ROM FLAG./098....MYQ.....0	TEST NO 3
1DD	ROM ./078.ATWO.ASHR..MYC.QYC.....0	TEST NO 3
1DE	ROM FLAG./0DC..BINV.....0	TEST NO 1
1DF	ROM ./049..ALUB.....WBUS....0	VERIF MAN. REG M
1E0	ROM ./100..ALUB.....PYD.....0	TRAP DLN
1E1	ROM FLAG./195.ARA1.ALUA.....0	DLN
1E2	ROM ./09F.....0	TEST NO 1
1E3	ROM ./021..BINV..MYC.....0	TEST NO 1
1E4	ROM FLAG./01A.....PM2.....0	TEST NO 2
1E5	ROM ./033....MYQ.....0	TEST NO 2
1E6	ROM FLAG./04C..BSHR..MYC.....GCRFNU.0	ROUT.AFFICH.INCR
1E7	ROM ./04C....MYQ.....0	TEST NO 1
1E8	ROM ./016.AEP.APB.CALU.MYC.SRQ.....0	TEST NO 2
1E9	ROM FLAG./074.ATEN.AXB.....GCRFNU.0	TEST NO 2
1EA	ROM ./09F.....0	TEST RB
1EB	ROM ./032.ATEN.ASHR.CALU.MYC.....0	TEST RB
1EC	ROM ./012.ATEN.ALUA..MYC.QYC.....0	TEST NO 3
1ED	ROM FLAG./044.ARA2.AMB...SRQ.....GCRFNU.0	TEST NO 3
1EE	ROM ./1E9.AEP.ALUA....SYD....SEQBUS...CRFLO	FPP STORE ST EXP
1EF	ROM FLAG./010....SLQ.SP2...WEXM.SEQBUS.BUSR.GBOF.0	FPP ST MANTI.
1F0	ROM ./100..ALUB.....PYD.....0	TRAP DRN
1F1	ROM FLAG./185.AWA1.ASHR...SRQ.....GCRDSR.0	DRN
1F2	ROM ./09F.....0	TEST NO 1
1F3	ROM ./07F.....0	TEST NO 1
1F4	ROM ./0C1.....SM2.PM2...SEQBUS...0	TEST MEMOIRE NO2
1F5	ROM ./063..ALUB....SYD.PYD.....0	TEST MEMOIRE NO2
1F6	ROM ./097..DBIO.....WBUS.SEQBUS...0	VERIF MAN REG L
1F7	ROM ./0B8.ARR1.ALUA.CALU.MYC.....WBUS..BUSR.GBTMP.0	CIO QTR
1F8	ROM ./036.AEP.ALUA.CALU.MYC.....GCTLD.0	DER MVB READ
1F9	ROM ./007.AWA1.AMB.....PP2.....GCTLD.0	DER MVB WRITE
1FA	ROM ./03E.AEP.ALUA.CALU.MYC.....GCTLD.0	DER MVF READ
1FB	ROM ./005.AWA1.APB.....PP2.....CCTLD.0	DER MVF WRITE
1FC	ROM FLAG./06C.ARA1.AXB....SM2.PM2.....GCRFNU.0	TEST MEMOIRE NO1
1FD	ROM FLAG./0C0.ARA0.ALUA.CALU.MYC..SYD.PYD.....0	TEST MEMOIRE NO1
1FE	ROM ./120.ATWO.TWOA.CALU.MYQ.QYC.....GCTLD.0	PAGE FAULT ML
1FF	ROM ./125.ATWO.TWOA.CALU..QYC.....GCTLD.0	PAGE FAULT

Ta 2-5A Control-ROM Binary Content Pc

ADD.	SNA	NAN	A	ADL	C	M	Q	S	P	CT	B	SEQ	R	GP	CR
000	00	1111101000	00011	00001	00	10	11	00	00	0	111	00	0	00000	00000
001	11	1111111111	00000	00000	11	10	11	10	11	0	000	10	0	11100	00000
002	00	1111101001	00000	00000	00	00	00	10	11	0	000	00	1	00000	00000
003	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
004	01	1111111000	11110	10010	00	00	11	00	00	0	000	00	0	00000	00000
005	00	1111111011	00000	00000	00	00	00	11	10	0	000	00	0	01110	00000
006	00	1111111111	10100	00011	00	10	00	00	00	0	000	00	0	00000	00000
007	00	1111111111	00000	01110	01	10	00	00	00	0	000	10	0	00000	00000
008	11	1111111111	01100	00001	11	10	11	10	11	0	000	10	0	11100	10000
009	00	1111101001	00000	00001	00	00	00	01	01	0	000	00	1	00000	10000
00A	00	1011011011	11110	00011	00	00	00	00	00	0	111	00	0	00000	00000
00B	00	1111111111	00000	00011	00	10	00	00	00	0	000	00	0	00000	00000
00C	00	1000000001	00100	00011	00	00	00	00	00	0	011	00	1	00000	00000
00D	00	1000000001	10100	00011	00	00	00	00	00	0	011	00	1	00000	00000
00E	00	0111001110	11011	00011	00	10	00	00	00	0	000	00	0	00000	00000
00F	00	0111001011	11011	00011	00	10	00	00	00	0	000	00	0	00000	00000
010	01	1110100000	11110	00011	00	00	11	00	00	0	000	00	0	00000	00000
011	00	1111101001	00000	00001	00	00	00	01	01	0	000	00	1	00000	00000
012	01	0111000000	01000	00001	00	00	00	00	00	0	100	00	0	10011	00000
013	00	0111000000	00000	00011	00	00	00	01	01	0	000	00	0	00000	00000
014	00	1110110000	11011	10010	00	10	00	00	00	0	000	00	0	00000	00000
015	00	1110110000	11011	10010	00	10	00	00	10	0	000	00	0	01110	00000
016	11	1111111111	00000	00000	11	10	11	10	11	0	000	10	0	11100	00000
017	11	1111111110	00000	00000	00	00	00	00	00	0	000	10	0	00001	00000
018	01	1100101011	10100	00011	00	10	00	00	00	0	000	00	0	01111	00000
019	01	1010111011	10100	00011	00	10	01	00	00	0	000	00	0	01111	00000
01A	01	1011111011	00100	00011	00	00	11	00	00	0	000	00	0	00000	00000
01B	00	0110011110	01001	10001	00	00	01	00	00	1	000	01	0	00110	00000
01C	01	1011101011	10100	00011	00	10	00	00	00	0	000	00	0	00000	00000
01D	01	1010011011	10100	00011	00	10	01	00	00	0	000	00	0	00000	00000
01E	00	0110111101	00100	00011	00	00	11	00	00	0	000	00	0	00000	00000
01F	00	0110011110	01001	01111	00	00	10	00	00	1	000	01	0	00011	00000
020	11	1111111111	01100	00110	11	10	11	10	11	0	000	10	0	11100	10100
021	00	1111101001	10100	00110	00	00	00	01	01	0	000	00	1	00000	10100
022	00	0111101100	00101	00011	00	00	00	01	00	0	000	00	1	00000	00000
023	00	0111101000	00101	00011	00	00	00	01	00	0	000	00	1	00000	00000
024	00	1000000001	00100	00110	00	00	00	00	00	0	011	00	1	00000	10100
025	00	1000000001	10000	00100	00	00	00	00	00	0	011	00	1	00000	10100
026	00	1011101111	11011	10010	00	10	00	00	00	0	000	00	0	00000	00000
027	00	1100111110	01011	00000	00	00	01	00	00	0	000	00	0	01011	00000
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029	00	0111000011	11010	10010	00	10	11	00	01	0	000	00	0	00000	00000
02A	00	1010111001	11010	01011	00	10	11	00	00	0	000	00	0	00000	00000
02B	00	1010001011	10100	00011	00	00	00	01	00	0	100	00	1	10011	00000
02C	01	1110100010	01111	01110	00	11	00	11	10	1	000	10	0	00000	00000
02D	00	0110111100	00000	00001	00	00	00	01	01	0	000	00	1	00000	00000
02E	00	1001101000	00000	00000	10	10	00	00	00	0	000	00	0	00110	00000
02F	01	1110000000	11100	00011	00	00	11	00	00	0	000	00	0	00000	00000
030	11	1111111111	01100	00000	11	10	11	10	11	0	000	10	0	11100	11000
031	00	1111101001	10100	00000	00	00	00	01	01	0	000	00	1	00000	11000
032	10	1000000000	00000	00000	01	10	11	10	11	0	000	10	0	00000	00000
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035	01	0101111000	11000	00011	00	00	00	00	00	0	000	00	0	00100	00000
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037	11	1111111111	01100	00010	11	10	11	10	11	0	000	10	0	11100	00000
038	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
039	00	0110111110	00100	00011	00	00	11	00	00	0	000	00	0	00000	00000
03A	01	1110001100	00000	01101	00	10	00	00	00	0	000	00	0	00100	00000
03B	11	1111111111	10100	00011	00	00	00	01	00	0	000	00	0	00000	00000
03C	01	1110000010	01111	01110	00	00	00	10	10	1	000	10	0	00101	00000
03D	00	0110111100	00000	00001	00	00	00	01	01	0	000	00	1	00000	00000
03E	00	1010111111	11011	01011	00	00	00	01	01	0	000	00	0	00000	00000
03F	01	1101100000	00000	00000	00	00	01	00	00	0	100	00	0	10011	00000
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041	01	1110010000	10110	01000	00	10	00	00	00	0	000	00	1	00000	00000
042	00	0111111101	00000	00000	01	10	00	00	11	0	000	10	0	00000	00000
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04D	00	1111101001	00000	00001	00	00	00	01	01	0	000	00	1	00000	00000
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05B	01	1101001101	01100	01111	00	00	10	00	11	0	000	00	0	00000	00000
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05F	00	1111111111	10110	00001	00	10	00	00	00	0	000	00	0	00000	00000
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079	00	1010100000	11011	01111	00	00	11	00	00	0	000	00	0	11000	00000
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07B	01	1100001101	01001	01111	00	00	10	00	11	0	000	00	0	00011	00000
07C	00	0110001101	10100	00011	00	10	00	00	00	1	000	00	0	00000	00000
07D	00	1010011000	11011	01111	00	00	11	00	00	0	001	00	0	10101	00000
07E	00	0110001011	10100	00011	00	10	00	00	00	1	000	00	0	00000	00000
07F	01	1111110100	00000	01001	00	00	11	00	00	0	000	00	0	00100	00000
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099	00	0101001001	00010	10010	00	00	11	00	00	0	000	00	0	00000	00000
09A	00	0100101011	00001	00011	00	00	00	00	00	0	111	00	1	11001	00000
09B	00	0111111110	01101	00001	00	00	00	00	00	0	000	00	0	00000	00000
09C	01	0101100111	11011	01111	00	10	00	00	00	0	000	00	1	11001	00000
09D	00	1010000011	10100	00011	00	10	00	00	00	0	111	00	1	00110	00000
09E	00	1011000000	10100	00011	00	10	00	00	00	0	000	00	0	11010	00000
09F	00	0100111011	00000	00000	00	00	00	00	00	0	100	00	0	10100	01100
0A0	00	1110101101	00000	01010	00	00	00	01	00	0	000	00	0	01001	00000
0A1	00	1111101001	10100	00110	00	00	00	01	01	0	000	00	1	00000	00000
0A2	00	0111001111	11011	00011	00	10	00	00	00	0	000	00	0	00000	00000
0A3	10	1000000000	00101	00011	00	00	11	01	00	0	000	00	0	00000	00000
0A4	00	0110111011	01001	10001	00	00	01	00	00	1	000	01	0	00000	00000
0A5	01	0000111111	11011	00011	00	00	00	01	00	0	000	00	0	00000	00000
0A6	00	1010101101	00000	01101	00	10	00	00	10	0	000	00	0	00000	00000
0A7	00	0110011011	10100	00011	00	00	11	00	00	0	000	00	0	00000	00000
0A8	00	0100011101	00000	00000	00	00	00	00	00	0	000	00	1	10010	00000
0A9	00	0100011110	00000	00000	01	00	11	10	00	0	000	10	1	00000	00000
0AA	00	1010011111	00000	01101	00	10	00	00	00	0	000	00	0	00000	00000
0AB	00	1010100010	00000	00000	01	10	00	10	11	0	000	10	0	00000	00000
0AC	00	1000000001	00100	00011	00	00	00	00	00	0	011	00	1	10010	00000
0AD	00	0100101001	01010	00110	00	11	11	00	00	0	000	00	0	00000	00000
0AE	00	1111101001	10100	00011	00	00	00	01	00	0	000	10	0	00000	00000
0AF	01	1010100000	00000	00000	00	00	01	10	00	0	000	10	1	11000	00000
0B0	00	1011001101	00000	01101	00	10	00	00	00	0	000	00	0	00000	00000
0B1	00	1111101001	10100	00000	00	00	00	01	01	0	000	00	1	00000	00000
0B2	01	1011100000	10010	00110	00	10	00	00	00	0	000	00	1	00000	00000
0B3	10	1000000000	00000	00000	00	00	00	00	11	0	000	00	0	00000	00000
0B4	00	0110100010	01001	01111	00	00	10	00	00	1	000	01	0	00011	00000
0B5	01	0000001111	11011	00011	00	00	00	00	01	0	000	00	0	00000	00000
0B6	00	1111101001	10100	00011	00	00	00	00	00	0	000	10	0	00000	00000
0B7	01	1010010000	00000	00000	00	00	01	10	00	0	001	10	1	10101	00000
0B8	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
0B9	00	0100010101	00000	00000	01	00	11	10	00	0	000	10	1	00000	00000
0BA	00	1111101001	01011	01110	00	00	00	00	00	0	000	10	0	00000	00000
0BB	00	1010000010	00000	00000	01	10	00	10	11	0	000	10	0	00000	00000
0BC	00	1001111101	00000	01101	00	00	00	01	00	0	000	10	0	00000	00000
0BD	00	0100010111	01010	00000	00	11	11	00	00	0	000	00	0	00000	00000
0BE	00	0100111110	10000	01100	00	10	00	00	00	0	000	00	1	00101	00100
0BF	00	1111101001	01010	00001	00	00	00	00	00	0	000	00	1	00101	10000

Table 2-5A contd.

ADD.	SNA	NAN	A	ADL	C	M	Q	S	P	CT	B	SEQ	R	GP	CR
0C0	11	1111111111	01100	00001	11	10	11	10	11	0	000	10	0	11100	00000
0C1	00	1111101001	00000	00001	00	00	00	01	01	0	000	00	1	00000	00000
0C2	00	1001101101	00000	01001	00	00	00	00	00	0	000	00	1	01100	00000
0C3	00	0111101110	00000	00000	01	10	00	00	11	0	000	10	0	00000	00000
0C4	00	0010011111	01010	00110	00	00	00	00	00	0	000	00	0	00000	00000
0C5	00	1111101001	00000	00011	00	00	00	01	01	0	000	00	1	00000	00000
0C6	00	0100010000	00100	00011	00	00	00	11	00	0	000	00	0	00000	00000
0C7	11	1111111111	00100	00000	11	10	11	10	11	0	000	10	0	11100	11100
0C8	00	0100000110	00100	01011	10	10	00	00	00	0	000	00	1	10000	00000
0C9	11	1111111111	01100	01001	11	10	11	10	11	0	000	10	0	11100	00000
0CA	00	1111101001	00000	01110	00	00	00	01	01	0	000	10	1	00000	00000
0CB	00	1001100010	00000	00000	00	00	00	00	00	0	000	00	0	01001	00000
0CC	00	1000000001	00100	00011	00	00	00	00	00	0	011	00	1	10000	00000
0CD	00	1001111101	00000	01101	00	00	00	01	00	0	000	00	0	01110	00000
0CE	01	1001010000	00000	00110	10	10	01	00	00	0	000	00	0	00000	00000
0CF	00	1011011110	00000	00000	11	10	11	00	00	0	111	11	0	11100	00000
0D0	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
0D1	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
0D2	00	1001001011	01101	00001	00	00	00	00	00	0	000	00	0	00000	00000
0D3	10	1000000000	00000	01110	01	00	11	01	11	0	000	10	0	00000	00000
0D4	01	1000011011	01010	00000	01	10	00	01	00	0	000	10	0	00111	00000
0D5	00	0010010110	01001	00110	00	00	00	00	00	0	000	00	0	00000	00000
0D6	01	1001000000	00000	00000	00	00	01	00	00	0	000	00	0	00000	00000
0D7	01	0111110000	00000	01001	00	00	11	00	00	0	000	00	0	00000	00000
0D8	11	1111111111	00100	00000	11	10	11	10	11	0	000	10	0	11100	11100
0D9	11	1111111111	10100	00000	11	10	11	10	11	0	000	10	0	11100	11100
0DA	00	1001001001	10110	00011	00	10	00	00	00	0	000	00	0	01001	00000
0DB	00	1001000010	00011	00011	00	00	00	01	00	0	001	00	1	10101	00000
0DC	00	0100011001	00100	00011	10	10	00	00	00	0	000	00	1	10000	00000
0DD	00	1000111101	00000	00001	00	11	00	11	00	0	011	10	1	00000	00000
0DE	01	1000110000	00000	00000	00	00	01	00	00	0	000	00	0	00000	00000
0DF	01	0111110000	00000	01001	00	00	11	00	00	0	000	00	0	00000	00000
0E0	00	0011110111	00000	00001	00	00	00	01	00	0	000	00	0	00000	00000
0E1	01	1100101101	10100	00011	00	10	00	00	00	0	000	00	0	00000	00000
0E2	00	1000010111	11011	00110	00	10	00	11	00	0	001	10	1	10101	00000
0E3	00	0111101101	00000	00000	01	10	00	00	00	0	000	10	0	00000	00000
0E4	00	0010101111	00000	00001	00	11	00	00	10	0	011	00	1	00000	00000
0E5	00	0010101111	00000	00001	00	11	00	00	10	0	011	00	1	10010	00000
0E6	01	1000001000	00000	00000	00	00	01	00	00	0	000	00	0	00000	00000
0E7	01	0111110000	00000	01001	00	00	11	00	00	0	000	00	0	00000	00000
0E8	00	1001100101	01011	00000	11	10	00	00	00	0	100	11	0	01011	00000
0E9	00	1111101001	10100	00011	00	00	00	01	00	0	000	10	1	00000	00100
0EA	00	1000100000	11010	10010	00	00	11	00	10	0	000	00	0	00000	00000
0EB	00	0011100011	10100	00011	01	11	11	01	00	0	000	10	0	01100	00100
0EC	00	0001010110	11011	10010	00	10	00	00	00	0	000	00	0	00000	00000
0ED	01	1001100000	01000	00001	00	00	00	00	00	0	111	00	0	00000	00000
0EE	00	0011010111	11011	10010	00	10	00	00	00	0	000	00	0	00000	00000
0EF	00	1000011101	01011	00000	00	00	01	01	00	0	000	00	0	01011	00000
0F0	00	0010011110	11010	01011	00	10	00	00	00	0	000	00	0	00000	00000
0F1	01	0111101111	10100	00011	00	10	00	00	00	0	000	00	0	00000	00000
0F2	00	1000001101	10110	00011	00	00	01	10	00	0	011	00	1	01001	00000
0F3	00	1001011100	00000	01110	00	00	00	01	00	0	000	10	1	00000	00000
0F4	00	0111101011	00001	00011	00	00	00	01	00	0	000	00	1	00000	00000
0F5	00	0111101011	00001	00011	00	00	00	01	00	0	000	00	1	10010	00000
0F6	01	0111110000	00000	01001	00	00	11	00	00	0	000	00	0	00000	00000
0F7	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
0F8	00	1001001000	11000	00011	00	10	00	00	10	0	000	00	0	00000	00000
0F9	11	1111111111	01100	00101	11	10	11	10	11	0	000	10	0	11100	10000
0FA	00	1000001100	10100	00011	00	11	00	10	00	0	011	10	1	00000	00000
0FB	00	1000000011	00000	00001	00	00	00	01	00	0	000	10	0	00000	00000
0FC	00	1001101101	00000	00000	00	00	00	11	00	0	000	00	1	00000	00000
0FD	00	1000000001	00000	00101	00	00	00	00	00	0	011	00	1	00000	10000
0FE	00	1111101001	10100	00011	00	00	00	01	00	0	000	10	1	00000	00000
0FF	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
100	00	0001111111	00000	00000	00	00	00	00	00	0	000	00	0	01001	00000
101	00	1100110101	00000	00011	00	11	00	00	01	0	000	00	1	00000	00000
102	00	0111101100	00100	00110	00	00	00	01	00	0	000	00	1	00000	00000
103	00	1101011101	00100	00110	00	00	00	01	00	0	000	00	1	00000	00000
104	01	0110100011	00000	00000	01	10	00	00	00	0	100	11	0	00000	00000
105	01	0110101001	00000	00011	00	00	00	00	00	0	000	00	0	00100	00000
106	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
107	00	0011001110	00000	01101	00	10	00	00	00	0	000	00	0	00000	00000
108	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
109	00	0010001011	00100	00011	00	00	00	00	00	0	000	00	0	00000	00000
10A	00	0111101000	00101	00110	00	00	00	01	00	0	000	00	1	00000	00000
10B	00	1101011100	00101	00110	00	00	00	01	00	0	000	00	1	00000	00000
10C	00	1100010010	11011	00011	00	10	11	00	00	0	000	00	0	00000	00000
10D	00	1111101001	00000	00011	00	00	00	01	01	0	000	00	1	00000	00000
10E	00	1111101011	00000	00000	00	00	00	00	01	0	000	00	0	00000	00000
10F	00	1001001010	11011	10010	00	00	11	00	00	0	000	00	0	00000	00000
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111	10	1000000000	00101	00110	00	00	11	01	00	0	000	00	0	00000	00000
112	00	1001011100	00101	00110	00	00	00	01	00	0	000	00	1	00000	00000
113	10	1000000000	10100	00011	01	10	11	01	00	0	000	10	0	00000	00000
114	00	0010010000	01010	00110	01	10	00	01	00	0	000	10	0	00111	00000
115	00	0010101010	01010	00110	00	00	00	00	00	0	000	00	0	00000	00000
116	00	1010101110	11010	00011	00	10	00	00	00	0	000	00	0	01101	00000
117	10	1000000000	00000	00000	01	10	11	00	00	0	000	10	0	00000	00000
118	00	0111101100	10101	00110	00	00	00	01	00	0	000	00	1	00000	00000
119	00	1111110011	10110	10101	00	00	00	00	00	0	000	00	0	01011	00000
11A	00	1111110010	01101	00000	00	00	00	00	00	0	000	00	0	01011	00000
11B	00	1111101001	00100	00011	00	00	00	00	00	0	000	00	1	00100	10000
11C	01	1101101010	00100	00011	00	00	00	00	00	0	000	00	0	00000	00000
11D	00	1001110101	01101	01101	00	00	00	00	00	0	000	00	0	00000	00000
11E	00	1111011100	01110	01110	00	00	00	00	00	0	100	11	0	00000	00000
11F	00	1111111111	00100	00011	00	10	00	00	00	0	000	00	0	01110	00000
120	00	0000001001	00000	00000	00	00	00	00	00	0	100	00	0	10011	00000
121	01	1101001001	11010	10010	00	10	00	00	00	0	000	00	0	00000	00000
122	00	1100001011	01100	01111	00	00	10	00	00	1	000	01	0	00000	00000
123	11	1111111111	00001	00011	11	10	11	10	11	0	000	10	0	11100	10000
124	00	0110110110	00000	00000	00	11	00	00	00	0	000	00	0	00000	00000
125	00	1101010111	01010	01101	00	10	00	00	00	0	000	00	0	00100	00000
126	00	0000110001	00000	00101	00	10	00	00	00	0	000	00	0	00000	00000
127	11	0011111110	00000	00001	00	00	11	00	00	0	000	10	0	00000	00000
128	00	1111010001	00001	00011	00	10	00	00	00	0	000	00	1	10101	10000
129	00	1011001100	10100	01111	00	10	00	00	00	0	000	00	0	00000	00000
12A	00	0010000001	00001	01011	10	10	00	00	00	0	000	00	0	00000	00000
12B	01	0001101000	00010	00011	00	00	00	00	00	0	000	00	0	00100	00000
12C	00	0010000011	00000	01001	00	00	00	01	00	0	111	00	0	00000	00000
12D	00	0110011110	00000	01010	00	00	10	00	00	0	000	00	0	00000	00000
12E	00	1000101010	11011	10010	00	10	00	10	00	0	000	00	0	00000	00000
12F	00	1000101010	11011	10010	00	10	00	00	00	0	000	00	0	00000	00000
130	00	0101111111	00000	00000	00	00	00	00	00	0	000	00	0	01101	00000
131	00	0110011101	00000	00000	00	11	00	00	00	0	000	00	0	00000	00000
132	00	0110111000	01010	00001	00	00	00	00	00	1	000	00	0	00100	00000
133	00	0000111000	00000	00000	00	11	00	00	00	0	000	00	0	00000	00000
134	00	0110010110	11000	00011	00	10	00	00	00	1	000	00	0	00000	00000
135	00	1110100111	01101	00110	00	00	00	01	10	0	000	00	1	00000	00000
136	00	0111101001	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
137	00	0110001110	10101	00110	00	10	00	00	00	1	000	00	0	00000	00000
138	00	0110001110	11000	00011	00	00	00	00	10	0	000	00	0	00000	00000
139	00	1110000011	10101	00011	00	00	11	00	00	0	000	00	1	00000	00000
13A	00	0110001001	11000	00011	00	00	00	00	01	0	000	00	0	00000	00000
13B	00	1101100011	00111	00011	00	00	00	00	10	1	011	00	1	00000	00000
13C	00	0110000010	11000	00011	00	00	11	00	01	0	000	00	0	00000	00000
13D	00	1101000011	00111	00011	00	00	00	00	10	1	011	00	1	00000	00000
13E	01	0000010110	10100	00011	00	00	00	00	00	0	011	00	0	00000	00000
13F	00	1010010111	00001	10010	00	10	11	11	10	0	011	00	0	00000	00000
140	00	0011111110	00000	00000	00	00	00	00	00	0	100	00	0	10011	00000
141	00	1111101001	01101	00000	00	00	00	00	00	0	000	00	1	01011	00000
142	00	1110011111	01100	01010	00	00	00	00	00	0	000	00	1	00000	00000
143	00	1000000001	10000	00000	00	00	00	00	00	0	011	00	1	00000	11000
144	00	1100010000	00000	00001	00	00	00	00	00	0	111	11	0	00000	01000
145	00	0101101111	00010	00011	00	00	11	00	00	0	000	00	0	00000	00000
146	01	0000011000	11011	00110	00	10	00	00	00	0	000	00	0	00100	00000
147	00	0000011000	00000	00000	00	00	01	00	00	0	000	00	0	00000	00000
148	00	0101101101	01001	10100	00	00	10	00	00	1	000	01	0	00000	00000
149	00	0101101101	01001	10100	00	11	00	00	00	0	000	00	0	11101	00000
14A	00	0101101001	01010	01101	00	00	00	00	00	0	000	00	0	00000	00000
14B	00	0110101111	00010	00011	00	00	00	00	00	0	000	00	0	00100	00000
14C	00	0101101101	00000	00001	00	00	10	00	00	0	000	10	1	11001	00000
14D	00	0010000010	00000	00000	00	00	00	00	10	0	000	10	1	11001	00000
14E	00	1001010011	11011	01111	00	10	11	11	10	0	011	00	0	00000	00000
14F	00	0011010010	01001	00001	00	00	00	11	10	0	000	00	0	00000	00000
150	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	01101	00000
151	00	0101000011	01001	01001	00	10	11	00	00	0	000	00	0	00000	00000
152	01	0001100000	00000	00000	00	11	00	00	00	0	000	10	1	11001	00000
153	00	1011100011	00000	10010	00	00	00	01	00	0	000	00	0	00000	00000
154	00	0000010000	00000	00101	00	00	11	10	00	0	001	10	1	10100	00000
155	00	0000010000	00000	00000	00	00	00	10	00	0	001	10	1	10100	00000
156	00	0111101001	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
157	00	0101000111	00000	00010	00	00	00	01	00	0	100	00	1	10111	00000
158	00	0101000110	01100	01110	11	10	00	00	00	0	000	10	0	00110	01000
159	00	1100010000	01100	00010	00	00	01	00	00	0	000	00	0	00000	00000
15A	00	0101001001	01001	00011	00	00	00	00	00	0	000	00	0	01111	00000
15B	00	0101000010	11001	11110	00	00	01	00	00	1	000	00	0	00000	00000
15C	00	0101000010	01001	11110	00	00	01	00	00	1	000	01	0	00000	00000
15D	01	1101101010	01001	11100	00	00	01	00	00	0	000	00	0	00100	00000
15E	00	0101000000	11011	00110	10	10	00	00	01	0	000	00	0	00000	00000
15F	00	0100010001	01010	01001	00	00	10	00	00	0	000	00	0	00000	00000
160	00	0001110001	00000	00000	00	00	00	00	00	0	100	00	0	10011	00000
161	11	1111111111	01010	00001	11	10	11	10	11	0	000	10	0	11100	00000
162	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
163	00	0001110011	10000	00011	00	10	00	00	00	0	000	00	0	00000	00000
164	00	0100110110	01001	01110	00	00	00	00	00	0	100	11	0	10100	00000
165	00	1011111101	00000	00000	00	00	00	00	00	0	100	00	1	10100	00000
166	00	0001100010	01111	00001	00	00	00	00	00	1	000	00	0	00000	00000
167	00	0001100011	01111	00001	00	00	01	00	00	1	000	00	0	00000	00000
168	11	0110111110	00000	00000	00	00	00	00	00	0	000	10	0	00000	00000
169	01	0100111100	10110	01000	00	00	00	00	00	0	000	00	0	00100	00000
16A	00	0000110000	00010	00011	00	00	00	00	00	0	111	10	1	11001	00000
16B	00	0100100011	01010	10010	00	00	00	00	00	0	000	00	0	00100	00000
16C	00	0100100100	01001	11010	00	00	00	00	00	0	000	00	1	00000	10100
16D	11	1111111111	01010	01111	11	10	11	10	11	0	000	10	0	11100	00000
16E	00	0100100000	10100	10010	00	10	00	00	00	0	000	00	0	00000	00000
16F	00	0100000001	10100	00110	00	11	00	00	01	0	000	00	0	00000	00000
170	00	0000011001	00000	01101	00	10	00	00	00	0	000	00	0	00000	00000
171	00	1010100100	10100	00011	01	10	00	01	00	0	000	10	0	00000	00000
172	00	1111101111	10100	00011	01	10	00	01	00	0	000	10	1	00000	00000
173	00	0100010000	10100	00011	11	00	11	01	00	0	000	10	0	00000	00000
174	00	1100011001	01010	10010	00	00	00	00	00	0	000	00	0	00100	00000
175	00	1010000110	10100	00011	01	10	00	01	00	0	000	10	0	00000	00000
176	00	0111101001	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
177	00	0100001111	01000	00001	00	11	00	00	00	0	000	00	1	00000	00000
178	11	1111111111	00000	00000	11	10	11	10	11	0	000	10	0	11100	11100
179	00	0100000011	01100	01001	11	10	00	00	00	0	000	10	0	00000	00000
17A	00	0001001111	00000	01010	00	11	10	00	00	0	000	00	0	00000	00000
17B	00	0001100110	00000	00001	00	11	00	00	01	0	000	00	0	00000	00000
17C	00	1110010010	10100	00011	00	00	00	01	00	0	000	00	1	00000	00000
17D	11	1111111111	00100	00010	11	10	11	10	11	0	000	10	0	11100	00000
17E	01	0100000000	10100	00110	00	00	00	00	01	0	111	00	0	00000	00000
17F	00	1100011001	01000	01010	00	00	00	00	00	0	000	11	0	00100	00000

Table 2-5A contd.

ADD.	SNA	NAN	A	ADL	C	M	Q	S	P	CT	B	SEQ	R	GP	CR
180	00	0001010000	00000	00000	00	11	00	00	00	0	100	00	0	10011	00000
181	00	0001000000	00000	00000	01	10	00	00	00	0	000	10	0	00000	00000
182	00	0010100000	00000	00000	00	11	00	00	00	0	000	00	0	00000	00000
183	00	0111101001	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
184	00	0011111010	00100	00011	00	00	00	00	00	0	111	00	1	10110	00000
185	00	1100001000	00100	00011	00	00	00	00	00	0	111	10	0	00000	00000
186	01	0010101100	00011	00000	00	00	10	00	00	0	000	00	0	00100	00000
187	01	0011100100	00111	00000	00	00	01	00	00	1	000	00	0	00100	00000
188	00	0011110110	01101	00110	00	00	00	01	00	0	000	00	1	00000	00000
189	10	1000000000	00000	01110	00	00	00	11	01	0	000	10	1	00000	00000
18A	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
18B	00	0000011011	00000	01010	00	00	10	00	10	0	000	00	0	00000	00000
18C	00	0011110010	11011	00110	00	10	00	00	00	0	000	00	0	01010	00000
18D	00	0011101110	01000	00101	00	11	00	00	00	0	000	00	0	00000	00000
18E	01	0001001100	00001	00111	00	00	00	00	00	0	000	00	0	00100	00000
18F	00	0011100001	11011	00100	00	10	00	00	00	0	000	00	0	00000	00000
190	00	0000011001	00000	00101	00	10	00	00	00	0	000	00	0	00000	00000
191	00	1101111110	00000	00010	10	10	11	00	00	0	000	00	0	00000	00000
192	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
193	01	0000000010	00000	00000	01	10	00	00	00	0	000	10	0	00000	00000
194	00	0011101010	01100	00000	00	00	00	01	00	0	000	00	0	01011	00000
195	00	0011101000	10110	00011	00	00	00	10	00	0	011	00	1	00000	00000
196	00	0111101001	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
197	00	0011100111	10100	00011	00	11	00	10	00	0	011	10	1	00000	00000
198	00	1111101001	00000	00001	00	00	00	01	01	0	000	10	1	00000	00000
199	00	0010111110	00000	01101	00	10	00	00	00	0	000	00	0	00000	00000
19A	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
19B	01	0011111000	00000	00000	00	11	00	00	00	0	000	00	0	00000	00000
19C	01	0010111100	10100	00111	00	00	00	11	10	0	000	00	0	00100	00000
19D	00	0111111011	00000	00000	00	00	00	00	00	0	100	00	0	10011	00000
19E	00	0011100000	01000	01001	00	10	00	00	00	0	000	00	0	00000	00000
19F	00	0010100001	10100	00110	00	10	00	00	01	0	111	00	0	00000	00000
1A0	01	1001111010	01000	00001	00	11	00	00	10	0	000	00	0	00000	00000
1A1	01	1011110100	11010	00111	00	00	00	00	00	0	000	00	0	00100	00000
1A2	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1A3	01	0011100010	00000	00000	01	10	00	00	00	0	000	10	0	00000	00000
1A4	00	0010110110	00101	00000	00	10	00	00	00	0	000	00	0	00000	00000
1A5	00	1001010111	01001	00110	00	11	00	01	00	0	000	00	1	00000	00000
1A6	00	0100101110	11011	01011	00	10	00	00	00	0	111	11	0	01110	01000
1A7	01	0010111000	00000	00000	00	00	01	00	00	0	111	00	0	10111	00000
1A8	01	1001010101	01001	00000	00	00	00	01	00	0	000	10	0	00111	00000
1A9	00	1001111010	01101	01010	00	00	00	00	00	0	000	00	0	00000	00000
1AA	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1AB	00	0000100011	01010	10000	00	00	00	00	00	0	000	00	0	00000	00000
1AC	01	0010100010	00000	00001	00	00	00	11	10	0	011	10	0	00000	00000
1AD	00	0101100000	00000	00011	00	00	00	01	01	0	000	00	0	00000	00000
1AE	10	1111111111	01001	00001	11	10	11	00	10	0	000	11	0	11100	00000
1AF	00	0101100001	01000	00001	00	00	00	01	01	0	000	00	0	01101	00000
1B0	00	0010110111	11011	00011	00	10	11	00	00	0	000	00	0	00000	00000
1B1	00	0010000110	01000	01101	00	11	00	00	00	0	000	00	0	00000	00000
1B2	01	0001111100	00000	01101	00	10	00	00	00	0	000	00	0	00100	00000
1B3	01	0101111000	11011	00010	00	10	11	00	00	0	000	00	0	01101	00000
1B4	01	0111100010	01000	00001	00	00	00	00	10	0	000	00	0	00000	00000
1B5	01	1000001011	01010	00000	00	00	00	00	00	0	000	00	0	00000	00000
1B6	11	0101111110	00000	00000	00	00	00	00	00	0	000	10	0	00000	00000
1B7	01	0001010011	00000	00001	00	11	00	00	10	0	011	00	1	00000	00000
1B8	00	1011000010	00000	00001	00	00	00	00	00	0	011	00	1	00000	00000
1B9	00	0001111010	00000	00010	00	00	00	01	00	0	100	00	1	10110	00000
1BA	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1BB	00	0000110110	00000	01010	00	00	10	00	00	0	000	00	0	00000	00000
1BC	00	0010111000	11010	00011	00	00	11	00	00	0	111	11	0	11100	00000
1BD	00	0101100011	00000	00000	00	00	00	10	00	0	000	10	1	11001	00000
1BE	00	0010000000	00000	01001	00	10	00	00	00	0	000	00	0	01110	00000
1BF	01	0000101100	10100	00111	00	11	00	00	00	0	000	00	0	00100	00000
1C0	00	1111010000	00000	00000	00	00	00	00	00	0	100	00	0	10011	00000
1C1	00	0001110111	01001	00000	00	00	00	00	00	0	000	00	0	00000	00000
1C2	01	0001011100	00000	01101	00	10	11	00	00	0	000	00	0	00100	00000
1C3	00	0100001101	11011	01011	00	10	11	00	00	0	000	00	0	01101	00000
1C4	01	0111100011	01101	00001	00	11	00	00	00	0	000	00	0	00000	00000
1C5	00	1100011000	01100	01110	01	00	00	00	00	0	000	10	0	00000	00100
1C6	00	0110011100	00000	00000	01	00	11	00	00	0	000	10	0	00000	00000
1C7	00	0001011001	00000	00001	10	10	00	00	00	0	111	00	0	00000	00000
1C8	00	0001110110	01010	00000	00	00	00	00	00	0	000	00	0	00000	00000
1C9	00	0001111011	11011	00110	00	10	00	00	00	0	000	00	0	00000	00000
1CA	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1CB	00	0011110001	11011	01111	00	10	00	00	00	0	000	00	0	00000	00000
1CC	00	0011111111	00000	00101	00	00	11	00	00	0	000	00	0	00000	00000
1CD	00	0100111000	11011	01111	00	10	11	00	00	0	000	00	0	01101	00000
1CE	00	0101011100	01000	00001	00	00	00	00	00	0	000	10	0	11010	00000
1CF	00	1101111000	10100	00011	00	00	00	01	00	0	000	10	0	11010	00000
1D0	00	0000101111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1D1	00	0011101010	01100	00000	00	00	00	01	00	0	000	00	0	00000	00000
1D2	01	0011111100	00000	01101	00	10	10	00	00	0	000	00	0	00100	00000
1D3	00	0001100010	00000	00000	00	00	00	00	00	0	000	00	0	00010	00000
1D4	01	0111101010	01001	00110	00	00	00	01	00	0	000	10	0	00111	00000
1D5	01	0111101010	01001	00110	00	00	00	01	00	0	000	10	0	10010	00000
1D6	11	0100111110	00000	00000	00	00	00	00	00	0	000	10	0	00000	00000
1D7	01	0110110000	00000	00001	01	00	11	00	00	0	111	10	0	00000	00000
1D8	01	0100001001	11010	00111	00	00	00	00	00	0	000	00	0	00100	00000
1D9	00	0100010111	10100	00000	00	00	00	00	01	0	000	00	0	00000	00000
1DA	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1DB	00	0011100000	11010	10010	00	10	00	00	00	0	000	00	0	00000	00000
1DC	01	0100110000	00000	00000	00	11	00	00	00	0	000	00	0	00000	00000
1DD	00	0011111000	11011	01111	00	10	11	00	00	0	000	00	0	00000	00000
1DE	01	0000011100	00000	00101	00	00	00	00	00	0	000	00	0	00000	00000
1DF	00	0010011001	00000	00001	00	00	00	00	00	0	111	00	0	00000	00000
1E0	00	1000000000	00000	00001	00	00	00	00	01	0	000	00	0	00000	00000
1E1	01	1100010101	00001	00011	00	00	00	00	00	0	000	00	0	00000	00000
1E2	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1E3	00	0001000011	00000	00101	00	10	00	00	00	0	000	00	0	00000	00000
1E4	01	0000011010	00000	00000	00	00	00	00	10	0	000	00	0	00000	00000
1E5	00	0001110011	00000	00000	00	11	00	00	00	0	000	00	0	00000	00000
1E6	01	0010011100	00000	01101	00	10	00	00	00	0	000	00	0	00100	00000
1E7	00	0010011100	00000	00000	00	11	00	00	00	0	000	00	0	00000	00000
1E8	00	0000101110	10100	00110	00	10	10	00	00	0	000	00	0	00000	00000
1E9	01	0011101100	11010	00111	00	00	00	00	00	0	000	00	0	00100	00000
1EA	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1EB	00	0001100011	11010	01111	00	10	00	00	00	0	000	00	0	00000	00000
1EC	00	0000100101	11010	00011	00	10	11	00	00	0	000	00	0	00000	00000
1ED	01	0010001100	00010	00000	00	00	10	00	00	0	000	00	0	00100	00000
1EE	00	1111010011	10100	00011	00	00	00	01	00	0	000	10	0	00000	01100
1EF	01	0000101000	00000	00000	00	00	01	10	00	0	100	10	1	10100	00000
1F0	00	1000000000	00000	00001	00	00	00	00	01	0	000	00	0	00000	00000
1F1	01	1100001101	01001	01111	00	00	10	00	00	0	000	00	0	00011	00000
1F2	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1F3	00	0011111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1F4	00	0110000001	00000	00000	00	00	00	00	11	10	0	000	10	0	00000
1F5	00	0011100011	00000	00001	00	00	00	01	01	0	000	00	0	00000	00000
1F6	00	0100101111	00000	01110	00	00	00	00	00	0	111	10	0	00000	00000
1F7	00	0101111011	00100	00011	00	10	00	00	00	0	111	00	1	10111	00000
1F8	00	0001110110	10100	00011	00	10	00	00	00	0	000	00	0	00010	00000
1F9	00	0000000111	01001	00000	00	00	00	00	11	0	000	00	0	00010	00000
1FA	00	0001111110	10100	00011	00	10	00	00	00	0	000	00	0	00010	00000
1FB	00	0000001101	01001	00110	00	00	00	00	11	0	000	00	0	00010	00000
1FC	01	0011011100	00001	00111	00	00	00	11	10	0	000	00	0	00100	00000
1FD	01	0110000000	00000	00011	00	10	00	01	01	0	000	00	0	00000	00000
1FE	00	1001011101	11011	10010	00	11	11	00	00	0	000	00	0	00010	00000
1FF	00	1001001101	11011	10010	00	00	11	00	00	0	000	00	0	00010	00000

Table 2-5B Control-ROM Binary Content P856

ADD.	SNA	NAN	A	ADL	C	M	Q	S	P	CT	B	SEQ	R	GP	CR
000	00	1111101000	00011	00001	00	10	11	00	00	0	111	00	0	00000	00000
001	11	1111111111	00000	00000	11	10	11	10	11	0	000	10	0	11100	00000
002	00	1111101001	00000	00000	00	00	00	10	11	0	000	00	1	00000	00000
003	01	0110010000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
004	01	1111111000	11110	10010	00	00	11	00	00	0	000	00	0	00000	00000
005	00	1111111011	00000	00000	00	00	00	11	10	0	000	00	0	01110	00000
006	00	1111111111	10100	00011	00	10	00	00	00	0	000	00	0	00000	00000
007	00	1111111111	00000	01110	01	10	00	00	00	0	000	10	0	00000	00000
008	11	1111111111	01100	00001	11	10	11	10	11	0	000	10	0	11100	10000
009	00	1111101001	00000	00001	00	00	00	01	01	0	000	00	1	00000	10000
00A	00	1011011101	11110	00011	00	00	00	00	00	0	111	00	0	00000	00000
00B	00	1111111111	00000	00011	00	10	00	00	00	0	000	00	0	00000	00000
00C	00	1000000001	00100	00011	00	00	00	00	00	0	011	00	1	00000	00000
00D	00	1000000001	10100	00011	00	00	00	00	00	0	011	00	1	00000	00000
00E	00	0111001110	11011	00011	00	10	00	00	00	0	000	00	0	00000	00000
00F	00	0111001101	11011	00011	00	10	00	00	00	0	000	00	0	00000	00000
010	01	1110100000	11110	00011	00	00	11	00	00	0	000	00	0	00000	00000
011	00	1111101001	00000	00001	00	00	00	01	01	0	000	00	1	00000	00000
012	01	0111000000	01000	00001	00	00	00	00	00	0	100	00	0	10011	00000
013	00	0111000000	00000	00011	00	00	00	01	01	0	000	00	0	00000	00000
014	00	1110110000	11011	10010	00	10	00	00	00	0	000	00	0	00000	00000
015	00	1110110000	11011	10010	00	10	00	00	10	0	000	00	0	01110	00000
016	11	1111111111	00000	00000	11	10	11	10	11	0	000	10	0	11100	00000
017	11	1111111110	00000	00000	00	00	00	00	00	0	000	10	0	00001	00000
018	01	1100010011	10100	00011	00	10	00	00	00	0	000	00	0	01111	00000
019	01	1010101101	10100	00011	00	10	01	00	00	0	000	00	0	01111	00000
01A	01	1011111011	00100	00011	00	00	11	00	00	0	000	00	0	00000	00000
01B	00	0110011100	01001	10001	00	00	01	00	00	1	000	01	0	00110	00000
01C	01	1011101011	10100	00011	00	10	00	00	00	0	000	00	0	00000	00000
01D	01	1010010011	10100	00011	00	10	01	00	00	0	000	00	0	00000	00000
01E	00	0110111101	00100	00011	00	00	11	00	00	0	000	00	0	00000	00000
01F	00	0110011110	01001	01111	00	00	10	00	00	1	000	01	0	00011	00000
020	11	1111111111	01100	00110	11	10	11	10	11	0	000	10	0	11100	10100
021	00	1111101001	10100	00110	00	00	00	01	01	0	000	00	1	00000	10100
022	00	0111011000	00101	00011	00	00	00	01	00	0	000	00	1	00000	00000
023	00	0111011000	00101	00011	00	00	00	01	00	0	000	00	1	00000	00000
024	00	1000000001	00100	00110	00	00	00	00	00	0	011	00	1	00000	10100
025	00	1000000001	10000	00100	00	00	00	00	00	0	011	00	1	00000	10100
026	00	0011101111	11011	10010	00	10	00	00	00	0	000	00	0	00000	00000
027	00	1100111110	01011	00000	00	00	00	01	00	0	000	00	0	01011	00000
028	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
029	00	0111000011	11010	10010	00	10	11	00	01	0	000	00	0	00000	00000
02A	00	1010111001	11010	01011	00	10	11	00	00	0	000	00	0	00000	00000
02B	00	1010000101	10100	00011	00	00	00	01	00	0	100	00	1	10011	00000
02C	01	1110100010	01111	01110	00	11	00	11	10	1	000	10	0	00000	00000
02D	00	0110111100	00000	00001	00	00	00	01	01	0	000	00	1	00000	00000
02E	00	1001101000	00000	00000	10	10	00	00	00	0	000	00	0	00110	00000
02F	01	1110000000	11100	00011	00	00	11	00	00	0	000	00	0	00000	00000
030	11	1111111111	01100	00000	11	10	11	10	11	0	000	10	0	11100	11000
031	00	1111101001	10100	00000	00	00	00	01	01	0	000	00	1	00000	11000
032	10	1000000000	00000	00000	01	10	11	10	11	0	000	10	0	00000	00000
033	10	1000000000	00000	00000	01	10	11	00	11	0	000	10	0	00000	00000
034	00	1000000001	00100	00000	00	00	00	00	00	0	011	00	1	00000	11000
035	01	0101111100	11000	00011	00	00	00	00	00	0	000	00	0	00100	00000
036	00	0011110011	11011	10010	00	10	00	00	00	0	000	00	0	00000	00000
037	11	1111111111	01100	00010	11	10	11	10	11	0	000	10	0	11100	00000
038	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
039	00	0110111110	00100	00011	00	00	11	00	00	0	000	00	0	00000	00000
03A	01	1110000100	00000	01101	00	10	00	00	00	0	000	00	0	00100	00000
03B	11	1111111111	10100	00011	00	00	00	01	00	0	000	00	0	00000	00000
03C	01	1110000010	01111	01110	00	00	00	10	10	1	000	10	0	00101	00000
03D	00	0110111100	00000	00001	00	00	00	01	01	0	000	00	1	00000	00000
03E	00	1010111111	11011	01011	00	00	00	00	01	0	000	00	0	00000	00000
03F	01	1101100000	00000	00000	00	00	01	00	00	0	100	00	0	10011	00000
040	11	1111111111	01100	01000	11	10	11	10	11	0	000	10	0	11100	10000
041	01	1110001000	10110	01000	00	10	00	00	00	0	000	00	1	00000	00000
042	00	0111111101	00000	00000	01	10	00	00	11	0	000	10	0	00000	00000
043	00	0111110101	00000	00000	01	10	00	00	11	0	000	10	0	00000	00000
044	00	1000000001	00100	01000	00	00	00	00	00	0	011	00	1	00000	10000
045	00	1000000001	00000	01010	00	00	00	00	00	0	011	00	1	00000	00000
046	11	1111111111	00100	01000	11	10	11	10	11	0	000	10	0	11100	10000
047	00	1111101001	00000	00000	00	00	00	00	00	0	000	00	1	00000	01100
048	01	1101001110	00001	11100	00	00	00	00	00	0	000	00	0	00100	00000
049	01	1010000000	00001	00111	00	11	11	00	00	0	000	00	0	00000	00000
04A	00	0111000010	10100	00000	00	10	00	00	00	0	000	00	0	00000	00000
04B	01	1101101101	01100	10010	00	00	00	00	11	0	000	00	0	00000	00000
04C	01	1101100101	00111	00011	00	00	00	10	10	1	011	10	0	00000	00000
04D	00	1111101001	00000	00001	00	00	00	01	01	0	000	00	1	00000	00000
04E	01	1101010000	00000	00000	00	00	01	00	00	0	000	00	0	01101	00000
04F	00	1011110010	00000	01110	01	10	00	00	00	0	011	10	0	10001	00000
050	11	1111111111	01100	00010	11	10	11	10	11	0	000	10	0	11100	10000
051	01	1100001000	10110	00010	00	10	00	00	00	0	000	00	0	00000	00000
052	00	0111011100	00000	01110	00	00	00	01	11	0	000	10	1	00000	00000
053	00	0111011000	00000	01110	00	00	00	01	11	0	000	10	1	00000	00000
054	00	1000000001	00100	00010	00	00	00	00	00	0	011	00	1	00000	10000
055	00	0101010000	01000	01101	00	11	00	00	00	0	000	00	0	00000	00000
056	01	1101000000	00000	00000	00	00	01	00	00	0	000	00	0	00000	00000
057	01	1100100000	11110	10010	00	00	11	00	00	0	000	00	0	10001	00000
058	00	1101001110	01001	11100	00	00	00	00	00	0	000	00	0	00000	00000
059	01	1010000000	00001	00111	00	11	11	00	00	0	000	00	0	00000	00000
05A	00	0111000010	10100	00000	00	10	00	00	00	0	000	00	0	00000	00000
05B	01	1101001011	01100	01111	00	00	10	00	11	0	000	00	0	00011	00000
05C	01	1101000010	00111	00011	00	00	00	11	10	1	011	10	0	00000	00000
05D	00	0101111110	00000	00001	00	11	00	01	01	0	000	00	0	00000	00000
05E	00	1100110000	00000	00000	00	01	00	00	00	0	000	00	0	00000	00000
05F	00	1111111111	10110	00011	00	10	00	00	00	0	000	00	0	00000	00000
060	11	1111111111	01100	00111	11	10	11	10	11	0	000	10	0	11100	10000
061	00	0010001111	10110	00011	00	10	00	10	00	0	000	00	0	01001	00000
062	00	0111111100	00000	00000	01	10	00	00	00	0	000	10	0	00000	00000
063	00	0111110100	00000	00000	01	10	00	00	00	0	000	10	0	00000	00000
064	00	1000000001	00100	00111	00	00	00	00	00	0	011	00	1	00000	10000
065	11	1111111111	01010	01101	11	10	11	10	11	0	000	10	0	11100	10000
066	11	1111111111	00100	00111	11	10	11	10	11	0	000	10	0	11100	10000
067	00	1100000000	01000	00001	00	11	00	00	00	0	000	00	0	00000	00000
068	01	0110010000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
069	00	0010111111	00101	00011	00	00	11	00	01	0	000	00	0	00000	00000
06A	00	0110101110	01000	00001	00	00	00	10	00	0	000	00	0	00000	00000
06B	01	1100101011	01001	10001	00	00	01	00	11	0	000	00	0	00000	00000
06C	00	0111100100	01100	10010	00	00	00	00	00	1	000	01	0	00000	00000
06D	01	1110101111	01000	00001	00	00	00	00	00	0	000	00	0	00000	00000
06E	00	1111111111	00000	01110	01	10	00	10	11	0	000	10	0	00000	00000
06F	00	1111111111	00000	01110	01	10	00	00	00	0	000	10	0	00000	00000
070	10	1000000000	00110	00000	00	00	00	00	00	0	000	00	0	00010	00000
071	00	1100001111	00010	00011	00	00	11	00	00	0	000	00	0	01110	00000
072	00	1101011101	00000	01110	00	00	00	01	00	0	000	10	1	00000	00000
073	00	1101011100	00000	01110	00	00	00	01	00	0	000	10	1	00000	00000
074	11	1111111111	00100	00011	11	10	11	10	11	0	000	10	0	11100	10000
075	00	0110111100	00010	00011	00	00	00	00	00	0	000	00	1	00100	00000
076	00	0100010010	01001	11000	00	00	00	00	00	0	000	00	1	00000	11000
077	00	1110001011	11011	00011	00	10	00	00	00	0	000	00	0	00000	00000
078	00	0110001111	10100	00011	00	10	00	00	00	1	000	00	0	00000	00000
079	00	1010100000	11011	01111	00	00	11	00	00	0	000	00	0	11111	00000
07A	00	1100101011	01001	10001	00	00	01	00	00	0	000	00	0	00000	00000
07B	01	1100001011	01001	01111	00	00	10	00	11	0	000	00	0	00011	00000
07C	00	0110001011	10100	00011	00	10	00	00	00	1	000	00	0	00000	00000
07D	00	1010010000	11011	01111	00	00	11	00	00	0	000	00	0	10101	00000
07E	00	0110001011	10100	00011	00	10	00	00	00	1	000	00	0	00000	00000
07F	01	1111110100	00000	01001	00	00	11	00	00	0	000	00	0	00100	00000
080	00	0000010000	00000	00001	00	00	00	01	00	0	000	00	0	00000	00000
081	00	1000000000	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
082	00	1101100010	01010	01110	00	00	00	00	00	0	100	11	0	00000	00000
083	10	1000000000	00101	00011	00	10	11	00	00	0	000	00	0	00000	00000
084	00	1100010011	01100	10010	00	00	00	00	00	1	000	01	0	00000	00000
085	00	1100001011	01100	10001	00	00	01	00	00	1	000	01	0	00110	00000
086	00	1011101001	00000	00000	00	00	00	00	00	1	000	00	0	00000	00000
087	00	1011111001	00101	00011	00	00	11	00	00	0	000	00	0	00010	00000
088	01	0101100011	00000	01010	00	10	00	00	00	0	000	00	1	11111	00000
089	00	0101110010	01001	01010	00	00	11	00	00	0	000	00	0	01111	00000
08A	00	1001100000	00000	00011	00	00	00	00	00	0	111	00	1	00000	00000
08B	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
08C	01	0101010111	11010	01011	00	10	11	00	00	0	001	00	0	10100	00000
08D	00	1101010000	00000	00000	00	00	00	00	00	0	000	10	0	01101	00000
08E	01	1110101100	10100	00011	00	00	00	10	00	0	000	10	0	00100	00000
08F	00	1010111001	00000	01101	00	10	01	00	00	0	000	00	0	00000	00000
090	00	1101010101	11010	01011	00	10	00	00	00	0	000	00	0	00000	00000
091	10	1000000011	10100	00011	00	00	00	01	00	0	000	00	0	00000	00000
092	00	1111101101	10100	00011	00	10	00	00	00	0	100	11	0	11100	00000
093	10	1000000000	10100	00011	00	10	11	00	00	0	000	00	0	00000	00000
094	00	1100001011	01100	01111	00	00	00	00	00	1	000	01	0	00011	00000
095	01	1110000111	01000	00001	00	00	00	00	00	0	000	00	0	00000	00000
096	10	1000000000	00111	00011	00	10	00	00	00	0	000	00	0	00000	00000
097	00	1011101001	10100	00011	00	00	11	00	00	1	000	00	0	00000	00000
098	01	0101100011	00000	01010	00	10	00	00	00	1	000	00	1	11111	00000
099	00	0101001011	00010	10010	00	00	11	00	00	0	000	00	0	00000	00000
09A	00	0100101011	00001	00011	00	00	00	00	00	0	111	00	1	11111	00000
09B	00	0111111110	01101	00001	00	00	00	00	00	0	000	00	0	00000	00000
09C	01	0101100011	11011	01111	00	10	00	00	00	0	000	00	1	11111	00000
09D	00	1010000011	10100	00011	10	10	00	10	00	0	011	10	1	00110	00000
09E	00	1011000000	10100	00011	00	10	00	00	00	0	000	00	0	11111	00000
09F	00	0100011011	00000	00000	00	00	00	00	00	0	100	00	0	10101	01100
0A0	00	1110101101	00000	01010	00	00	00	01	00	0	000	00	0	01001	00000
0A1	00	1111101001	10100	00110	00	00	00	01	01	0	000	00	1	00000	00000
0A2	00	0111001111	11011	00011	00	10	00	00	00	0	000	00	0	00000	00000
0A3	10	1000000000	00101	00011	00	00	11	01	00	0	000	00	0	00000	00000
0A4	00	0110110111	01001	10001	00	00	01	00	00	1	000	01	0	00000	00000
0A5	01	0000011111	11011	00011	00	00	00	00	01	0	000	00	0	00000	00000
0A6	00	1010101101	00000	01101	00	10	00	00	10	0	000	00	0	00000	00000
0A7	00	0110011011	10100	00011	00	00	11	00	00	0	000	00	0	00000	00000
0A8	00	0100011101	00000	00000	00	00	00	00	00	0	000	00	1	10010	00000
0A9	00	0100011110	00000	00000	01	00	11	10	00	0	000	10	1	00000	00000
0AA	00	1010011111	00000	01101	00	10	00	00	00	0	000	00	0	00000	00000
0AB	00	1010100010	00000	00000	01	10	00	10	11	0	000	10	0	00000	00000
0AC	00	1000000001	00100	00011	00	00	00	00	00	0	011	00	1	10010	00000
0AD	00	0100101001	01010	00110	00	11	11	00	00	0	000	00	0	00000	00000
0AE	00	1111101001	10100	00011	00	00	00	01	00	0	000	10	0	00000	00000
0AF	01	1010100000	00000	00000	00	00	01	10	00	0	000	10	1	11111	00000
0B0	00	1010011101	00000	01101	00	10	00	00	00	0	000	00	0	00000	00000
0B1	00	1111101001	10100	00000	00	00	00	01	00	0	000	00	1	00000	00000
0B2	01	1011100000	10010	00110	00	10	00	00	00	0	011	00	0	00000	00000
0B3	10	1000000000	00000	00000	00	00	00	00	11	0	000	00	0	00000	00000
0B4	00	0110100010	01001	01111	00	00	10	00	00	1	000	01	0	00011	00000
0B5	01	0000011111	11011	00011	00	00	00	00	01	0	000	00	0	00000	00000
0B6	00	1110101001	10100	00011	00	00	00	01	00	0	000	10	0	00000	00000
0B7	01	1010010000	00000	00000	00	00	01	10	00	0	001	10	1	10101	00000
0B8	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
0B9	00	0100010010	00000	00000	01	00	11	10	00	0	000	10	1	00000	00000
0BA	00	1111101001	01011	01110	00	00	00	00	00	0	000	10	0	00000	00000
0BB	00	1010000010	00000	00000	01	10	00	10	11	0	000	10	0	00000	00000
0BC	00	1001111101	00000	01101	00	00	00	01	00	0	000	10	0	00000	00000
0BD	00	0100011011	01010	00000	00	11	11	00	00	0	000	00	0	00000	00000
0BE	00	0100111110	10000	00100	00	10	00	00	00	0	000	00	1	00101	10100
0BF	00	1111101001	01010	00001	00	00	00	00	00	0	000	00	1	00101	10000

Table 2-5B contd.

ADD.	SNA	NAN	A	ADL	C	M	Q	S	P	CT	B	SEQ	R	GP	CR
0C0	11	1111111111	01100	00001	11	10	11	10	11	0	000	10	0	11100	00000
0C1	00	1111010011	00000	00001	00	00	00	01	01	0	000	00	1	00000	00000
0C2	00	1001101101	00000	01001	00	00	00	00	00	0	000	00	1	01100	00000
0C3	00	0111011110	00000	00000	01	10	00	00	11	0	000	10	0	00000	00000
0C4	00	0010011111	01010	00110	00	00	00	00	00	0	000	00	0	00000	00000
0C5	00	1111101001	00000	00011	00	00	00	01	01	0	000	00	1	00000	00000
0C6	00	0100011000	00100	00011	00	00	11	00	00	0	000	00	0	00000	00000
0C7	11	1111111111	00100	00000	11	10	11	10	11	0	000	10	0	11100	11100
0C8	00	0100001110	00100	01011	10	10	00	00	00	0	000	00	1	10000	00000
0C9	11	1111111111	01100	01001	11	10	11	10	11	0	000	10	0	11100	00000
0CA	00	1111101001	00000	01110	00	00	00	01	01	0	000	10	1	00000	00000
0CB	00	1001110010	00000	00000	00	00	00	00	00	0	000	00	0	01001	00000
0CC	00	1000000001	00100	00011	00	00	00	00	00	0	011	00	1	10000	00000
0CD	00	1001111101	00000	01101	00	00	00	01	00	0	000	00	0	01110	00000
0CE	01	1001010000	00000	00110	10	10	01	00	00	0	000	00	0	00000	00000
0CF	00	1011011110	00000	00000	11	10	11	00	00	0	111	11	0	11100	00000
0D0	01	0110010000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
0D1	01	0110010000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
0D2	00	1001001101	01101	00001	00	00	00	00	00	0	000	00	0	00000	00000
0D3	10	1000000000	00000	01110	01	00	11	01	11	0	000	10	0	00000	00000
0D4	01	1000110111	01010	00000	01	10	00	01	00	0	000	10	0	00111	00000
0D5	00	0010101110	01001	00110	00	00	00	00	00	0	000	00	0	00000	00000
0D6	01	1001000000	00000	00000	00	00	01	00	00	0	000	00	0	00000	00000
0D7	01	0111111000	00000	01001	00	00	11	00	00	0	000	00	0	00000	00000
0D8	11	1111111111	00100	00000	11	10	11	10	11	0	000	10	0	11100	11100
0D9	11	1111111111	10100	00000	11	10	11	10	11	0	000	10	0	11100	11100
0DA	00	1001001001	10110	00011	00	00	00	00	00	0	000	00	0	01001	00000
0DB	00	1001000010	00100	00011	00	00	00	01	00	0	001	00	1	10101	00000
0DC	00	0100011001	00100	00011	10	10	00	00	00	0	000	00	1	10000	00000
0DD	00	1000111101	00000	00001	00	11	00	11	00	0	011	10	1	00000	00000
0DE	01	1000110000	00000	00000	00	00	01	00	00	0	000	00	0	00000	00000
0DF	01	0111111000	00000	01001	00	00	00	11	00	0	000	00	0	00000	00000
0E0	00	0011111011	00000	00001	00	00	00	01	00	0	000	00	0	00000	00000
0E1	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
0E2	00	1000101111	11011	00110	00	10	00	11	00	0	001	10	1	10101	00000
0E3	00	0111011101	00000	00000	01	10	00	00	00	0	000	10	0	00000	00000
0E4	00	0010101111	00000	00001	00	11	00	00	10	0	011	00	1	00000	00000
0E5	00	0010101111	00000	00001	00	11	00	00	10	0	011	00	1	10010	00000
0E6	01	1000001000	00000	00000	00	00	01	00	00	0	000	00	0	00000	00000
0E7	01	0111111000	00000	01001	00	00	11	00	00	0	000	00	0	00000	00000
0E8	00	1001100010	01011	00000	11	10	00	00	00	0	100	11	0	01011	00000
0E9	00	1111010001	10100	00011	00	00	00	01	00	0	000	10	1	00000	00100
0EA	00	1000100000	11010	10010	00	00	11	00	10	0	000	00	0	00000	00000
0EB	00	0011110011	10100	00011	01	11	11	01	00	0	000	10	0	01100	00100
0EC	00	0001011110	11011	10010	00	10	00	00	00	0	000	00	0	00000	00000
0ED	01	1001100000	01000	00001	00	00	00	00	00	0	111	00	0	00000	00000
0EE	00	0011010111	11011	10010	00	10	00	00	00	0	000	00	0	00000	00000
0EF	00	1000011101	01011	00000	00	00	01	01	00	0	000	00	0	01011	00000
0F0	00	0010011110	11010	01011	00	10	00	00	00	0	000	00	0	00000	00000
0F1	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
0F2	00	1000000101	10110	00011	00	00	01	10	00	0	011	00	1	01001	00000
0F3	00	1001011100	00000	01110	00	00	00	01	00	0	000	10	1	00000	00000
0F4	00	0111010111	00001	00011	00	00	00	01	00	0	000	00	1	00000	00000
0F5	00	0111010111	00001	00011	00	00	00	01	00	0	000	00	1	10010	00000
0F6	01	0111111000	00000	01001	00	00	11	00	00	0	000	00	0	00000	00000
0F7	01	0110010000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
0F8	00	1001001000	11000	00011	00	10	00	00	10	0	000	00	0	00000	00000
0F9	11	1111111111	01100	00101	11	10	11	10	11	0	000	10	0	11100	10000
0FA	00	1000001100	10100	00011	00	11	00	10	00	0	011	10	1	00000	00000
0FB	00	1000000011	00000	00001	00	00	00	01	00	0	000	10	0	00000	00000
0FC	00	1001101101	00000	00000	00	00	00	11	00	0	000	00	1	00000	00000
0FD	00	1000000001	00000	00101	00	00	00	00	00	0	011	00	1	00000	10000
0FE	00	1111101001	10100	00011	00	00	00	01	00	0	000	10	1	00000	00000
0FF	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
100	00	0001111111	00000	00000	00	00	00	00	00	0	000	00	0	01001	00000
101	00	1100011010	00000	00011	00	11	00	00	01	0	000	00	1	00000	00000
102	00	0111101100	00101	00110	00	00	00	01	00	0	000	00	1	00000	00000
103	00	1101011101	00101	00110	00	00	00	01	00	0	000	00	1	00000	00000
104	00	0110100011	00000	00000	01	10	00	00	00	0	100	11	0	00000	00000
105	01	0110101000	00000	00011	00	00	00	00	00	0	000	00	0	00100	00000
106	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
107	00	0011001110	00000	01101	00	10	00	00	00	0	000	00	0	00000	00000
108	01	0110100000	10000	00011	00	00	11	00	00	0	000	00	0	11011	00000
109	00	0010010011	10101	00011	00	00	00	00	01	0	000	00	0	00000	00000
10A	00	0111010000	00101	00110	00	00	00	01	00	0	000	00	1	00000	00000
10B	00	1101011100	00101	00110	00	00	00	01	00	0	000	00	1	00000	00000
10C	00	0010010010	11011	00011	00	10	11	00	00	0	000	00	0	00000	00000
10D	00	1111010011	00000	00011	00	00	00	01	01	0	000	00	1	00000	00000
10E	00	1111101011	00000	00000	00	00	00	00	01	0	000	00	0	00000	00000
10F	00	1001001011	11011	10010	00	00	11	00	00	0	000	00	0	00000	00000
110	00	0110111111	00000	00000	00	00	00	00	00	0	000	00	0	01101	00000
111	10	1000000000	00101	00110	00	00	11	01	00	0	000	00	0	00000	00000
112	00	1001011100	00101	00110	00	00	00	01	00	0	000	00	1	00000	00000
113	10	1000000000	10100	00011	01	10	11	01	00	0	000	10	0	00000	00000
114	00	0010010000	01010	00110	01	10	00	01	00	0	000	10	0	00111	00000
115	00	0010101110	01010	00110	00	00	00	00	00	0	000	00	0	00000	00000
116	00	0101011110	11010	00011	00	10	00	00	00	0	000	00	0	01101	00000
117	10	1000000000	00000	00000	01	10	11	00	00	0	000	10	0	00000	00000
118	00	0111011100	01101	00110	00	00	00	01	00	0	000	00	1	00000	00000
119	00	1111100011	01101	00000	00	00	00	00	00	0	000	00	0	01011	00000
11A	00	1111110010	01101	00000	00	00	00	00	00	0	000	00	0	01011	00000
11B	00	1111010001	00100	00011	00	00	00	00	00	0	000	00	1	00101	10000
11C	01	1101101101	00100	00011	00	00	00	00	00	0	000	00	0	00000	00000
11D	00	1001110010	01101	01101	00	00	00	00	00	0	000	00	0	00000	00000
11E	00	1111101100	01110	01110	00	00	00	00	00	0	100	11	0	00000	00000
11F	00	1111111111	00110	00011	00	10	00	00	00	0	000	00	0	01110	00000
120	00	0000001001	00000	00000	00	00	00	00	00	0	100	00	0	10011	00000
121	01	1101001101	11010	10010	00	10	00	00	01	0	000	00	0	00000	00000
122	00	1100011011	01100	01111	00	00	10	00	00	1	000	01	0	00011	00000
123	11	1111111111	00001	00011	11	10	11	10	11	0	000	10	0	11100	10000
124	00	0110110110	00000	00000	00	11	00	00	00	0	000	00	0	00000	00000
125	00	0110101011	01010	01101	00	10	00	00	00	0	000	00	0	00100	00000
126	00	0000010001	00000	00101	00	10	00	00	00	0	000	00	0	00000	00000
127	11	0011111110	00000	00001	00	00	11	00	00	0	000	10	0	00000	00000
128	00	1111010011	00001	00011	00	00	00	00	00	0	000	00	1	00101	10000
129	00	1011001001	10100	01111	00	10	00	00	00	0	000	00	0	00000	00000
12A	00	0010000001	00001	01011	10	10	00	00	00	0	000	00	0	00000	00000
12B	01	0000110100	00010	00011	00	00	00	00	00	0	000	00	0	00100	00000
12C	00	0010000111	00000	01001	00	00	00	01	00	0	111	00	0	00000	00000
12D	00	0110011110	00000	01010	00	00	10	00	00	0	000	00	0	00000	00000
12E	00	1000101011	11011	10010	00	10	00	00	10	0	000	00	0	00000	00000
12F	00	1000010101	11011	10010	00	10	00	00	00	0	000	00	0	00000	00000
130	00	0101111111	00000	00000	00	00	00	00	00	0	000	00	0	01101	00000
131	00	0110011101	00000	00000	00	11	00	00	00	0	000	00	0	00000	00000
132	00	0110111100	01010	00001	00	00	00	00	00	0	000	00	1	00100	00000
133	00	0001111000	00000	00000	00	11	00	00	00	0	000	00	0	00000	00000
134	00	0110010010	11000	00011	00	10	00	00	10	0	000	00	0	00000	00000
135	00	1110100011	01101	00110	00	00	00	01	00	0	000	00	1	00000	00000
136	00	0111010011	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
137	00	0110001111	10100	00110	00	10	00	00	00	0	001	00	0	00000	00000
138	00	0110001110	11000	00011	00	00	00	01	00	0	000	00	0	00000	00000
139	00	1110000111	00101	00011	00	00	11	00	10	0	000	00	1	00000	00000
13A	00	0110001100	11000	00011	00	00	00	01	00	0	000	00	0	00000	00000
13B	00	1101100011	00111	00011	00	00	00	00	10	1	011	00	1	00000	00000
13C	00	0110000010	11000	00011	00	00	11	00	01	0	000	00	0	00000	00000
13D	00	1101010011	00111	00011	00	00	00	00	10	1	011	00	1	00000	00000
13E	01	0000010010	10100	00011	00	00	00	00	00	0	000	00	0	00000	00000
13F	00	0010010011	00001	10010	00	10	11	11	10	0	000	00	0	00000	00000
140	00	0011111110	00000	00000	00	00	00	00	00	0	100	00	0	10011	00000
141	00	1111101001	01101	00000	00	00	00	00	00	0	000	00	1	01011	00000
142	00	1110011111	01100	01010	00	00	00	00	00	0	000	00	1	00000	00000
143	00	1000000001	10000	00000	00	00	00	00	00	0	011	00	1	00000	11000
144	00	1100011000	00000	00001	00	00	00	00	00	0	111	11	0	00000	01000
145	00	0101101111	00010	00011	00	00	11	00	00	0	000	00	0	00000	00000
146	01	0000111001	11011	00110	00	10	00	00	00	0	000	00	0	00100	00000
147	00	0000011000	00000	00000	00	00	01	00	00	0	000	00	0	00000	00000
148	00	0101101110	01001	10100	00	00	10	00	00	1	000	01	0	00000	00000
149	00	0101101011	01001	10100	00	11	00	00	00	0	000	00	0	11101	00000
14A	00	0101101001	01010	01101	00	00	00	00	00	0	000	00	0	00000	00000
14B	00	0110101011	00100	00011	00	00	00	00	00	0	000	00	0	00100	00000
14C	00	0101011101	00000	00001	00	00	10	00	00	0	000	10	1	11111	00000
14D	00	0100001010	00000	00000	00	00	00	10	00	0	000	10	1	11111	00000
14E	00	0010101011	11011	01111	00	10	11	10	11	0	011	00	0	00000	00000
14F	00	0011101100	01001	00001	00	00	00	11	10	0	000	00	0	00000	00000
150	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	01101	00000
151	00	0101001001	01001	01001	00	10	11	00	00	0	000	00	0	00000	00000
152	01	0000110000	00000	00000	00	11	00	10	00	0	000	10	1	11111	00000
153	00	1011110011	00000	10010	00	00	00	01	00	0	000	00	0	00000	00000
154	00	0000010000	00000	00101	00	00	11	10	00	0	001	10	1	10100	00000
155	00	0000010000	00000	00000	00	00	00	10	00	0	001	10	1	10100	00000
156	00	0111010011	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
157	00	0101000111	00000	00010	00	00	00	01	00	0	100	00	1	10111	00000
158	00	0101000110	01100	01110	11	10	00	00	00	0	000	10	0	00110	01000
159	00	1100001000	01100	00010	00	00	01	00	00	0	000	00	0	00000	00000
15A	00	0101001001	01001	00011	00	00	00	00	00	0	000	00	0	01111	00000
15B	00	0101000111	10101	11110	00	00	01	00	00	1	000	00	0	00011	00000
15C	00	0101000100	01001	11110	00	00	01	00	00	1	000	01	0	00000	00000
15D	01	0101101100	01001	11100	00	00	01	00	00	0	000	00	0	00100	00000
15E	00	0101000000	11011	00100	10	10	00	00	01	0	000	00	0	00000	00000
15F	00	0100010001	01010	01001	00	00	10	00	00	0	000	00	0	00000	00000
160	00	0001111001	00000	00000	00	00	00	00	00	0	100	00	0	10011	00000
161	11	1111111111	01010	00001	11	10	11	10	11	0	000	10	0	11100	00000
162	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
163	00	0001110011	10000	00011	00	10	00	00	00	0	000	00	0	00000	00000
164	00	0100110100	01001	01110	00	00	00	00	00	0	100	11	0	10100	00000
165	00	1011111101	00000	00000	00	00	00	00	00	0	100	00	1	10100	00000
166	00	0001000010	01111	00001	00	00	00	00	00	0	000	00	0	00000	00000
167	00	0001100011	01111	00001	00	00	01	00	00	1	000	00	0	00000	00000
168	11	0110111110	00000	00000	00	00	00	00	00	0	000	10	0	00000	00000
169	01	0100111001	10110	01000	00	00	00	00	00	0	000	00	0	00100	00000
16A	00	0001100000	00010	00011	00	00	00	00	00	0	111	10	1	11111	00000
16B	00	0100101011	01010	10010	00	00	00	00	00	0	000	00	0	00100	00000
16C	00	0100100010	01001	11010	00	00	00	00	00	0	000	00	1	00000	10100
16D	11	1111111111	01010	01111	11	10	11	10	11	0	000	10	0	11100	00000
16E	00	0100100000	10100	10010	00	10	00	00	00	0	000	00	0	00000	00000
16F	00	0100000001	10100	00110	00	11	00	00	01	0	000	00	0	00000	00000
170	00	0000111001	00000	01101	00	10	00	00	00	0	000	00	0	00000	00000
171	00	1010100100	10100	00011	01	10	00	01	00	0	000	10	0	00000	00000
172	00	1111110111	10100	00011	01	10	00	01	00	0	000	10	0	00000	00000
173	00	0100001000	10100	00011	11	00	11	01	00	0	000	10	0	00000	00000
174	00	1100001001	01010	10010	00	00	00	00	00	0	000	00	0	00100	00000
175	00	1010000100	10100	00011	01	10	00	01	00	0	000	10	0	00000	00000
176	00	0111010001	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
177	00	0100000111	01000	00001	00	11	00	00	00	0	000	00	1	00000	00000
178	11	1111111111	00000	00001	11	10	11	10	11	0	000	10	0	11100	11100
179	00	0100000011	01100	01001	11	10	00	00	00	0	000	10	0	00000	00000
17A	00	0001000111	00000	01010	00	11	10	00	00	0	000	00	0	00000	00000
17B	00	0001001100	00000	00001	00	11	00	00	01	0	000	00	0	00000	00000
17C	00	1110011000	10100	00011	00	00	00	01	00	0	000	00	1	00000	00000
17D	11	1111111111	01100	00010	11	10	11	10	11	0	000	10	0	11100	00000
17E	00	0100000000	10100	00110	00	00	00	00	01	0	111	00	0	00000	00000
17F	00	1100001110	01000	01010	00	00	00	00	00	0	000	11	0	11100	00000

Table 2-5B contd.

ADD	SNA	NAN	A	ADL	C	M	Q	S	P	CT	B	SEQ	R	GP	CR
180	00	0001010000	00000	00000	00	11	00	00	00	0	100	00	0	10011	00000
181	00	0001000000	00000	00000	01	10	00	00	00	0	000	10	0	00000	00000
182	00	0010100000	11010	10010	00	10	00	00	00	0	000	00	0	00000	00000
183	00	0111101001	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
184	00	0011111010	00100	00011	00	00	00	00	00	0	111	00	1	10110	00000
185	00	1100001000	00100	00011	00	00	00	00	00	0	111	10	0	00000	00000
186	01	0010101100	00011	00000	00	00	10	00	00	0	000	00	0	00100	00000
187	01	0011001100	00111	00000	00	00	01	00	00	1	000	00	0	00100	00000
188	00	0011110110	01101	00110	00	00	00	01	00	0	000	00	1	00000	00000
189	10	1000000000	00000	01110	00	00	00	11	01	0	000	10	1	00000	00000
18A	00	0100011111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
18B	00	0000011011	00000	01010	00	00	10	00	10	0	000	00	0	00000	00000
18C	00	0011100010	11011	00110	00	10	00	00	00	0	000	00	0	01010	00000
18D	00	0011101110	01000	00101	00	11	00	00	00	0	000	00	0	00000	00000
18E	01	0001001100	00001	00111	00	00	00	00	00	0	000	00	0	00100	00000
18F	00	0011001001	11011	00100	00	10	00	00	00	0	000	00	0	00000	00000
190	00	0000011001	00000	00101	00	10	00	00	00	0	000	00	0	00000	00000
191	00	1101111110	00000	00010	10	10	11	00	00	0	000	00	0	00000	00000
192	00	0100011111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
193	01	0000000010	00000	00000	01	10	00	00	00	0	000	10	0	00000	00000
194	00	0011010010	01100	00000	00	00	00	01	00	0	000	00	0	01011	00000
195	00	0011010000	10110	00011	00	00	00	10	00	0	011	00	1	00000	00000
196	00	0111101001	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
197	00	0011001111	10100	00011	00	11	00	10	00	0	011	10	1	00000	00000
198	00	1111101001	00000	00001	00	00	00	01	01	0	000	10	1	00000	00000
199	00	0010011110	00000	01101	00	10	00	00	00	0	000	00	0	00000	00000
19A	00	0100011111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
19B	01	0011113000	00000	00000	00	11	00	00	00	0	000	00	0	00000	00000
19C	01	0010111100	10100	00111	00	00	00	11	10	0	000	00	0	00100	00000
19D	00	0111111011	00000	00000	00	00	00	00	00	0	100	00	0	10011	00000
19E	00	0031100000	01000	01001	00	10	00	00	00	0	000	00	0	00000	00000
19F	00	0010100001	10100	00110	00	10	00	00	01	0	111	00	0	00000	00000
1A0	01	1001110100	01000	00001	00	11	00	00	10	0	000	00	0	00000	00000
1A1	01	1011101100	11010	00111	00	00	00	00	00	0	000	00	0	00100	00000
1A2	00	0100011111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1A3	01	0011000010	00000	00000	01	10	00	00	00	0	000	10	0	00000	00000
1A4	00	0010111010	00101	00000	00	10	00	00	00	0	000	00	0	00000	00000
1A5	00	1001010111	01001	00110	00	11	00	01	00	0	000	00	1	00000	00000
1A6	00	0100101110	11011	01011	00	10	00	00	00	0	111	11	0	01110	01000
1A7	01	0010111000	00000	00000	00	00	01	00	00	0	111	00	0	10111	00000
1A8	01	1001010110	01001	00000	00	00	00	01	00	0	000	10	0	00111	00000
1A9	00	1001110110	01101	01010	00	00	00	00	00	0	000	00	0	00000	00000
1AA	01	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1AB	00	0000010011	01010	10000	00	00	00	00	00	0	000	00	0	00000	00000
1AC	01	0010100010	00000	00001	00	00	00	11	10	0	011	10	0	00000	00000
1AD	00	0101100000	00000	00011	00	00	00	01	01	0	000	00	0	00000	00000
1AE	10	1111111111	01001	00001	11	10	11	00	10	0	000	11	0	11100	00000
1AF	00	0101100001	01000	01001	00	00	00	01	01	0	000	00	0	01101	00000
1B0	00	0010111011	11011	00011	00	10	11	00	00	0	000	00	0	00000	00000
1B1	00	0010001110	01000	01101	00	11	00	00	00	0	000	00	0	00000	00000
1B2	01	0001111100	00000	01101	00	10	00	00	00	0	000	00	0	00100	00000
1B3	01	0101112000	11011	00010	00	10	11	00	00	0	000	00	0	01101	00000
1B4	01	0111110010	01000	00001	00	00	00	00	10	0	000	00	0	00000	00000
1B5	01	1000001011	01010	00000	00	00	00	00	00	0	000	00	0	00000	00000
1B6	11	0101111110	00000	00000	00	00	00	00	00	0	000	10	0	00000	00000
1B7	01	0001010011	00000	00001	00	11	00	00	10	0	011	00	1	00000	00000
1B8	00	1011000010	00000	00001	00	00	00	00	00	0	011	00	1	00000	00000
1B9	00	0001110110	00000	00010	00	00	00	01	00	0	100	00	1	10110	00000
1BA	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1BB	00	0000011010	00000	01010	00	00	10	00	00	0	000	00	0	00000	00000
1BC	00	0010111000	11010	00011	00	00	11	00	00	0	111	11	0	11100	00000
1BD	00	0101100011	00000	00000	00	00	00	10	00	0	000	10	1	11111	00000
1BE	00	0010000000	00000	01001	00	10	00	00	00	0	000	00	0	01110	00000
1BF	01	0000101100	10100	00111	00	11	00	00	00	0	000	00	0	00100	00000
1C0	00	1111101000	00000	00000	00	00	00	00	00	0	100	00	0	10011	00000
1C1	00	0001101111	01001	00000	00	00	00	00	00	0	000	00	0	00000	00000
1C2	01	0001011100	00000	01101	00	10	11	00	00	0	000	00	0	00100	00000
1C3	00	0100000101	11011	01011	00	10	11	00	00	0	000	00	0	01101	00000
1C4	01	0111110001	01101	00001	00	11	00	00	00	0	000	00	0	00000	00000
1C5	00	1100001000	01100	01110	01	00	00	00	00	0	000	10	0	00000	00100
1C6	00	0110011100	00000	00000	01	00	11	00	00	0	000	10	0	00000	00000
1C7	00	0001010011	00000	00001	10	10	00	00	00	0	111	00	0	00000	00000
1C8	00	0001110110	01010	00000	00	00	00	00	00	0	000	00	0	00000	00000
1C9	00	0001111011	11011	00110	00	10	00	00	00	0	000	00	0	00000	00000
1CA	00	0100011111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1CB	00	0011110001	11011	01111	00	10	00	00	00	0	000	00	0	00000	00000
1CC	00	0011111111	00000	00101	00	00	11	00	00	0	000	00	0	00000	00000
1CD	00	0100110000	11011	01111	00	10	11	00	00	0	000	00	0	01101	00000
1CE	00	0101011100	01000	00001	00	00	00	00	00	0	000	10	0	11111	00000
1CF	00	1101111000	10100	00011	00	00	00	01	00	0	000	10	0	11111	00000
1D0	00	0001011111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1D1	00	0011010010	01100	00000	00	00	00	01	00	0	000	00	0	00000	00000
1D2	01	0011111100	00000	01101	00	10	00	00	00	0	000	00	0	00100	00000
1D3	00	0001100010	00000	00000	00	00	00	00	00	0	000	00	0	00010	00000
1D4	01	0111010010	01001	00110	00	00	00	01	00	0	000	10	0	00111	00000
1D5	01	0111010010	01001	00110	00	00	00	01	00	0	000	10	0	10010	00000
1D6	11	0100011110	00000	00000	00	00	00	00	00	0	000	10	0	00000	00000
1D7	01	0110110000	00000	00001	01	00	11	00	00	0	111	10	0	00000	00000
1D8	01	0100000100	11010	00111	00	00	00	00	00	0	000	00	0	00100	00000
1D9	00	0000010111	10100	00000	00	00	00	00	01	0	000	00	0	00000	00000
1DA	00	0100011111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1DB	00	0011100000	11010	10010	00	10	00	00	00	0	000	00	0	00000	00000
1DC	01	0100110000	00000	00000	00	11	00	00	00	0	000	00	0	00000	00000
1DD	00	0011110000	11011	01111	00	10	11	00	00	0	000	00	0	00000	00000
1DE	01	0000011100	00000	00101	00	00	00	00	00	0	000	00	0	00000	00000
1DF	00	0010010001	00000	00001	00	00	00	00	00	0	111	00	0	00000	00000
1E0	00	1000000000	00000	00001	00	00	00	00	01	0	000	00	0	00000	00000
1E1	01	1100010101	00001	00011	00	00	00	00	00	0	000	00	0	00000	00000
1E2	00	0100011111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1E3	00	0001000001	00000	00101	00	10	00	00	00	0	000	00	0	00000	00000
1E4	01	0000011010	00000	00000	00	00	00	00	10	0	000	00	0	00000	00000
1E5	00	0001110011	00000	00000	00	11	00	00	00	0	000	00	0	00000	00000
1E6	01	0010011100	00000	01101	00	10	00	00	00	0	000	00	0	00100	00000
1E7	00	0010011100	00000	00000	00	11	00	00	00	0	000	00	0	00000	00000
1E8	00	0000101110	10100	00110	00	10	00	00	00	0	000	00	0	00000	00000
1E9	01	0011101000	11010	00111	00	00	00	00	00	0	000	00	0	00100	00000
1EA	00	0100111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1EB	00	0001100011	11010	01111	00	10	00	00	00	0	000	00	0	00000	00000
1EC	00	0000100010	11010	00011	00	10	11	00	00	0	000	00	0	00000	00000
1ED	01	0010001100	00010	00000	00	00	10	00	00	0	000	00	0	00100	00000
1EE	00	1111101001	10100	00011	00	00	00	01	00	0	000	10	0	00000	01100
1EF	01	0000100000	00000	00000	00	00	00	01	10	0	001	10	1	10100	00000
1F0	00	1000000000	00000	00001	00	00	00	00	01	0	000	00	0	00000	00000
1F1	01	1100000101	01001	01111	00	00	10	00	00	0	000	00	0	00011	00000
1F2	00	0100011111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1F3	00	0011111111	00000	00000	00	00	00	00	00	0	000	00	0	00000	00000
1F4	00	0110000001	00000	00000	00	00	00	11	10	0	000	10	0	00000	00000
1F5	00	0011000011	00000	00001	00	00	00	01	01	0	000	00	0	00000	00000
1F6	00	0100101111	00000	01110	00	00	00	00	00	0	111	10	0	00000	00000
1F7	00	0101111011	00100	00011	00	10	00	00	00	0	111	00	1	10111	00000
1F8	00	0001101110	10100	00011	00	10	00	00	00	0	000	00	0	00010	00000
1F9	00	0000000111	01001	00000	00	00	00	00	11	0	000	00	0	00010	00000
1FA	00	0001111110	10100	00011	00	10	00	00	00	0	000	00	0	00010	00000
1FB	00	0000000101	01001	00110	00	00	00	00	11	0	000	00	0	00010	00000
1FC	01	0011011100	00001	00111	00	00	00	11	10	0	000	00	0	00100	00000
1FD	01	0110000000	00000	00011	00	10	00	01	01	0	000	00	0	00000	00000
1FE	00	1001011101	11011	10010	00	11	11	00	00	0	000	00	0	00010	00000
1FF	00	1001001101	11011	10010	00	00	11	00	00	0	000	00	0	00010	00000

2.48 INSTRUCTION WORD LOGIC

The instruction word logic (Figure 2-8AA) comprises the K register and the instruction decoder. This logic stores and decodes the program instruction word for use by the Microprogram Control.

2.49 K -- Instruction Register

This 16-bit register holds the instruction word which is obtained from memory via the GP-Bus BIO lines. The instruction-word format is given in Section I (paragraph 1.62). Four type 74175 IC chips are used as a straight 16-bit buffer register, with both high and low outputs available for decoding. Bus data BIO00-15R are loaded by CLK at the trailing edge of BP, when GFETCH is active. GFETCH is a general-field command bit (Table 2-3).

2.50 Instruction Decoder

The instruction decoder uses a programmable logic array (PLA) as the main decoding logic. The PLA provides an address code to the microinstruction control-store for 96 different input combinations. A set of gate-logic decoders in parallel with the PLA are used for ineffective branches and FPP instructions without attached FPP. The PLA0, PLA1 control logic controls some of the PLA and the gate-logic decoding. These instruction-decoder outputs are used with the Microprogram Control and are described in paragraphs 2.37 and 2.40 (Microinstr. Instr. Word, M.S. Pointer).

2.51 Logic gates are used to decode the K register into basic fields for controlling the PLA decoder and gate decoders. These gates may indicate when the instruction R1 or R2 fields contain 0 or 15, or when a branch condition is indicated and verified. Some bits of the K register are used as direct control bits for the PLA decoder. Complete PLA decoding is shown in Table 2-6.

2.52 PLA ROM maps are provided (Table 2-7) to show the PLA output code (as a two-bit hexadecimal number) produced for the various instructions or addressing types. The PLA output code relates directly to the control-store ROM address used by the microprogram control.

Table 2-6 Instruction Decoder PLA

	Data Input	Output	Comments	Group
	I14 ← → I0	F8 ← → F1		
	PLA0 PLA1 K0 K1 K2 K3 K4 R1E0 R1E15 K9 K10 R2E0 R2E15 K15	RAD 1 — 8		
1	LL----------	LLLLLLLL	Inhibit mode	
2	HHLLHLLH------	LLLLLLLL	INH, RIT, HLT	Privileged Instruction Detection
3	HHLHLL-L------	LLLLLLLL	I/O instructions	
4	HHLHHH-L------	LLLLLLLL	RER, WER	
5	HHH-----H-----	LLLLLLLL	Format 1 with R1=15	
6	HHHLLLL--LHLH-	LLLLLLLL	LD, ST with R2=15	
7	HHHLHHH--LHLH-	LLLLLLLL	ML, MS with R2=15	
8	HH-HHH-H----HL	LLLLLLLL	MVF, MVB, RTN with R2=15	
9	HHHLHHHH------	LLLLLLLL	TS, TS	
10	HHHHLHLL------	LLLLLLLL	EL, ES	
11	H-LH----------	L-------	K1 (Generals)	Format 0 (T8)
12	H-L-H---------	-L------	K2 (Generals)	
13	H-L--H--------	--L-----	K3 (Generals)	
14	H-L---H-------	---L----	K4 (Generals)	
15	H-L----H------	-------L	0R1 (Generals)	
16	H-LLLLL-------	LL------	LDK	
17	H-LLLLH-------	-------L	ABK	
18	H-LHLH--------	-------L	RF, RB	
19	H-LHLLL--HLH-L	-------L	WMP	
20	H-LLHHH----H-L	-----L--	Shift with n=0	
21	H-H----------	------L-	K0 (Generals)	Addressing Routines Format 1 (T1-7)
22	H-H------H----	-L------	K9 (Generals)	
23	H-H-------H---	--L-----	K10 (Generals)	
24	H-H--------H--	---L----	0R2 (Generals)	
25	H-H----------H	-------L	K15 (Store)	
26	H-HLLLH--LHL--	-------L	OPC-1 T3 (Store)	
27	H-HHHLL-------	L------L	OPC-12 Char. Instr.	
28	H-HLLLL--LHLHL	L-------	LDR T3 15R2	
29	H-HLHHHL-LHLHL	-----L--	MLR T3 15R2	
30	H-HHLL-L------	L------L	Floating Point	
31	H-H------LL---	L------L	T1 routine	
32	H-H-LLL------H	L------L	ST, TS, MS	
33	H-HLHLLH-----H	L------L	CM	
34	H-HLHHH-------	L------L	OPC-7, K0	
35	H-HHLHLL------	L------L	EL, ES	
36	H-HHHLH------H	L------L	CC	
37	H-HHLH-H-LHL--	L------L	DAR*, DSR *	
38	H-HHLH-H-H----	L------L	DA, DS	
39	H-HHHHL------L	-----L--	Return	
40	HHHHHHL------L	---L----	Return, User	

	Data input	Output	Comments	Group
	114 ⟷ 10	F8 ⟷ F1		
	PLA0 PLA1 K0 K1 K2 K3 K4 R1E0 R1E15 K9 K10 R2E0 R2E15 K15	RAD 1 — 8		
41	L HHH- - - - - - - - -	L - - - L - - -	K0.K1	Execution
42	L HH- H- - - - - - - -	- L - - - - - -	K0.K2	
43	L HH- - H- - - - - - -	- - L - - - - -	K0.K3	
44	L H- - - - H- - - - - -	- - - L - - - -	K4	
45	L HH- - - - - - H- - - H	- - - - - L - -	K0.K9.K15	
46	L H- - - - - H- - - - - -	- - - - - - - L	OR1	
47	L HHL L HH- - L L - - H	- - - - - L - L	NGR	
48	L HHL H- L - - L L - - H	- - - - - L L -	TM, TNM	
49	L H- L L L H- - - - - - -	- - - - - - - L	AB	
50	L H- L L L L - - - - - - -	- - - - L - - -	LD, ST	
51	L HHL L L L - - L H- HH	- - - - - - L -	STR with R2=15	
52	L HHHL H- H- L HH- -	- - - - - - L -	DAK, DSK	
53	- - HHL H- H- L L - - -	- - - - - L - -	DAR, DSR (ADD. also)	
54	L HHHHL L - - L L - - -	- - - - - - - L	ECR	
55	L H- HHHL - - L L - - -	- - - - - L - -	CR, EX	
56	L HHHHHHH- - - - - - -	- - - - - - - L	C1	
57	L H- L HHH- - - - - - -	- - - - L - - -	ML, MS, TL, TS, Shift	
58	L HHL HHHL - L HL HH	- - - - - - L -	MSR with R2=15	
59	L HHL HHH- - L HH- -	L - - - - - - -	MLK	
60	L HL L HHH- - H- - - -	- - - - - - L -	Shift K9	
61	L HL L HHH- - - H- - -	- - - - - L - -	Shift K10	
62	L H- HHHL - - - - - HL	- - - - - - L -	RTN with R2=15	
63	L HHHL L HL - L L - - -	- - - - - - L -	FFX, FFL	
64	H- - L HHL H- - - - - -	L L L L L L L L	XRK OR1	Trap Detection
65	H- L HL L - H- - - - - -	L L L L L L L L	I/O instr. OR1	
66	H- - HL HH- - - - - - H	L L L L L L L L	RB K15	
67	H- L HHL L - - - - - - -	L L L L L L L L	OPC-12 K0	
68	H- HL - - - - - L HH- H	L L L L L L L L	K0.$\overline{K1}$.K15 (T2)	
69	H- HL L L H- - H- - - H	L L L L L L L L	AB K15	
70	H- HL L L H- - - H- - H	L L L L L L L L		
71	H- HL L HHH- L L - - H	L L L L L L L L	SUR K15	
72	H- HL HL - H- - - - - L	L L L L L L L L	AN, OR OR1, $\overline{K15}$	
73	H- HL HL L H- L L - - -	L L L L L L L L	ANR OR1	
74	H- HL HL HH- - - - - H	L L L L L L L L	ORS OR1	
75	H- HL HL H- - L L - - H	L L L L L L L L	ORR K15	
76	H- HL HHH- - L L - - -	L L L L L L L L	OPC-7 (T1)	
77	H- HL HHHH- L HH- -	L L L L L L L L	MLK OR1	
78	H- HHL - - H- - - - - H	L L L L L L L L	OPC-8 to 11 OR1.K15	
79	H- HHL - - - - L HH- H	L L L L L L L L	OPC-8 to 11 T2.K15	
80	H- HHL - L L - L L - - -	L L L L L L L L	OPC-8, 10 T1.$\overline{OR1}$	
81	H- HHL L - L - L HH- -	L L L L L L L L	OPC-8, 9 T2.$\overline{OR1}$	

	Data Input	Output	Comments	Group
	114 ⟷ 10	F8 ⟷ F1		
	PLA0 PLA1 K0 K1 K2 K3 K4 R1E0 R1E15 K9 K10 R2E0 R2E15 K15	RAD 1 — 8		
82	H- HHL HL L - L HH- -	L L L L L L L L	DAK $\overline{OR1}$	Trap Detection
83	H- HHHL L H- - - - - -	L L L L L L L L	OPC-12 OR1	
84	H- HHHL L - - L HH- H	L L L L L L L L	OPC-12 T2.K15	
85	H- HHHL HH- H- - - H	L L L L L L L L	CC OR1	
86	H- HHHL HH- - H- - H	L L L L L L L L		
87	H- HHHHL L - - - - - L	L L L L L L L L	OPC-14 $\overline{OR1}$, $\overline{K15}$	
88	H- HHHH- H- L L - - L	L L L L L L L L	OPC-14,15 $\overline{OR1}$, $\overline{K15}$, T2	
89	H- HHHH- - - L HH- L	L L L L L L L L	OPC-14,15 $\overline{K15}$, T2	
90	H- HHHH- H- H- - - L	L L L L L L L L	OPC-14,15 OR1, $\overline{K15}$, K9	
91	H- HHHHHH- L L - - -	L L L L L L L L	C1R OR1	
92	H- HHHHH- - L HH- -	L L L L L L L L	C2 T2	
93	H- HHHHHH- L HL - L	L L L L L L L L	C1R * OR1	
94	L HH- - - - - - - H- - H	- - - - - L - -	K0 K10 K15	Execution Misc.
95	L HHHL L HL - L L - - H	- - - - - L - -	FFX	
96	L HHHHHL - H- - - - H	- - - - - - L -	CF with R1=15	

Table 2-7 PLA ROM Map

PLA Output

F: 8 7 6 5 | 4 3 2 1

MSB LSB

Example: Addressing type RT5S = /43 = 0100 0011$_2$

MSB \ LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		NO JUMP	NO JUMP P+2	NO FPP												
1		ABK														
2	ADK	ADKP	RT3	RT3S			RTN									
3	SUK	SUKP	RT2	RT2S			RTN USER									
4	ANK	RLY RIT INH	RT5	RT5S												
5	ORK	ENB SMD LKK	RT4	RT4S												
6	XRK		RT7	RT7S												
7	SM n ≠ 0	DSM n ≠ 0	RT6	RT6S	SM n ≠ 0	DSM n ≠ 0										
8	CIO CTR	WMP		RT1				RT1D								
9	SST TST INR			RT1P				RT1DP								
A		RF	RT3B	RT3C				RT3BM								
B		RB		RT2C												
C	LDK	LDKP		RT5C												
D	CWC	CWCP		RT4C												
E	WER	MVF		RT7C												
F	RER	MVB		RT6C												

ADDRESSING MODE

MSB \ LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0									LC	LCP			ST	STP	STD	STDP
1		AB							SLA SLN	DLA DLN	SLL SLC	DLL DLC	SRA SRN	DRA DRN	SRL SRC	DRL DRC
2	AD	ADP			ADS	IM										
3	SU	SUP			SUS	C2 NGR										
4	AN				ANS	CP	TK									
5	OR				ORS											
6	XR				XRS		TNM									
7									ML	TL			MS	TS	MSRD	
8									FL	MU			FS			
9									FO	OV	FFL		FOS		FFX	
A									EL	DAR= DA		DAK	ES		DAR	
B										DSR = DS		DSK			DSR	
C									LC	ECP			SC			
D									CW	CWP			CC			
E										RTN		RTN A15	OF	EX	OF 15R1	
F									MLK	C1				C15		

EXECUTION MODE

2.53 DATA HANDLING LOGIC

The Data Handling Logic (Figure 2-4) comprises the arithmetic logic unit (ALU), data and address storage and handling registers, and the logic for the data path. The basic components of the Data Handling Logic are :

ALU -- Arithmetic Unit	2.59	2-8 GG
M -- CPU Working Register (multi-in) : load C ; load Q.	2.64	2-8 GG
D Selector : ALU direct ; ALU exchange character ; ALU shift right ; BIO.	2.61	2-8 HH
L -- Data Register (multi-in) : Load D direct ; load D shift left. (operation result; output buffer)	2.63	2-8 HH
C Selector : D0-15 or 8-15; BIO0-15 or 8-15; INTAD 0-5; ASRO-7.	2.65	2-8 JJ
Q -- Shift Register : load; shift right; shift left.	2.67	2-8 JJ
S -- Address Register/Counter	2.71	2-8 KK
A - Bus Selection	2.72	2-8 LL
IPL -- Initial Program Loader	2.76	2-8 LL
P -- Program Register/Counter	2.77	2-8 LL
A0-A15 -- Scratchpad	2.79	2-8 MM
PSW - Program Status Word	2.84	
PLR -- Priority Level Register	2.85	2-8 NN
CR -- Condition Register	2.86	2-8 NN
GF -- General Flip-Flops	2.89	2-8 PP

The Data Handling Logic performs parallel processing of 16-bit words. Double-length operations are provided for processing of 31-bit words. Two 16-bit data paths loop through the arithmetic unit (ALU) : one loop for operand A and one loop for operand B.

2.54 Operand A is supplied by the A-Bus. A-Bus control logic selects which of the sources on the A-Bus is to be used as the operand. The various sources are connected by open-collector gates so only the selected inputs activate the bus. Operand A includes the scratchpad A0-A15, program counter P, program-status word PSW, initial program loader IPL, constant selector, and control-panel selector which supplies control-panel commands and system commands. Operand B is supplied by CPU working register M, shift register Q, and data selector C. The Q register is used as a shift register in double-length operations and as an auxiliary operand accumulator.

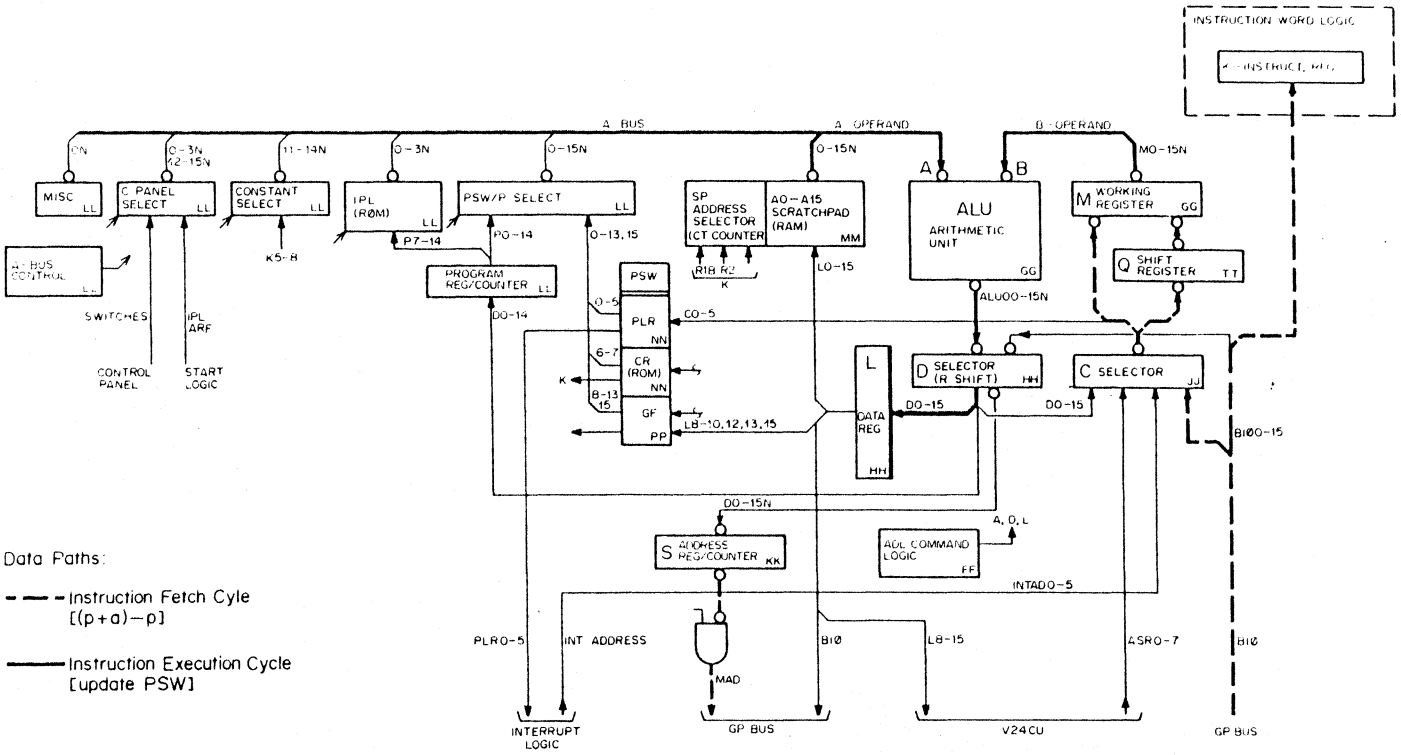
2.55 Data Path

Figure 2-4 shows the data path for instruction fetch operations (heavy dashed line) and instruction execution operations (heavy solid line). The fetch operation loads the instruction word into the instruction register K, and the eight least significant bits, via C, into the Q and M registers. The execution operation processes both operands through the ALU and outputs the result via D to the L register. Actual processing of data may be done by registers other than the ALU : the D selector and L and Q registers can perform shift operations in the data-path loop. With D selector at BIO direct, there is a direct loop from L, via BIO and D, to L. Scratchpad read, rewritten as same clock : path with D (exch. char.; shift right) and L (shift left).

2.56 A,D,L Command

The A,D,L command logic (Figure 2-8FF) controls the arithmetic operations by providing simultaneous command signals to the ALU, the D-selector, and the multiple-input L register. Thirty-two 8-bit command codes are stored in the ADL read-only memory (ROM). The command codes are selected by microinstruction bits μADL0-4 and some internal flags : Q15, Q16, FSIG, and M00N.

2.57 The first three address bits (μADL0-2) are used for direct ROM addressing (inputs E,D,C); they also control a dual 4-input multiplexer (type 9309) which selects the last two address bits (inputs B,A) of the ROM. ROM inputs B and A may be the last two microinstruction bits (muADL3-4, inverted)



Note: AA, BB etc. refers to logic diagrams 2-8AA, BB etc.

Figure 2-4 Data Handling Logic

or the flag bits Q15, Q16, FSIG, M00N, as follows :

Multiplexer Select Input			Multiplexer Output to ADL Command ROM	
µADL: 0, 1, 2		RALUA: 1N, 2N	RADL3	RADL4
0 0 0		1 1	µADL3N	µADL4N
0 0 1		1 1	µADL3N	µADL4N
0 1 0		1 1	µADL3N	µADL4N
0 1 1		1 1	µADL3N	µADL4N
1 0 0		1 1	µADL3N	µADL4N
1 0 1		1 0	Q15	Q16
1 1 0		0 1	µADL3N	FSIGN
1 1 1		0 0	µADL3N	DIVFLAGN

DIVFLAG = FSIGN ⊕ M00N

Table 2-8 shows the complete microinstruction/flag control of the ADL ROM, the ROM contents, and the output functions.

2.58 The ADL-ROM outputs ALUS0N-3N are used as the ALU selection inputs S0-4 (Figure 2-8 GG). The ALUCO16 signal is sent to the ALU and the ALU look-ahead-carry unit as a carry control signal. The microinstruction bit µADL4 is also sent directly to the ALU CE input to select logic functions (CE-high) or arithmetic functions(CE-low). The ADL-ROM outputs DS0-1 (combined with microinstruction field bit GMULTI) are the control signals for the four-input D selector (Figure 2-8 HH). The D00DN signal that is generated as an auxiliary part of the ADL command logic is used as one input to the D selector, bit 0; this logic is described with the D selector. The ADL-ROM output LSEL is sent to the L register (Figure 2-8HH) to select direct load (LSEL-low) or shift left (LSEL-high).

Table 2-8 ADL Command ROM

MUADL 0 1 2 3 4	FLAGS	ADDRESS	ALUS0N ALUS1N ALUS2N ALUS3N ALUCO16 DS0N DS1N LSEL	MNEMO	FUNCTION
0 0 0 1 1		0 0	0 0 0 0 0 0 1 1 0	ALUA	Operand A
0 0 0 1 0		0 1	0 0 1 0 0 1 1 0	AOB	Logical OR of A and B
0 0 0 0 1		0 2	1 0 1 0 0 1 1 0	ALUB	Operand B
0 0 0 0 0		0 3	1 0 0 1 1 1 1 0	AMB	Arithmetic Subtract A minus B
0 0 1 1 1		0 4	0 1 1 0 0 1 1 0	AXB	Logical XOR of A and B
0 0 1 1 0		0 5	0 1 1 0 0 1 1 0	APB	Arithmetic Addition A plus B
0 0 1 0 1		0 6	0 1 0 1 0 1 1 0	BINV	Operand B Inverted
0 0 1 0 0		0 7	0 1 1 0 1 1 1 0	APLB1	Arithmetic Addition with Carry A plus B plus 1
0 1 0 1 1		0 8	0 0 0 0 0 0 1 0	ACR	Operand A characters crossed on Selector D
0 1 0 1 0		0 9	0 0 1 1 1 1 1 0	ZERO	ALU output is zero
0 1 0 0 1		0 A	1 0 1 0 0 0 1 0	BCR	Operand B characters crossed on Selector D
0 1 0 0 0		0 B	0 1 1 1 1 1 1 0	AANDB	Logical AND of A and B
0 1 1 1 1		0 C	0 0 0 0 0 1 0 0	ASHR	Operand A shifted right one position
0 1 1 1 0		0 D	0 0 0 0 0 0 0 0	DBIO	BIO Receivers selected on D
0 1 1 0 1		0 E	1 0 1 0 0 1 0 0	BSHR	Operand B shifted right one position
- - - - -		0 F	1 1 1 1 1 1 1 1	-	Not used
- - - - -		1 0	1 1 1 1 1 1 1 1	-	Not used
1 0 0 1 0		1 1	1 1 0 0 0 1 1 0	TWOA	Operand A added to itself
1 0 0 0 1	Q15 Q16	1 2	0 0 0 0 0 1 1 1	ASHL	Operand A shifted left one position
1 0 0 0 0		1 3	1 1 0 0 0 1 1 1	FORA	Operand A four times (two in ALU and SAL)
1 0 1 0 0	0 0	1 4	0 0 0 0 0 1 0 0		Operand ASHR
1 0 1 0 0	0 1	1 5	0 1 1 0 0 1 0 0	MULTI	Operands A plus B and SHR
1 0 1 0 0	1 0	1 6	1 0 0 1 1 1 0 0		Operand A minus B and SHR
1 0 1 0 0	1 1	1 7	0 0 0 0 0 1 0 0		Operand ASHR

MUADL 0 1 2 3 4	FLAGS	ADDRESS	ALUS0N ALUS1N ALUS2N ALUS3N ALUCO16 DS0N DS1N LSEL	MNEMO	FUNCTION
1 1 0 1 0	1	1 8	0 1 1 0 1 1 1 0	DADD	Arithmetic addition A plus B plus 1
1 1 0 1 0	FSIG 0	1 9	0 1 1 0 0 1 1 0		Arithmetic addition A plus B
1 1 0 0 0	1	1 A	1 0 0 1 0 1 1 0	DSVB	Arithmetic subtract A minus B minus 1
1 1 0 0 0	0	1 B	1 0 0 1 1 1 1 0		Arithmetic Subtract A minus B
1 1 1 1 0	1	1 C	0 1 1 0 0 1 1 1	DIVSH	Addition and SHR 2 (A+B) + Q0
1 1 1 1 0	FSIG ⊕ M00 0	1 D	1 0 0 1 1 1 1 1		Subtract and SHR 2 (A-B) + Q0
1 1 1 0 0	1	1 E	0 1 1 0 0 1 1 0	DIVALU	Addition A + B
1 1 1 0 0	0	1 F	1 0 0 1 1 1 1 0		Subtract A - B

2.59 ALU -- Arithmetic Unit

The arithmetic unit (Figure 2-8 GG) uses four 4-bit ALU chips (type 74181) to perform arithmetic and logic functions on two 16-bit operands. The ALU chips are controlled by microinstruction bit μADL4 and the ADL-command logic (using bits μADL0-4). Bit μADL4 is applied to the CE input to select arithmetic (CE-low) or logic (CE-high) functions. All control bits are active high, while the data in and out (in this application) are active low. The ALU functions are shown in the following table. The control-signal logic, and the complete arithmetic unit functions combined with the D and L register operations, are discussed in the previous section (A,D,L Command) and shown in Table 2-8.

ALU Function Table

	ADL-Control ROM						
μADL4	ALUCO16	ALUSO-----3				Operation	
CE	CIN	S3	S2	S1	S0		
0	0	1	0	0	1	A plus B	ARITHMETIC
0	0	1	0	1	1	A or B	
0	0	1	1	0	0	A plus A	
0	1	0	0	0	1	A and B	
0	1	0	0	1	1	Zero	
0	1	0	1	1	0	A minus B	
1	-	0	1	0	1	B inverted	LOGIC
1	-	1	0	0	1	A⊕B	
1	-	1	0	1	0	B	
1	-	1	1	1	1	A	
1	-	1	0	0	1	A⊕B + 1	

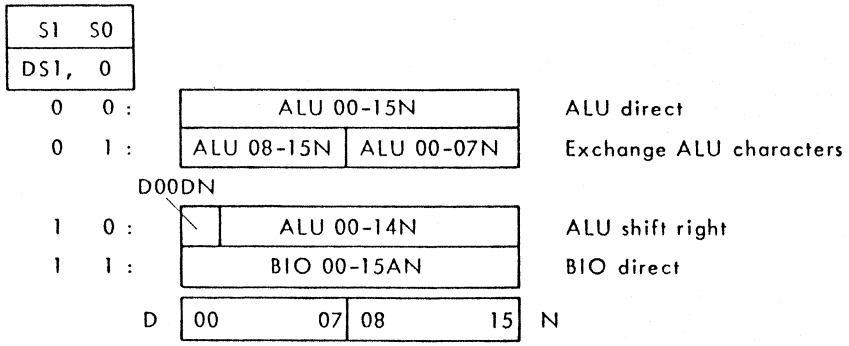
Control signals are all active high. Functions are for active-low data in and out.

A carry-look-ahead unit (type 74182) is used in conjunction with the ALU chips to provide anticipated carry across all four ALU circuits.

2.60 The zero-ALU (0ALUN) output is generated in subtract mode when both operands are equal (A=B). A zero-ALU, left-half (0ALUL) output sets the stack overflow indicator (STOV). Since stack operations forbid a memory address equal-to or less-than 128 (100 hexadecimal), the left-most character of the address (bits 0-7) must have at least one bit set. When S is loaded from the ALU during a stack operation, the all-zero ALU output (A=B) indicator STOV is therefore gated by GFSTOV to set GF flip-flop PIF (Figure 2-8 PP).

2.61 D Selector

The D selector (Figure 2-8 HH) is used as a control element in the arithmetic loop. The four D-selector functions (ALU direct, exchange ALU characters left and right, ALU shifted right, and BIO direct) are selected by the ADL-command logic (Table 2-8). The ADL-command signals DS0, DS1 operate the D selector as follows :



The D selector comprises eight type 9309 (dual 4-input multiplexer) circuits. These circuits provide both the true and complementary outputs of the active-low inputs. The inverted D-selector output (active-high) is sent to the L register, C selector, and P register/counter. The true output (active low) is sent to the S register/counter.

2.62 The ALU shift-right mode is used for shift-right and multiplication operations. The input bit D00DN used during this mode is provided by the ADL command logic (Figure 2-8 FF). Shift Right Arithmetic (SRA) and Shift Right Normalize (SRN) instructions use the ALU sign bit, ALU00. The Double Shift Right Circular (DRC) instruction uses Q15 for D00DN. Multiplication instructions set D00DN directly when negative overflow is detected (NOVF), or use the ALU sign bit ALU00 when positive overflow is not detected (POVF). The D00DN selection is shown in the following table.

GCRDSR.K9.ALU00	Shift Right, Arithmetic or Normalize (SRA,SRN)
GCRDSR.K08Q15	Double Shift Right Circular (DCR)
µADL0.NOVF	Multiply and negative overflow
µADL0.P0VN.ALU00	Multiply and positive overflow

2.63 L -- Data Register

The L register (Figure 2-8 HH) is a 16-bit, multiple-input register comprised of four type 74298 chips. The L register is used for storing the data from the ALU (or BIO) to be output to the scratchpad (A0-15) or the GP bus. The input data to the L register is provided by the D selector. The L register is in the operand-A loop between the ALU and the scratchpad. Since the L register is loaded by the leading-edge of BP, an operand can be read from and re-written into the scratchpad on the same clock cycle. The two inputs to the L register are D direct and D shifted left. These two operating modes for L are selected by the ADL command logic (Table 2-4) bit LSEL :

LSEL	Data Source		Function
0	D 00-15		D direct
1	D 01-15	Q00	D shifted left
L	00——14	15	

Bit Q00 is shifted into the least-significant position during a Division instruction when the new remainder is loaded.

The L register stores active-high data with no inversion between input and output.

2.64 M -- CPU Working Register

The M register (Figure 2-8 GG) is a 16-bit, multiple-input register comprised of four type 74298 chips. The M register is used as the CPU working register in the operand-B data path. Microinstruction control of the register uses bits µMLOAD and µMSEL to load the register and to select the C selector or Q shift register for inputs, as follows :

Enable Clock µMLOAD	Select C or Q µMSEL	Mnemonic	Data Source
0	-	No Op	Off; previously stored data available at output.
1	0	MYC	C 00 15
1	1	MYQ	Q 00 15
			M 00 15

The M register stores active-low data with no inversion between input and output. The µLOAD signal enables the CLMN input to the clock to store the selected data on the leading edge of BP.

2.65 C Selector

The C selector (Figure 2-8 JJ) uses two, quad 2-input multiplexers (type 8234) for the bit 0-7 selection, and four, dual 4-input multiplexers (type 9309) for the bit 8-15 selection. The result is a four-input multiplexer with two 16-bit sources and two 8-bit sources. Three microinstruction selection bits are used in such a manner that the two 16-bit sources (D and BIO) can be selected whole or as short constants (bits 8-15 only), or either of the 8-bit sources (INTAD and ASR) can be selected. The sources are selected by microinstruction bits μC0, μC1, and GCSLEN as follows:

$(\mu C0+\overline{C1})$ CLEFS0	μC0	μC1	GCSLEN	Mnemonic	Source
00-07		08-15			
S0	S1	S0	S1		
1	0	0	1	CALU	D00 — 15
0	0	1	1	CBIO	BIO00 — 15
1	1	0	1	CLUR	D08 — 15
1	1	1	1	CIOR	BIO08 — 15
1	1	0	0	CLUR	INTAD0 — 5 | 0 | 0
1	1	1	0	CIOR	ASR0 — 7
1	0	0	0	(CALU)	D00 — 07 / INTAD0 — 5 | 0 | 0
0	0	1	0	(CBIO)	BIO00 — 07 / ASR0 — 7
				C	00N — 07N / 08N — 15N

The last two possibilities are not used.

2.66 The C selector inverts all selected data from active high to active low. The 0's supplied for the not-used bit positions are therefore output as inactive highs. The C-selector outputs are sent to the Q and M registers in the operand-B data path. The six least-significant bits (C00N-05N) are also sent to the priority level register during an interrupt routine.

2.67 Q Shift Register

The Q register (Figure 2-8 JJ) uses four type 74194 circuits as a 16-bit, left/right shift register. Q may be parallel-loaded from the C selector, shifted right (with ALU15N as a serial input), or shifted left (with the selected bit, Q15DN, as a serial input). Loading and shifting is done on the leading-edge of clock pulse BP (BPQ) according to the function selected by microinstruction bits μQ0, μQ1 as follows :

μQ0, Q1	Mnemonic	Function
0 0	QI	Hold contents (No Op)
0 1	SLQ	Shift Left Q
1 0	SRQ	Shift Right Q
1 1	QYC	Parallel load Q from C

In the operand-B arithmetic loop, Q can be loaded from the M register, via ALU--D--C, and reloaded into the M register on the same BP clock pulse. No Q-register shifting may be performed on a single-clock-pulse loop since Q must be in the parallel-load mode.

2.68 The shift-right serial input, ALU15N, is used for double-length, shift-right operations. The shift-left serial input, Q15DN, is used for double-length left circular (DLC) shift and Divide instructions. Q15DN is derived from a 74151A circuit by the selection-inputs K008N, M00N, and ALU00N. For DLC shift instructions (K08N active low), the serial input is provided by microinstruction bit GCSELN if M00N is active; the serial input is a logic zero (high) if M00N is inactive (high). For Divide instructions (K08N high and RALUA1N (μADL 0.1) = 0), Q15DN is produced from the quotient bit ALU00 ⊕ M00. See following diagram.

K08N	M00N	ALU00N		
S2	S1	S0	Q15DN =	
L	L	L	GCSELN	DLC
L	L	H	GCSELN	
L	H	L	H	
L	H	H	H	
H	L	L	(μADL0.1)	Divide
H	L	H	H	
H	H	L	H	
H	H	H	(μADL0.1)	

L = low = active

2.69 The two least-significant bits of Q are used to control the next-cycle operation of a Multiply execution. One bit position (Q16) of a fifth 74194 is used to save the previous contents of Q15 at the end of the Multiply cycle, while Q14 is shifted into Q15. Q00, Q15N, and Q16N are used by the ADL command logic (Figure 2-8 FF) for arithmetic operation control. The three other bit positions of the fifth 74194 are used in the Bus Controller logic (Figure 2-8 TT). This fifth 74194 is used in the Hold (GCRFNUN = 0) or Parallel-Load (GCRFNUN = 1) modes only.

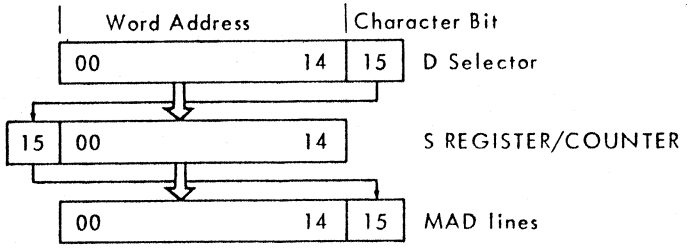
2.70 Q-register bit Q00/Q00N is used for microinstruction addressing in the Flag mode (paragraph 2.28 and Figure 2-8 DD). Q00 is also used as a serial input to the L register during a left-shift L operation.

2.71 S -- Address Register/Counter

The S register/counter (Figure 2-8 KK) is a 16-bit synchronous up/down counter using four type 74S169 circuits. Fourteen bits of the S register/counter are used to store the memory word address, and increment or decrement the address in one-word steps. Loading or counting takes place on the leading edge of the BP pulse, according to the following control from microinstruction bits μS0 and μS1:

μS0, S1	Mnemonic	Function
0 0	SI	Inhibit counting or loading
0 1	SYD	Load S0-16N with D0-15N
1 0	SP2	S plus 2 (count down)
1 1	SM2	S minus 2 (count up)

Since S is loaded with negative (low-level active) data, the count-down mode increments the value of the contents and count-up decrements. The S register/counter is loaded from the D selector, as shown in the following diagram :



D00-14, representing the memory word address, is loaded into the least-significant position of S, while D15, representing the character address, is loaded into the most-significant position. S-register counting then affects a two-character address change (S plus 2, or S minus 2) for a single increment or decrement of the counter. The character indicator from the most-significant position in S is then switched back to the least-significant position on the memory address lines (MAD00-15). The S register/counter works with low-level data, and does not invert.

2.72 A-Bus Selection

The A-Bus selection logic determines which source is to be used as operand-A of the arithmetic operation. Control of the A-bus selection is by microinstruction bits μA0-4 (Table 2-9). The possible sources for operand-A on the A-bus are :

- Scratchpad A0-A15
- Initial program loader IPL
- Program counter P

- Program status word PSW
- Instruction field (R1 or R3)
- Constant 2_{10} (/002) or 16_{10} (/010)
- Control-panel/System
- A-bus equals zero

All operand-A sources onto the A-bus are via active-low, open-collector output circuits (8234 multiplexers, 6200 ROM, 7489 RAM, and one 7403 gate). All these circuits provide a high-level output to the bus when they are not selected. This high is then over-ridden by any active low signal from a selected source.

2.73 The scratchpad (Figure 2-8 MM) is selected directly by μA0 to the chip-select inputs of the scratchpad logic. The specific scratchpad address (A0 to A15) is then selected by μA2-4 controlling the scratchpad-address logic. When the scratchpad is selected, μA1 differentiates between reading and writing the selected address.

2.74 Any A-bus source except the scratchpad is selected by the A-bus control logic (Figure 2-8 LL). The inverted μA0 input to the 1-of-10 decoder chip (type 9301) forces the decoder higher than the seven possible outputs that are connected; this effectively keeps this part of the A-bus selection switched off when the scratchpad is selected. If μA0 is active (high), and μA1-3 are all low, the non-connected output-0 is decoded and no A-bus source is selected; operand-A is then equal to zero. The active-low outputs from the 9301 decoder select either the IPL (output-1) or one of the type 8234 multiplexers. These multiplexers have their A inputs selected by an active low to S1 only, or their B inputs selected by an active low to S0.

2.75 Double-Word Trap. If a Trap occurs during a double-word operation, (P) must be decremented an extra position. The DWIF flip-flop (Figure 2-8 LL) is set for all double-word instructions. If a Trap routine (Figure 1-12) is initiated, the first microinstruction (address /0FF) produces GAEXL which is gated by DWIF to set A-bus bit A00N. This increments the normal microinstruction address by one to select /12E rather than /12F.

Table 2-9 A-Bus Selection

Microinstruction μA0, A1, A2, A3, A4					Control decoder (9301) output active	Mnemonic	Function
0	0	0	0	0		ARA0	Read scratchpad accumulator : A0
0	0	0	0	1		ARA1	A1
0	0	0	1	0		ARA2	A2
0	0	0	1	1		ARA15	A15
0	0	1	0	0		ARR1	R1 (Addressed by K5-7,8)
0	0	1	0	1		ARR2	R2 (Addressed by K11-14)
0	0	1	1	0		AR1215	(Addressed by K12-15)
0	0	1	1	1		ARCT	(Addressed by CT counter)
0	1	0	0	0		AWA0	Write scratchpad accumulator : A0
0	1	0	0	1		AWA1	A1
0	1	0	1	0		AWA2	A2
0	1	0	1	1		AWA15	A15
0	1	1	0	0		AWR1	R1 (Addressed by K5-7,8)
0	1	1	0	1		AWR2	R2 (Addressed by K11-14)
0	1	1	1	0		AW1215	(Addressed by K12-15)
0	1	1	1	1		AWCT	(Addressed by CT counter)
1	0	0	0	-	--	AZ	A-bus equals zero
1	0	0	1	-	1	AIPL	Read IPL
1	0	1	0	-	2	AEP	Read P
1	0	1	1	-	3	APSW	Read PSW
1	1	0	0	-	4	AEN	Read content of K5-8
1	1	0	1	1	5	ATW0	Constant 2_{10} (/002) onto A-bus
1	1	0	1	0	5	ATEN	Constant 16_{10} (/010) onto A-bus
1	1	1	0	-	6	APUP	Control panel inputs onto A-bus
1	1	1	1	-	7	ASYS	System inputs onto A-bus

2.76 IPL -- Bootstrap

The IPL circuit is a 64-word hardware bootstrap stored in a type 6200 Read Only Memory (ROM) of 256 four-bit words. The ROM contents are regrouped into 16-bit words when they are loaded into main memory by the IPL-microprogram routine (Figures 1-9, 1-10). The IPL/Bootstrap logic (Figure 2-8LL) is addressed by the P-register/counter (bits P07-14) and is accessed through the A-bus. The A-bus-selection command code is μA0,1,2, 3 = 1 0 0 1 for the read-IPL routine. Table 2-10 is a listing of a bootstrap after being loaded into memory 00-63. Use of the bootstrap for initial program loading is discussed in Section III. Other bootstrap ROMs may be provided with different CPUs.

2.77 P -- Program Register/Counter

The P register/counter (Figure 2-8 LL) is a 16-bit synchronous up/down counter using four type 74S169 circuits. The fourteen least-significant positions of P are loaded from the D selector with the 14-bit word address of the program. The P register is also used as an internal counter : in this case, the most-significant bit (which isn't loaded from D) is sent to the flag-selection logic as PM1 (P minus 1). PM1 is used by microinstruction Addressing, Flag mode (paragraph 2.26) to indicate the end of a multiple word instruction.

2.78 Loading or counting of P takes place on the leading edge of the BP pulse (BPP) according to the following control from microinstruction bits μP0 and μP1 :

μP0,P1	Mnemonic	Function
0 0	PI	Inhibit counting or loading
0 1	PYD	Load P0-14 with D0-14
1 0	PM2	P minus 2 (count down)
1 1	PP2	P plus 2 (count up)

The program word-address in P is accessed through the A-bus. The A-bus selection code μA0,A1,A2,A3 = 1010 for read-P. The eight least-significant address bits (P07-14) are also applied directly to the addressing inputs of the IPL ROM, for use when the IPL is selected.

Table 2-10 List of Bootstrap Loaded in Memory

```
Step  P Reg.  Mem. Cont.        Instruct.
000                             IDENT   BEBOOT
001                     *
002                     *
003                     *       DISPLAY THE KEYS AS FOLLOWS:
004                     *
005                     *       BITS    MEANING
006                     *       0=1     IPL LOADED FROM ASR, FORMAT 4* 4
007                     *       1=1     DISK, THEN
008                     *       2=1     MOVING HEADS
009                     *       2=0     FIXED HEADS
010                     *       3=1     I/O BUS
011                     *       3=0     MULTIPLEX
012                     *       4 to 7  BOU LINE (4 RIGHTMOST BITS)
013                     *       8=1     MULTI DEVICE CONTROLLER
014                     *       8=0     SINGLE DEVICE CONTROLLER
015                     *       9=1     CDD DISK
016                     *       10 to 15 DEVICE ADDRESS
017                     *
018                     *
019                     *
020                     *       DESCRIPTION
021                     *
022                     *       REBOOT LOADS ONE RECORD ONTO LOCATION /80 THEN START AT /84
023                     *       THE RECORD IS THE SECTOR # 1 IF DISK, OR 254 CHARACTERS OF THE
024                     *       INPUT DEVICE, LEADING NULL CHARACTERS IGNORED
025                     *
026                     *
027                     *
028                     *       USED REGISTERS :
029                     *
030                     *       A1 BOU LINES, NOT TO BE DESTROYED IF BOOT IS CALLED AGAIN
031                     *       A2 ADDR OF INR INSTRUCTION
032                     *       A3 ADDR OF CIO INSTRUCTION(WHICH IS DESTROYED AND NEEDS TO BE
033                     *                  RESTORED IF BOOT IS CALLED AGAIN)
034                     *       A4 ADDR OF SST INSTRUCTION
035                     *       A5 MULTIPLEX: CONTENTS OF 1ST WORD TO BE SENT TO EXT REGISTER
036                     *          IO BUS : CHARACTER COUNT, INITIALIZED AT 254 AND DECREMENTED
037                     *       A6 MULTIPLEX: CONTENTS OF 2ND WORD TO BE SENT TO EXT REGISTER
038                     *                  (LOADING ADDR)
039                     *          IO BUS: ADDR OF NEXT CHAR TO BE LOADED, INIT AT /80 AND
040                     *                  INCREMENTED
041                     *       A7,A8 WORK REGISTERS
042                     *       A9 WORK REGISTER
043                     *       A10 TO A14 NOT USED
044                     *       A15 CONTAINS THE KEYS'VALUE
045                     *
046                     *
047                     *
048                     *
049                     *
050                     *
051                     *       28/8/73 ARE FIXED:
052                     *       MULTIPLEX DLBLE WORD INITIALIZATION
053                     *       SST INST FOR MULTIPLE DEVICE CONTROLLER
054                     *
055                             EJECT
056                             ADRG    0
057                     *
058                     *
059                     BOOT    EQU     *
060                     *       INITIALIZE REGISTERS
061   0000  0200        F       LDK     A2,INR    ADDR OF INR INSTRUCTION
062   0002  0300        F       LDK     A3,CIO    ADDR OF CIO INSTRUCTION
063   0004  0400        F       LDK     A4,SST    ADDR OF SST INSTRUCTION
064                     *                         EXTRACT DEVICE ADDR AND INIT I/O COMMANDS
065   0006  861E                LDR     A6,A15
066   0008  263F                ANK     A6,/3F    DEVICE ADDR
067   000A  9629                ADRS    A6,A2     INITIALIZE I/O INSTRUCTIONS
068   000C  962D                ADRS    A6,A3
069   000E  9641                ADS     A6,HIO
      0010  0000        F
070                     *                         EXTRACT CONTROLLER ADDR AND INIT WER INST
071   0012  871E                LDR     A7,A15
072   0014  3FC8                SLC     A7,8      MULTI OR SINGLE DEVICE CONTROLLER
073   0016  5600        F       RF(6)   INIT20    SINGLE ONE
074   0018  260F                ANK     A6,/F     MULTIPLE ONE
075                     INIT20  EQU     *         INITIALIZE MULTIPLEX DBLE WORD:
076   001A  9631                ADRS    A6,A4     SST INSTRUCTION
077   001C  3E41                SLL     A6,1
078   001E  9641                ADS     A6,WER1   SET UP WER INSTRUCTIONS
      0020  0000        F
079   0022  9641                ADS     A6,WER2
      0024  0000        F
```

Step	P Reg.	Mem. Cont.		Instruct.		
080			*			LOAD A1 WITH BOU CONTENTS
081	0026	811C		LDR	A1,A7	
082	0028	0550		LDK	A5,80	MULTIPLEX DOUBLEWORD: LOAD 80 CHAR INTO
083			*			LOCATION /80
084	002A	0680		LDK	A6,/80	
085			*			CHECK IF DISK
086	002C	3FE7		SRC	A7,7	
087	002E	5600	F	RF(6)	NODISK	NO
088			*			FIXED HEADS ?
089	0030	3FC1		SLC	A7,1	
090	0032	5600	F	RF(6)	NOSEEK	YES
091	0034	0103		LDK	A1,3	SEEK ZERO
092	0036	41C0	CIO	CIO	A1,1,0	CIO SEEK ZERO
093			NOSEEK	EQU	*	
094	0038	811E		LDR	A1,A15	
095	003A	3966		SRL	A1,6	SECTOR NUMBER
096	003C	213C		ANK	A1,/3C	
097	003E	8520		LDKL	A5,/80CD	1ST WORD OF MULTIPLEX FOR DISK DEVICE
	0040	80CD				
098			NODISK	EQU	*	
099			*			EXECUTE WER, WHATEVER THE CHANNEL IS
100			WER1	EQU	*	
101	0042	7500		WER	A5,0	
102			WER2	EQU	*	
103	0044	7601		WER	A6,1	
104	0046	F031		EXR*	A4	SST
105	0048	F02D		EXR*	A3	
106	004A	5C06		RB(4)	* -4	
107	004C	871E		LDR	A7,A15	
108	004E	3F43		SLL	A7,3	
109	0050	5600	F	RF(6)	SST	MULTIPLEX
110			*			
111			*			IO BUS
112			*			
113	0052	8194		LDR	A9,A5	IF A9=A5 IGNORE LEADING CHAR.
114			INR	EQU	*	
115	0054	4F00		INR	A7,0,0	READ ONE CHAR
116	0056	5C04		RB(4)	* -2	
117	0058	E994		CWR	A9,A5	LEADING CHAR?
118	005A	5400	F	RF(4)	INR10	NO
119	005C	27FF		ANK	A7,/FF	CHECK IF NULL
120	005E	580C		RB(0)	INR	YES, IGNORE
121			*			NO, CHECK IF 4* 4
122			*			
123			INR10	EQU	*	
124	0060	879E		LDR	A15,A15	4* 4
125	0062	5600	F	RF(6)	STORE	NO 8+8
126	0064	3F44		SLL	A7,4	YES, 4* 4
127	0066	809C		LDR	A8,A7	SAVE LEFT BITS
128	0068	F029		EXR*	A2	READ NEXT CHARACTER
129	006A	5C04		RB(4)	* -2	
130	006C	270F		ANK	A7,/F	GET 4 RIGHT MOST BITS
131	006E	9702		ADR	A7,A8	
132			STORE	EQU	*	
133	0070	E739		SCR	A7,A6	STORE CHAR
134	0072	1601		ADK	A6,1	NEXT CHAR ADDR
135	0074	1D01		SUK	A5,1	COUNT DONE ?
136	0076	5924		RB(1)	INR	NO
137			*			YES
138			*			
139	0078	4180	HIO	CIO	A1,0,0	
140			*			
141			STATUS	EQU	*	
142	007A	4FC0	SST	SST	A7,0	
143	007C	5C04		RB(4)	* -2	
144	007E	0F84		AB	/84	
145			*			
146			*			
147			*			
148				END	BOOT	

SYMBOL TABLE

BOOT	0000	A	INR	0054	A	CIO	0036	A	SST	007A	A
HIO	0078	A	INIT20	001A	A	WER1	0042	A	WER2	0044	A
NODISK	0042	A	NOSEEK	0038	A	INR10	0060	A	STORE	0070	A
STATUS	007A	A									

ASS.ERR. 00000

:EOF

2.79 A0-A15 -- Scratchpad

These sixteen 16-bit accumulators comprise 15 working registers (A0-A14) and the stack pointer (A15). The working registers are used as an operand for some instructions. Fifteen registers (A1-A15) are program addressable. The scratchpad (Figure 2-8 MM) is controlled by the A-bus selection commands, μA0-4. The complete command code for scratchpad addressing and function is given in Table 2-9. For the write-scratchpad modes, the contents of the L register (L00-15) are loaded in the selected address (A0-A15). For read-scratchpad modes, the inverted contents of the selected address are gated onto the A-bus.

2.80 The 16-word scratchpad comprises four 64-bit read/write memory chips, type 7489. These circuits provide data inversion (active high input, low output) and open-collector outputs with a high-level off-state when μA0 to the chip-select input is 1 (scratchpad not selected). The scratchpad write-enable input, WSPN, from the start logic (Figure 2-8 RR), is active from the center of clock time T6 to T7, if μA0,A1 = 01.

2.81 The four-bit scratchpad address (SPA0-3) is selected through four type 74151A eight-input multiplexers. The first four sets of inputs are wired to +5 or 0 volts to obtain the direct address code of A0, A1, A2, or A15. The inputs 4, 5, or 6 select different fields of the instruction word to address the scratchpad : the R1/R3 field is provided by buffered K05-08/K05-07 (K08 is given via K0008BUFN if K00 = 1, indicating format-1 instruction); the R2 field is provided by K11-14N; the K12-15 field gives the number of shifts (in complement form). The seventh input selects the CT counter for addressing successive scratchpad registers.

2.82 The five-bit CT counter (Figure 2-8 MM) is used to count repeat cycles for the sequensor control, or (for P857) to address sequential scratchpad registers during Multiple Load or Store instructions. The counter comprises a type 74161 BCD counter for the four least-significant bits (CT0). A buffer at the output of the counter maintains the scratchpad address while the counter is being incremented. The buffer copies CT at the trailing edge of each AP pulse.

Counter operation is controlled by microinstruction bit μCT and general-field bit GCTLDN, as follows :

μCT (H=1)	GCTLDN (L=1)	Function
0	0	No change
0	1	Load CT1-4 from SPA0-3; CT0 from K11
1	0	Count CT at each T3N

The counter is preset to 16 (CT0-4 = 10000) by KRYN during each instruction Fetch cycle. Other initial counts less than 16 may be loaded into CT1-4 via the scratchpad address selector.

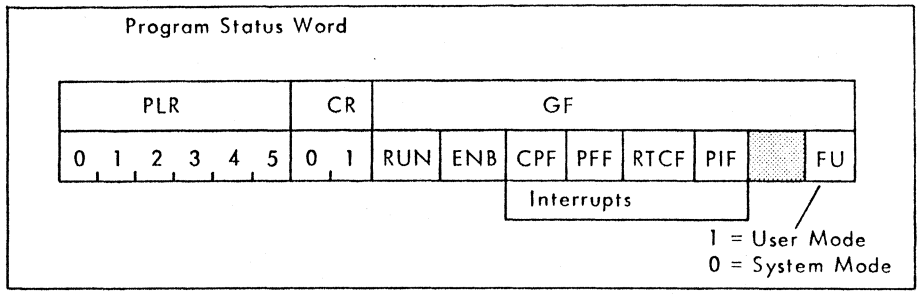
2.83 The number of shifts to be performed are loaded in complement form from the K12-15 field and effectively decremented by the counter operation. The counter is loaded with (R2) for the Double Arithmetic instructions in T1D addressing mode, enabling the least-significant operand word to be processed first. For DAR and DSR instructions in T1D addressing mode, (R2) + 1 addressing is obtained by the CT counter providing the least-significant address bits to the scratchpad. Multiply and Divide instructions count from the preset count of 16. The CTEND signal is generated when the count reaches 31 (CT0-4 = 11111). CTEND is used by the Sequensor to end the repeat cycles.

2.84 PSW -- Program Status Word

The PSW is a 16-bit status word comprising the priority level register (PLR), condition register (CR), and general flip-flops (GF). The complete PSW is saved in the stack, via the A-bus, during the following :

- Interrupt routine
- Trap routine
- Page Fault
- Call Function (CFR)
- Halt (HLT)
- Inhibit Interrupt (INH)
- Reset Internal Interrupt (RIT)
- Enable Interrupt (ENB)
- Link to Monitor (LKM)
- Set Mode (SMD)

During a Return (OPC14) instruction, System Mode (A15), the PLR, the CR, and the ENB and FU-bits of GF are restored from the stack to the PSW; the other bits of GF are not changed by the Return. During a Return instruction, User Mode ($\overline{A15}$), only CR is restored from the stack.



RESTORED FROM STACK AFTER:	
RTN (A15)	RTN ($\overline{A15}$)
PLR	PLR
CR	
ENB	(ENB unchanged)
FU	

2.85 PLR -- Priority Level Register

The PLR (Figure 2-8 NN) is a 6-bit register that stores the priority level code of the running program for the Interrupt logic. This register, comprising two type 74175 circuits, is preset to priority level 63 by the system master-clear signal MCLN. The register output, PLR0-5, is used by the Interrupt logic (paragraph 2.97) for comparison with Interrupt Requests. If an Interrupt Request is accepted, the Interrupt Routine is initiated : the contents of the PLR are saved in the stack with the rest of the program status word, and the PLR is loaded with the new program's interrupt level by INTAD0-5 via the C selector.

2.86 CR -- Condition Register

The 2-bit condition register (Figure 2-8 NN) indicates the result of various CPU operations. The condition register flip-flops are updated at each BP clock time (BPQ). The CR input conditions (Table 2-11) are selected by a pair of type 74175A 8-input multiplexers, with the selection controlled by microinstruction bits μCR0-2.

Table 2-11. CR Input Conditions

CR INPUT SELECTION

Selection μCR0,1,2	Mnemonic	Input to CR		Function
		CR0	CR1	
0 0 0	CRNC	CR0	CR1	No change
0 0 1	CRRTN	BIO06R	BIO07R	CR load during Return
0 1 0	CRIO	Timeout	ACBN	Programmed channel loading
0 1 1	CRFLO	FLOCR0	FLOCR1	Floating Point loading
1 0 0	CRLOG	ROMCR1	ROMCR5	Logic operation loading
1 0 1	CRADD	ROMCR2	ROMCR6	Addition operation loading
1 1 0	CRSUB	ROMCR3	ROMCR7	Subtraction operation loading
1 1 1	CRCMP	ROMCR4	ROMCR8	Compare operation loading

CR INPUT ROM CODE

	ROM Addressing					ROM Output to CR Input Selector			
	0ALUL	0ALUR	ALU00N	A00N	M00N	LOGIC CR1,5	ADD CR2,6	SUB CR3,7	COMP CR4,8
	0	0	0	0	0	1 0	1 0	1 0	1 0
	0	0	0	0	1	1 0	1 0	1 0	1 0
	0	0	0	1	0	1 0	1 0	1 1	0 1
	0	0	0	1	1	1 0	1 1	1 0	1 0
	0	0	1	0	0	0 1	1 1	0 1	0 1
	0	0	1	0	1	0 1	0 1	1 1	1 0
	0	0	1	1	0	0 1	0 1	0 1	0 1
	0	0	1	1	1	0 1	0 1	0 1	0 1
	0	1	0	0	0	1 0	1 0	1 0	1 0
	0	1	0	0	1	1 0	1 0	1 0	1 0
	0	1	0	1	0	1 0	1 0	1 1	0 1
	0	1	0	1	1	1 0	1 1	1 0	1 0
	0	1	1	0	0	0 1	1 1	0 1	0 1
	0	1	1	0	1	0 1	0 1	1 1	1 0
	0	1	1	1	0	0 1	0 1	0 1	0 1
	0	1	1	1	1	0 1	0 1	0 1	0 1
	1	0	0	0	0	1 1	1 1	1 1	1 1
	1	0	0	0	1	1 1	1 1	1 1	1 1
	1	0	0	1	0	1 1	1 1	1 1	1 1
	1	0	0	1	1	1 1	1 1	1 1	1 1
	1	0	1	0	0	0 1	1 1	0 1	0 1
	1	0	1	0	1	0 1	0 1	1 1	1 0
	1	0	1	1	0	0 1	0 1	0 1	0 1
	1	0	1	1	1	0 1	0 1	0 1	0 1

not used

	ROM Addressing					ROM Output to CR Input Selector			
	0ALUL	0ALUR	ALU00N	A00N	M00N	LOGIC CR1,5	ADD CR2,6	SUB CR3,7	COMP CR4,8
1	1	1	0	0	0	1 1	1 1	1 1	1 1
	1	1	0	0	1	1 1	1 1	1 1	1 1
	1	1	0	1	0	1 1	1 1	1 1	1 1
	1	1	0	1	1	1 1	1 1	1 1	1 1
	1	1	1	0	0	0 0	1 1	0 0	0 0
	1	1	1	0	1	0 0	0 0	1 1	1 0
	1	1	1	1	0	0 0	0 0	1 1	0 1
	1	1	1	1	1	0 0	0 0	0 0	0 0
	-	-	-	-	-	1 1	1 1	1 1	1 1

not used

1 : OVF + Enable input

Input 0 copies the previous CR contents (no change). Inputs 1-3 select conditions for Return, programmed channel loading, and Floating Point loading.

2.87 Inputs 4-7 are selected for arithmetic operations, and the input conditions are provided by a type-7488A read only memory (ROM). One specific pair of the eight ROM output bits is selected for the type of arithmetic operation being performed (logic, addition, subtraction, or compare). The 2-bit condition codes are selected from one of 32 ROM addresses by : the sign bit of the two ALU operands, A00N and M00N; the sign of the result, ALU00N; and the zero contents of the result for both left and right characters, 0ALUL and 0ALUR.

2.88 An overflow condition, set into the OVF flip-flop, sets CR to 3 (11_2) by switching off the enable input to the ROM to produce an all-Ones output. The overflow condition is tested by two series-connected multiplexers (the 8-input 75141 and the quad 2-input 74157), as follows :

74157			74151					
Input	Select A00		In	Select K01	ALU00	A01	Function	
(+5V) 1 μMLOAD	0 (11) 1 (10)		0 2	0 0	1 0	1 1	overflow OK	Shift
μMLOAD (+5V) 1	0 (11) 1 (10)		1 3	0 0	1 0	0 0	OK overflow	
GCRDSRN OVFMUN	0 (11) 1 (10)		4 5	1 1	1 1	1 0	overflow OK	Divide
(+5V) 1 GCRDSRN	0 (11) 1 (10)		6 7	1 1	0 0	1 0	OK overflow	

OVFMUN = GMULTI.$\overline{\text{ALUS0}}$.M00

The OVF signal fed back to the input-selection enable, prevents changing the overflow condition once an overflow has been set. The overflow flip-flop must be reset by command bit GCRVZ0N. The K01 input is 0 for Op-codes less than 8 to select shift instructions, or 1 for Op-codes of 8 or higher to select Multiply, Divide, or Double instructions. The shift instructions set overflow (via 74151A inputs 0, 3) on the test A01N ⊕ A00N to indicate a changing sign bit. The Divide instructions, specified by command bit GCRDSRN, set overflow (via 74151A inputs 4,7) on the test ALU00N ⊕ A00, indicating that the quotient is greater than one word.

2.89 GF -- General Flip-Flops

These seven general control flip-flops (Figure 2-8 PP), which can be program controlled, are part of the program status word (PSW). All GF bits are stored in the stack along with the rest of the PSW, but only the FU (User Mode) is restored from the stack by the Return instruction.

GF	PSW Bit	Function	Loaded at CLG (set or reset)	Set by	Reset by
RUNF	8	Main CPU status pointer	L08	STARTF.T1	GFRZ0 +(PREQ.RUN.T1)+(FTDEL.$\overline{\text{RUN}}$)+RSLF
ENBF	9	Enable interrupts	L09	GFENBN.$\overline{\text{MCLN}}$	GFSYSN
CPF	10	Operator's Interrupt	L10	(CPINT+V24INT).T1	MCLN
PFF	11	Power Failure Interrupt	$\overline{\text{M11}}$ resets	PWF ∫	PWF.RSLF.UNLOCK
RTCF	12	Real Time Clock Interrupt	L12	RTCFZ1N from C.Panel	MCLN
PIF	13	Op-Code (Program) Interrupt	L13	GSTOV.STOV from ALU	MCLN
FU	15	User Mode (0=System Mode)	CLPLR.C15	L15.CLG	GFSYSN+MCLN

Program control of the GF bits is by the A-bus command signal AEPSWN (at clock time T8). AEPSWN selects the program status word (with GF) to the A-bus and gates the L-register data back into the GF. The AEPSWN.T8 control signal CLG gates L08-10, 12, 13, 15 to the respective GF bits. GF bit 11 (PFF) is reset at that time if M11 = 0. Bit 11 uses the M-register rather than the L-register because of the required polarity. In addition to the program control of the GF bits, asynchronous set and reset inputs are provided to each flip-flop.

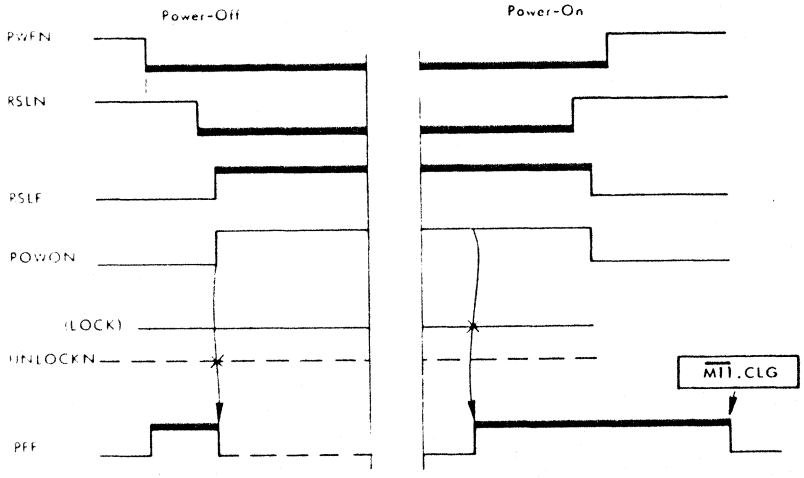
2.90 RUNF. This is the primary machine-state pointer (refer to Figure 1-8). The RUNF flip-flop is set at time T1 by the Start Command from the control panel. The RUNF flip-flop can be reset by any one of four ways :

- command bit GFRZ0;
- a Preset Address Compare from the control panel, at time T1;
- control-panel command Not Run, enabled by the buffered FETCH signal, FTDEL;
- RSLF which is set during the power-off sequence.

2.91 ENBF. This Enable-Interrupt flip-flop is set (with GFENBN) by the Enable Interrupt (ENB) instruction and reset (with GFSYSN) by the Inhibit Interrupt (INH) instruction. ENBF is also set or reset (with GFENBN) by the Return instruction when R2 = 15, and in function with ENB of the restored PSW.

2.92 CPF. This Operator's Interrupt can be set either by the INT switch on the control panel or by the interrupt signal BRGFN generated by the V24/Serial control unit. CPF is reset either by an RIT instruction with bit 0 = 0 (I10 = 0 during the CLG clock) or by the MCLN signal.

2.93 PFF. The Power Failure Interrupt flip-flop is set at the start of a power failure by the leading edge of the PWFN signal from the power supply; PFF is then reset during the power-off sequence if the key switch is set to any unlock position (OFF, ON, ONRTC). The Power Failure Interrupt flip-flop is set during the power-on sequence if the key switch is set to LOCK. PFF is reset by an RIT instruction with bit 11 = 0 (M11 = 0 during the CLG clock).



2.94 RTCF. The Real Time Clock Interrupt flip-flop is set by the RTCFZIN signal from the control panel. RTCFZIN is a one-microsecond signal generated once every 20ms by the power supply, and set via the control-panel key switch ONRTC or LOCK positions. The RTCF flip-flop is reset by an RIT instruction with bit 12 = 0 (L12 = 0 during the CLG clock) or by the MCLN signal.

2.95 PIF. The Operation-Code (Program) Interrupt flip-flop is set by a stack overflow condition or by the Link to Monitor (LKM) instruction to switch from User Mode to System Mode. Stack overflow (STOV from the arithmetic unit) sets PIF during memory stack operations (command bit GFSTOV) when the stack pointer decrements to less than 128_{10}. The LKM instruction sets PIF via the load input, with L13 = 1. The PIF flip-flop is reset by an RIT instruction with bit 13 = 0 (L13 = 0 during the CLG clock) or by the MCLN signal.

2.96 FU. The User Mode flip-flop is set during the Return A15 instruction if the previously-interrupted program was in User Mode (CLPLR.C15); the CLPLR signal loads the priority level register from the C-selector during the Return instruction, and C15 indicates the state of FU during the previous interrupt. The User Mode flip-flop is also set by the Set Mode (SMD) instruction (L15 = 1 during the CLG clock). FU is reset, to System Mode, by the Inhibit Interrupt (INH) instruction (with GFSYSN) or by the MCLN signal.

2.97 INTERRUPT LOGIC

The Interrupt logic (Figure 2-4 and 2-8 SS) generates the Scan External Interrupt signal (SCEIN), tests for internal and external interrupt requests, and initiates the Interrupt routine when a request is received of a higher priority than the running program. Refer to paragraph 1.16 for a description of the complete interrupt system. The Enable Interrupt control flip-flop, ENBF, is located with the general flip-flops (GF), along with the four dedicated internal interrupts : CPINTF, PFF, RTCF, and PIF.

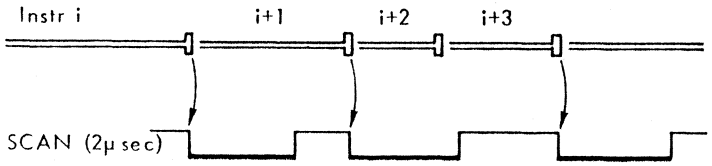
2.98 Internal Interrupts

Eight internal interrupt request lines (IS00-07N) are provided which have the highest system priority. At clock-time AP, all internal interrupt requests are

clocked into the two 74175 registers and are then available at the priority encoder 74148. If there are any internal interrupt requests waiting at the priority encoder, the low GS output switches the 74158 multiplexer to select the internal interrupts, and the high EO output (IECE) forces INTAD0,1 low (inactive). The highest-priority interrupt request is indicated by a 3-bit code at the 74148 A-outputs. The interrupt request code is switched through the 74158 multiplexer to the INTAD0-5 lines. The IECGSN signal is sent to the Start logic (Figure 2-8 RR) to enable setting the automatic restart flip-flop during the power-on/power-off sequences.

2.99 External Interrupts

A Scan External Interrupt (SCEIN) signal is generated during the status test at the end of each instruction, or during the Move instruction, if more than two microseconds have passed since the start of the previous scan. In order to validate the interrupt at the end of certain instructions, the microprogram does a 2.070 μsec wait before ending those instructions. (See Figure 1-13, Wait.)



The microinstruction control bits (Figure 2-8 SS) are NAETAN (μSNA0.1) for status test, and GMOVEN for the Move instruction. Either of these inputs puts a high on the D input of the FETAT flip-flop, if there is no pending Interrupt Request (Not IR). At time T3, FETAT is set and the FETATN output triggers the SCEIT single-shot. SCEIT is inverted to provide the 2μsec SCEIN signal to the GP bus.

2.100 The BIECINH flip-flop is triggered by T5 90ns after SCEIT is started. The low BIECINHN output is fed back to the OR'ed input of the single-shot to prevent SCEIT from being re-triggered. On the first T5 pulse after

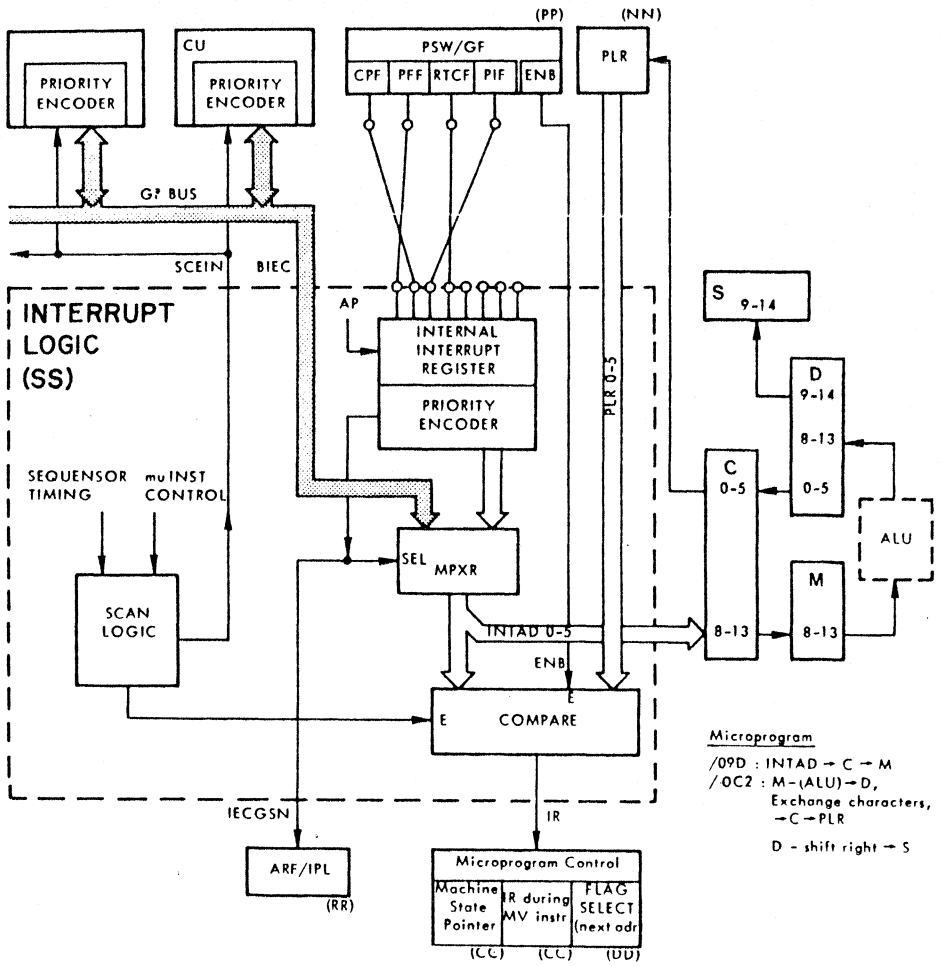


Figure 2-5 Interrupt System

the completion of the 2μsec SCEIT signal, BIECINH is reset, and the SCEIT single-shot is prepared for the next microinstruction-controlled start of a scan signal. The high BIECINH output applied to the most-significant input of the comparator inhibits comparison for 2μsec to wait for stabilization of the BIEC lines (propagation time plus selection of the highest priority level). IR could be sent between T3 and T5, but is never used during status test.

2.101 At the receipt of SCEIN, any CU with a pending interrupt request examines the BIEC lines. If there is no higher priority request, the CU's priority encoder puts the interrupt code on the BIEC0-5 lines. The BIEC code received at the Interrupt logic is switched through the 74158 multiplexer to the INTAD0-5 lines if there is no internal interrupt request.

2.102 Compare Interrupts

The highest-priority interrupt request (internal or external) is available at the INTAD0-5 lines. If the Enable Interrupt flip-flop ENBF is set and the BIECINH delay is completed, the INTAD lines are compared with the priority of the running program (stored in the priority level register PLR). BIECINH and ENBFN to the two most-significant inputs of the comparator must both be low to enable comparison. (The comparator inputs A3/B3 must compare equal before the A2/B2 inputs are tested, etc.; all four A and B inputs must compare before the cascade inputs from the lower-priority comparator are tested.) If the interrupt request on the INTAD lines is of higher priority (lower number) than the current PLR, the A<B output is activated to generate Interrupt Request signal IR.

2.103 The IR signal is sent to the Microprogram Control logic to initiate the Interrupt routine (Figure 2-5). The interrupt address on the INTAD0-5 lines is switched through the C and D selectors during the Interrupt routine to form part of the address in the S register and to reload the PLR with the new priority level.

2.104 SEQUENSOR (CPU CLOCK)

The Sequensor (Figure 2-8 EE) uses a crystal-controlled oscillator to drive twelve shift-register cells which provide the CPU timing signals :

- AP, T1, T2, T3, T4, T5, T6,
- BP, T7, T8, T9, T10.

The basic CPU clock signals are AP and BP. AP represents the beginning of a functional cycle (or microprogram) and is used to load the microinstruction address and read the microinstruction from the ROM control store; CPU logic controls and data paths are established by the command bits of the microinstruction. At each BP pulse time, the CPU logic executes the microprogram, according to the conditions established at AP time, and loads the results into the appropriate CPU registers.

2.105 Operating Modes and Cycles

The Sequensor operated in four different modes (Figure 2-6) controlled by microinstruction bits μSEQ0,1. Within the basic modes, the Sequensor operates in one of six cycles. Five of the operating cycles begin with the AP pulse; the sixth (Repeat cycle) begins and ends with the BP pulse, skipping AP. For internal CPU operations (LOGIC and REPEAT modes), the cycle lengths are controlled by controlling the generation of AP to begin the next cycle (pulses T7-T10 are inserted or deleted after BP as required). For all GP-bus cycles (SEQ BUS and SEQ BIO modes) and Floating Point execution, the cycle lengths are controlled by controlling the generation of T6 just before BP (pulse T5 may be repeated as a waiting loop until a synchronizing reply signal triggers T6).

2.106 Internal CPU Operations (AP Generation)

Four fixed-length Sequensor cycles are provided for the internal operations LOGIC mode :

- Logic cycle (360ns)
- Scratchpad cycle (405ns)
- Flag cycle (450ns)
- Fetch cycle (540ns)

mu SEQ 0,1	Mnemonic	Function
0 0	LOGIC	Internal CPU Operations
0 1	REPEAT	Short Execution Cycle
1 0	SEQBUS	GP-Bus Cycles
1 1	SEQBIO	I/O Cycles with Bus not released

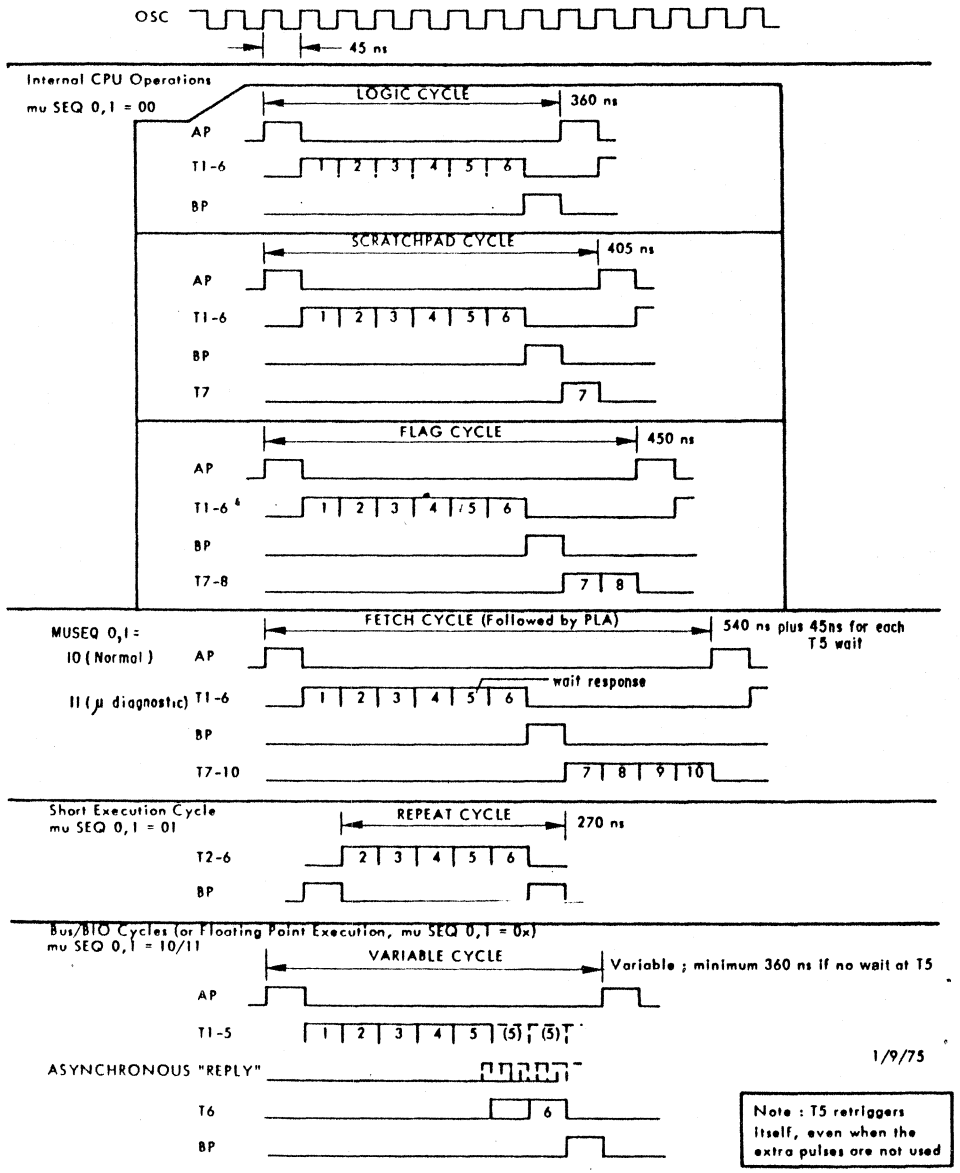


Figure 2-6 Sequensor Operating Cycles

All these cycles begin with AP and count directly through T1, T2, T3, T4, T5, T6, and BP. The time between BP and the end of the next cycle (next AP) is then controlled to provide the required execution time for the operation and to define all Next-Address data. The control is provided by a type 74151A multiplexer (APDN) which selects which clock pulse is to generate AP, as follows :

GFETCH	NAFLAGN	WSPRSLI	APDN Generation	
S2	S1	S0	Input	Function
0	0	0	T8	Flag Cycle (NAFLAG)
0	0	1	T8	
0	1	0	BP	Logic Cycle ($\overline{NAFLAG}$.WSP)
0	1	1	T7	Scratchpad Cycle ($\overline{NAFLAG}$.WSP)
1	0	0	T10	Fetch Cycle (GFETCH)
1	0	1	T10	
1	1	0	T10	
1	1	1	T10	

2.107 Logic Cycle. This cycle is used for register-to-register operations, with the result stored into a register other than the scratchpad. Input 13 of the APDN multiplexer is selected so that the AP pulse to begin the next cycle follows the BP pulse.

2.108 Scratchpad Cycle. This cycle is used for register-to-register operations with the result stored in the scratchpad. Data transfer from the L register to the scratchpad requires the extra clock pulse T7 between BP and the end of the cycle.

2.109 Flag Cycle. This cycle is used with a microinstruction that specifies Next-Address Flag mode. Two extra clock pulses (T7 and T8) are required to gate the Flag information onto the control-store address bus.

2.110 Fetch Cycle. The Sequensor fetch cycle is used during an instruction fetch cycle, where the Next Address must be decoded by the instruction-register PLA decoder. The timing required to decode the instruction word and to access the PLA needs four extra clock cycle (T7, T8, T9, T10) following BP.

2.111 Short Execution Cycle (No AP)

The Repeat cycle counts directly through T2, T3, T4, T5, T6, and BP without an AP or T1 clock pulse. This cycle is used for looping while the scratchpad CT counter counts. The microinstruction control inputs, with $\overline{\text{CTEND}}$, hold REPENDI high to gate the BP pulse directly to the T2 input. REPENDI also disables the APDN multiplexer to inhibit the AP pulse. The current microinstruction does not change during the Repeat cycles since AP is inhibited. When the CT counter reaches its full count of 31_{10}, CTEND forces REPENDI low and the APDN multiplexer is enabled to generate AP to begin the next cycle.

2.112 GP-Bus Cycles (T6 Generation)

Variable-length cycles are used for all GP-Bus operations and for Floating Point instruction executions. All these cycles begin with AP and count directly through T1, T2, T3, T4, and T5. The cycle-length parameters then control the generation of the T6 clock. The BP pulse and the succeeding AP pulse directly follow T6. The control of T6 is provided by a type 74151A multiplexer which selects the T6-enabling signal T6DN, as follows :

μSEQ0 S2	FLOACT S1	BSYDL S0	T6DN Generation Input	Function
0	0	0	1	Internal CPU operations (T6 follows T5)
0	0	1	1	
0	1	0	DONEF	Floating Point instruction execution
0	1	1	0	not used
1	0	0	0	
1	0	1	SYNCT6	Bus and Bus I/O cycles (SEQBUS, SEQBIO)
1	1	0	0	not used
1	1	1	0	

2.113 For the internal CPU operations, T6 directly follows T5. Sequensor control is provided through control of the AP pulse (preceeding paragraphs). The enabling One-bit is selected through the multiplexer by μSEQ0=0 and the floating point command bit FLOACT=0.

2.114 The Floating Point instruction execution is an operation that requires the DONEF response signal from the FPP before the cycle can be terminated. DONEF is selected directly at the I2 input of the T6DN multiplexer by μSEQ0=0, floating-point command bit FLOACT=1, and BSYDL=0. The FLOACT signal is the buffered microinstruction general-field bit GFLOT.

μSEQ	0,1	
	1 0	SEQBUS
	1 1	SEQBIO

2.115 For all GP Bus operations (SEQBUS and SEQBIO), the SYNCT6 input to the multiplexer is selected by μSEQ0=1, BSYDL=1, and FLOACT=0. The μSEQ0 bit = 1 for all Bus operations. BSYDL = 1 95ns after the CPU takes control of the GP Bus. The Sequensor does a waiting loop on the T5 clock until the required reply is received via the 8-input Nand gate SYNCT6. For Bus transfers that don't require memory exchange, the reply signal is provided by the Microprogram Control and T6 may directly follow T5. The reply signal (listed in Table 2-12) must be one of the following:

a. TRMN (SYNMEMN) must be received during a CPU/Memory exchange or during a CPU/External-Register exchange. The TRMN response signal (from Memory or External Register) on the Bus is received and gated by the Bus Controller logic (Figure 2-8 TT) to the Sequensor as input signal SYNMEMN.

b. TPMN delayed 190ns (TPMDLN) is received from the CU during a CU/Memory exchange under CPU control (programmed-channel transfer). The 190ns delay of TPMN is produced by Bus Controller logic for assuring data timing.

c. TIMEOUT generates T6 to end the cycle if no response is received to one of the Master-to-Slave signals TMRN, TMPN, TMEN within

6.48 µsec. This may indicate that the addressed Memory, Programmed Channel, or External Register is not present.

d. BIOEKEY gates T6 without extra T5 waiting loops during a control-panel to CPU transfer. BIOEKEY is generated on the Bus Controller logic (Figure 2-8 TT) by the microinstruction general-field bits GCRFNUN and GBOKFN, and gated into the Sequensor by GIDLEN.

e. GFETCHN general-field bit gates T6 without extra T5 waiting loops during instruction (K) register loading from the L register, via the Bus BIO lines. GFETCHN is gated by microinstruction control bit µTMRN to generate SYNIMN to the T6 input gate.

f. DONEMN is received from the MMU during an MMU/Memory exchange which is always under CPU control.

g. DONEFN is received from the FPP during an FPP/Memory exchange which is always under CPU control.

h. MFAULTN, delayed 120ns, from the MMU indicates a page fault (PAFN) during a Move Table instruction. The MFAULTN signal sets the PAF flip-flop in the control-store addressing logic (Figure 2-8 CC). The PAFN signal is delayed 120ns at the Sequensor input (SYNCT6) for control-store address timing.

i. BOFFN from the general-field bits GCRFNUN and GBOFN (Bus Controller logic) gates T6 without extra T5 waiting loops when FPP data is loaded, via the Bus BIO lines, into the CPU during a Fix instruction.

2.116 POWER FAILURE, RESTART, RESETS

The power-on and power-off sequences are shown on Figure 2-7. The logic is shown on Figure 2-8 RR, Start/Resets. While power is off, the Reset Logic (RSLN) signal is held at ground (active low) through a relay on the power supply.

2.117 Power-On Sequence

When the power supply is switched on, or when the mains power is restored after a failure, there is approximately an 850ms delay while the power supply stabilizes (Section 5, Power Sequence Logic) before RSLN goes inactive (high).

Table 2-12 Sequensor T6 Generation

µSEQ0	FLOACT	BSYDL	Cycle (text)	Synchronize T6 on :
S2	S1	S0		
0	0	x	Internal CPU operations	T5
0	1	0	Internal, Floating Point execution	DONEFN from FPP
1	0	1	GP Bus transfers with Memory exchange	
			CPU/Memory (a)	TRMN (SYNMEMN) from memory
			CPU/External Register (a)	TRMN (SYNMEMN) from memory
			Programmed Channel CU/Memory (b)	TPMN from CU, delayed 190ns
			Addressed Device Missing (c)	TIMEOUT, generated 6.48µsec after TMRN/TMPN/TMEN sent.
			MMU/Memory (f)	DONEMN from MMU *
			FPP/Memory (g)	DONEFN from FPP *
			Page Fault (h)	MFAULTN from MMU (PAFN), delayed 120ns. *
			GP Bus transfers without Memory exchange	
			Control Panel (d)	T5, if GBOKFN/GCRFNUN (BIOEKEY), and GIDLEN
			Fetch execution (e)	T5, if GFETCHN and µTMRN.
			Load from FPP (Fix execution) (i)	T5, if GBOFN (BOFFN) and GCRFNUN *
			any (a-i)	TIMEOUT, if required reply not received within 6.48 µsec

* Note - Signals (f,g,h,i) used with 857 only.

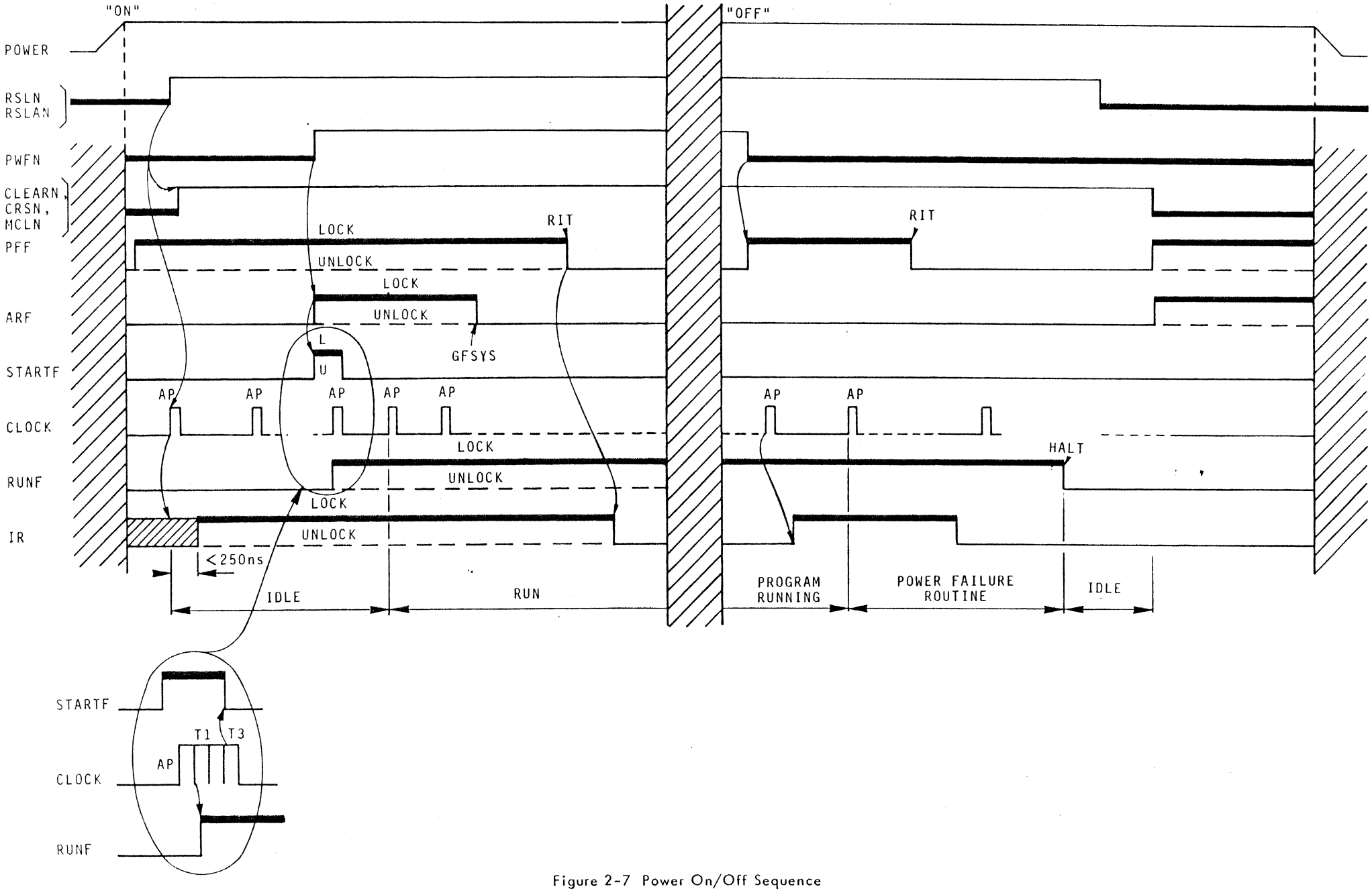


Figure 2-7 Power On/Off Sequence

When RSLN goes high, the OSCN pulse immediately resets RSLF to remove the logic reset condition. The inactive RSLAN/BN/CN signals to the Sequensor enable clock-pulses T1, T3, T5, T6, AP, BP, and the clock begins running.

2.118 Automatic Restart

Automatic restart is performed by the CPU if the control-panel key is at LOCK when the power comes on, therefore the key must be switched to LOCK when switching on or following a power failure while the key is not at LOCK. If the key is at LOCK when the +5 volts comes on to operate the flip-flops (and before RSLN, RSLF drop), PFF is set at the beginning of the power-on sequence (paragraph 2.93, PSW/GF, PFF). Beginning with the first AP, the internal interrupt request PFF is sampled by the Interrupt Logic. A level-0 (highest priority) Interrupt Request (IR) is then generated and the any-internal-interrupt signal IECGSN is active to the ARF flip-flop. The Power Failure (PWFN) signal from the power supply goes inactive (high) 0.5ms after RSLN goes inactive.

2.119 With the key at LOCK, the IECGSN signal sets Automatic Restart flip-flop ARF at the edge of the high-going PWFN signal. The ARFN output sets the STARTF flip-flop directly, via the asynchronous S-input. The RUNF flip-flop (2-8 PP) is set on the first T1 clock after STARTF is set. At the first AP after RUNF sets, the first microinstruction of the Automatic Restart routine (Figure 1-13) is read, and the CPU switches from Idle state to Run state. The second microinstruction of the Automatic Restart routine resets ARF with the GFENBN signal. The PFF flip-flop should be reset during the automatic restart subroutine by an RIT instruction.

2.120 Power-Off Sequence

The Power Failure (PWFN) signal is set by the power supply 10ms after detection of a mains loss, caused by power failure or by the key switched OFF. PWFN is sent via the GP Bus to the CPU and to any other elements on the Bus that must take action during power failure. The leading edge of PWF sets the PFF (GF/interrupt) flip-flop. This level-0 internal interrupt is detected by the Interrupt Logic at the first AP clock following the start of PWFN. The resulting Interrupt Request (IR) can initiate an interrupt subroutine for a power failure.

2.121 PWFN to the Bus Controller logic inhibits setting the OKVAL flip-flop. The Bus Controller thus denies requests by any other Master for Bus access, and the CPU has exclusive control of the Bus. The power failure subroutine requested by IR and PFF should commence with the second AP clock following PWFN. The subroutine should then reset PFF with an RIT instruction and reset RUNF with an HLT instruction. This saving subroutine must not last more than 2ms, and must end with a HLT instruction. The HLT instruction selects Microprogram Control address /177 to place the CPU in the Idle state. The Reset signal (RSLN) from the power supply is activated 3ms after PWFN.

2.122 Resets

The CPU logic is reset at the end of the power-off sequence by the RSLN signal from the power supply. RSLN is held active low while power is off. The first OSCN pulse after RSLN is active sets the RSLF flip-flop. RSLF activates RSLAN, RSLBN, RSLCN, and WSPRSLI, and resets the flip-flops STARTF, WSP, and RUNF. The RSLF-derived signals set or reset the CPU registers and flip-flops to their off states (Table 2-13) and hold them in that condition until the power-on sequence. The RSLN signal also activates the Master Clear signals CLEARN (to the Bus), MCL, and MCLN. Sequensor clock pulses are disabled by RSLF so that the CPU clock is stopped, although the oscillator-generated signal OSC runs continuously.

2.123 Master Clear

The Master Clear signal CPMCN can be generated by the control-panel MC switch if the key is <u>not</u> at LOCK and if the CPU is <u>not</u> in Run mode. The CPMCN signal (Figure 2-8RR) is OR'ed with the RSLF output to activate the signals CLEARN, MCL, and MCLN. CLEARN is sent on the GP Bus as a reset/initialize signal to all System elements. MCL is sent to the V24 CU on the CPU card. MCLN is used by the CPU (Table 2-13) to set the priority level register (PLR) to

Table 2-13 Resets and Clears

Logic-Resets, by RSLN/RSLF only

Logic	Sig.	Action
(RR)	RSLF	RSLAN,BN,CN → 1 STARTF → 0 WSPRSLI → 0
	WSPRSLI	WSP → 0
	RSLAN	ARFN → 0 IPLF → 0
(AA)	RSLBN	K-reg → 0
	RSLAN	KxxBUFN → 0
(BB)	RSLBN	RA0-8 → 0
(CC)	RSLAN	FTDEL → 0 KRY → 0
	RSLBN	PUPN → 0
(DD)	RSLBN	FSIG → 0 FSIGDIV → 0
(EE)	RSLBN	T1,T3,T5 → 0 TC810 → 0
	RSLAN	AP → 0 BP → 0 T6 → 0
	RSLCN	BPQ → 0
(JJ)	RSLCN	Q-reg → 0
(LL)	RSLBN	DWIF → 1
(NN)	RSLBN	OVF → 0 CR0,1 → 0
(PP)	RSLF	RUNF → 0
(SS)	RSLAN	BIECINH → 0 IF00-07 → 0
(TT)	RSLAN	BUSF → 0 DE → 0 FNU → 0 (DD) TMEF → 1 TMPF → 1 WRITFN → 0
	RSLBN	BIOELN → 1 BSYCPU → 0 CHFN → 1 FLOACT → 0 GBCPFN → 1 MADCPUN → 1 MADLCPUN → 1 MUBUSRFN → 1 OKVAL → 0 TMFN → 1 TMMN → 1 TMMU → 0 TMRF → 0
(PP)	RSLF.PWF.LOCK set interrupt flip-flop PFF	

Resets by Master Clear or RSLN/RSLF

(RR)	CPMCN or RSLAN	MCL → 1
	MCL	CLEARN → 1 MCLN → 1 V24 resets
(NN)	MCLN	PLR → level 63
(PP)	MCLN	ENBF → 1 CPINTF → 0 RTCF → 0 PIF → 0 FU → 0 CPGFZ0N → 1
	CPGFZ0N	CPGF → 0 V24 resets

level 63 and set the Enable Interrupt flip-flop ENBF. The GF flip-flops CPINTF, RTCF, PIF, and RU are all reset, and the control panel interrupt flip-flop CPGF is reset.

Table 2-14 CPU Signal LIST (A-C)

Signal	Logic	Comment
0ALUL,R,N	GG	
0ALURA	NN	
A00N-15N	LL,MM	A-Bus
A00AN	NN	
ABN	AA	
AC,N	NN	BUS(in)
ACAN	V24	
ACBN	NN	
ACHALTN	V24	
ACINR,N	V24	
ACOTRN	V24	
ACSOT,N	V24	
ACSST,N	V24	
ACSTARTN	V24	
AECONSTN	LL	
AEIPLN	LL	
AENBN	LL	
AEPN	LL	
AEPSWN	LL	
AESYSN	LL	
ALU00	FF	
ALU00N-15N	GG	
ALUCO04,08,12,16	GG	
AEPUPN	LL	
ALUCG00N,04N, 08N,12N	GG	
ALUCP00N,04N 08N,12N	GG	
ALUS0-3	GG	
ALUS0A-3A	GG	
ALUS0N-3N	FF	
AP,N,DN	EE	
AREDELA,N	V24	
AREDELBN	V24	
ARERCA,CB	V24	
ARF,N,D	RR	
ARFZ0N	RR	
ASR0-7	V24	
BOFFN	TT	Cmd - FPP
BOKFN	TT	
BOKIDLN	EE	
BOMFN	TT	
BIO00N-15N	KK	BUS(in/out)

Signal	Logic	Comment
BIO00AN-15AN	KK	
BIO00R-15R	KK	
BIOEKEY	TT	
BIOELN	TT	
BIOL	TT	
BIEC0-5	SS	input(ext.Int)
BIEC0R-5R	SS	
BIECINH,N	SS	
BP,N	EE	
BPLN	HH	
BPP	EE	
BPQ,N	EE	
BPS	KK	
BRC	AA	
BRGF,N	V24	
BSYCPU,N,AN	TT	
BSYDL	TT	
BSYN,R	TT	BUS(in/out)
BSYZ0N-1N	TT	
BUSF,N,AN	TT	
BUSFDEL,N	TT	
BUSFREN	TT	
BUSR,N	TT	BUS (in)
BUSRDEL	TT	
BUSRPFIN	TT	
C00N-15N	JJ	
CHA	TT	BUS
CHFN	TT	
CHIPER,D	V24	
CHPERZ0N	V24	
CLEARN	RR	BUS
CLEFTZ0	JJ	
CLF0N	V24	
CLG	PP	
CLK	AA	
CLMN	GG	
CLPLR	BB	CMD/G
CLTE0C	V24	
CLV24	V24	
COMVAL	V24	
CPBABS	LL	in from C.Panel
CPBRG	PP	
CPGFN	PP	
CPGFZ0N	PP	

Table 2-14 CPU Signal LIST (C-G)

Signal	Logic	Comment
CPINT,A	PP	in
CPINTF,N	PP	
CPINT4N	PP	
CPINZ1N	PP	
CPLR	LL	
CPMCN	RR	in from C.Panel
CPRR	LL	
CR0-1	NN	
CR0DN	NN	
CR1DN	NN	
CR0XK6	AA	
CR1XK7	AA	
CT0-4	MM	
CT101,102	V24	grounds
CT106,7,9	V24	
CT1082	V24	in for DNOTOP
CT133	V24	in for DREADYN
CT103,N	V24	in
CT104,N	V24	
CT0DN	MM	
CT0Z1N	MM	
CT1CO	MM	
CTBUF1N-4N	MM	
CTEND	MM	
CVN	AA	
CVKCR	AA	
D00-15	HH	
D00N-15N	HH	
D00DN	FF	
DE,N	TT	
DEBSYN	TT	
DEZ0N	TT	
DEZ1BPN	TT	
DES1T2N	TT	
DIVFLAG	FF	
DNOTOP	V24	CT1082 input
DONEF,N	EE	in from FPP
DONEMN	EE	in from MMU
DREADYN	V24	CT133 input
DS0-1	FF	
DS0N-1N	FF	
DWIF,Z0N	LL	
DWIN	AA	

Signal	Logic	Comment
ECHO,N	V24	
ECHOZ1N	V24	
ENBF,N	PP	
ENBFZ1N	PP	
ETATEST	CC	
F0-1,N	V24	
F0Z1N	V24	
F1Z0N	V24	
FACINR,N	V24	
FE,N	V24	
FECHO	V24	
FETATDN,EN	SS	
FETATN	SS	
FETCH	BB	
FHALT,N	V24	
FHALTZ0N,Z1N	V24	
FLAGDIV	DD	
FLAGN	DD	
FLOACT	TT	
FLOCR0-1	NN	in
FNU,N,D	DD	
FPPABS	AA	in from FPP
FSIG,N	DD	
FSIGDVD	DD	
FTBOF	EE	
FTDEL,N	BB,LL	
FTDERU	PP	
FTE0CN	V24	
FU	PP	User mode
FU15R2N	DD	
FUZ0N-Z1N	PP	
GAEXL,N	BB	CMD/G
GB0FN	BB	CMD/G
GB0KN	BB	CMD/G
GB0MN	BB	CMD/G
GBCHN	BB	CMD/G
GBCPFN	TT	
GBCPN	BB	CMD/G
GBEX,N	BB	CMD/G
GBTMEN	BB	CMD/G
GBTMFN	BB	CMD/G
GBTMMN	BB	CMD/G
GBTMPN	BB	CMD/G
GCRDSR,N	BB,FF	CMD/G

Table 2-14 CPU Signal LIST (G-M)

Signal	Logic	Comment
GCRFNU,N	BB,DD	CMD/G
GCRVMLN	BB	CMD/G
GCRVZ0,N	BB,DD	CMD/G
GCSELN	BB	CMD/G
GCT	MM	
GCTLDN	BB	CMD/G
GFENBN	BB	CMD/G
GFETCH,N	BB	CMD/G
GFKYZ0N	BB	CMD/G
GFLOT,N	BB	CMD/G
GFPLRN	BB	CMD/G to CLPR
GFRZ0,N	BB	CMD/G
GFSTOV,N	BB	CMD/G
GFSYSN	BB	CMD/G
GIDLEN	BB	CMD/G
CMOVEN	BB	CMD/G
CMULTI,N	BB,FF	CMD/G
GOSH	DD	
GOTOECH	V24	
GOTOWST	V24	
IEC0-2,N	SS	
IECE	SS	
IECGSN	SS	
IF00N-07N	SS	
IN	V24	
INRECH	V24	
INSTN	--	not used (C.Pan)
INTAD0-5	SS	Interrupt address
INTEPL	SS	
INTGPL	SS	
INTLPL	SS	
INTSERN	V24	
INTVAL	V24	
IPL,N	RR	in from C. Panel
IPLDEL	RR	
IPLF,N	RR	
IR,N	SS	
IS00N-07N	SS	in (Intern. Int's)

Signal	Logic	Comment
K00-15,N	AA	
K0008	AA	
K05-08BUFN	AA	
K08Q15	FF	
K10R2E0	AA	
K10R2N	AA	
K410N	AA	
K415N	AA	
K567	AA	
KFL0	AA	
KRY,N,DN	CC	
KRYZ0N-Z1N	CC	
L00-15	HH	
LOADMN	CC,LL	in from C. Panel
LOADRN	CC,LL	in from C. Panel
LSEL	FF	
M00N-15N	GG	
MAD00-15, 64,128	KK	
MADCPB	TT	
MADCPUN	TT	
MADLCPUN	TT	
MADLDN	TT	
MADLS	TT	
MADMMU,N,A	TT	
MADMUN	TT	
MADS	TT	
MCL,N	RR	
MFAULTN	CC	in fromMMU
MMUABS	TT	in from MMU
MOVE	CC	
MOVIRN	CC	
MSN	TT	BUS (in)
MSR	TT	
μA0-4	BB	CMD
μA0N-4N	LL	
μA1N	RR	
μADL0-4	BB	CMD
μBIOL,N	BB,TT	CMD
μBUSR,N	BB,TT	
μBUSRFN	TT	CMD
μC0-1	BB	CMD

Table 2-14 CPU Signal LIST (M-R)

Signal	Logic	Comment
μC0N	JJ	
μCR0-2	BB	CMD
μCT	BB	CMD
μGP0-4	BB	CMD to CMD/G
μGP1N	BB	CMD to CMD/G
μMLOAD	BB	CMD
μMSEL	BB	CMD
μNA0N-8N	BB	CMD
μNA7	AA	
MUNA7FUN	AA	
μP0-1	BB	CMD
μP0N	LL	
μQ0-1	BB	CMD
μS0-1	BB	CMD
μS0N	KK	
μSEQ0-1	BB	CMD
μSEQ1N	BB	CMD
μSNA0-1,N	BB	CMD
μTMRN	BB	CMD
μWRITE	BB	CMD
MVREADN	CC	
MVRML	CC	
NACND	AA	
NACNDAD	AA	
NADRT	CC	
NADRTMV	CC	
NAETAN	BB	CMD μSNA0.1
NAETAT	CC	
NAEXPL	CC	
NAFLAGN	CC	
NAFLG	CC	
NAFLGX	CC	
NAPLINH	CC	
NOFLON	AA	
NOJUMPN	AA	
NOVF	FF	
NXTCH,N	V24	
NXTCH0	V24	
ODEVPAR	V24	
OKO	TT	BUS
OKVAL	TT	
OR,ORB	V24	
OROPE	V24	

Signal	Logic	Comment
OSC,N	EE	
OSC90,N	EE	
OSCFLO	EE	
OTINECH	V24	
OTRECHN	V24	
OUT	V24	In/Out FF
OVDIVA,B	NN	
OVF,N,D	NN	
OVFMU,N	NN	
OVSHA,B	NN	
P00-14	LL	
PAFDELN	EE	
PAFN,Z0N	CC	
PARNB	V24	
PCO03,07,11N	LL	
PE,PEB	V24	
PFF,N	PP	
PFFZ0N, Z1N	PP	
PIF,N	PP	
PIFZ1N	PP	
PLOADN	LL	
PLA0-1, 0N	AA	
PLAVAL1	AA	
PLAVALN	AA	
PLR0-5	NN	
PM1	LL	
POVFN	FF	
POWQN	PP	
PREQN	PP	in from C.P.
PREQT1	PP	
PUPN,D	CC	
PWF,N	TT	in from P. Supply
PWFAN	PP	
Q00	JJ	
Q00N-16N	JJ	
Q15DN	JJ	
R1E0,N	AA	
R1E15	AA	
R2E0,N	AA	
R2E15	AA	
R110,N	V24	

Table 2-14 CPU Signal LIST (R-T)

Signal	Logic	Comment
R600,1200	V24	
R2400,4800	V24	
R9600	V24	
RA0-8	BB	
RAD0-8	AA,CC	Control Addr-Bus
RADET6N-T8N	CC	
RADETPLN	CC	
RADL3-4	FF	
RALUA1N-2N	FF	
RATESEL	V24	
RCP0N-3N	LL	in from C.Panel
RD08-15	V24	
RDA,N,1	V24	
RDADEL,N	V24	
RDARC	V24	
RDARN	V24	
READMN	CC,LL	in from C.Panel
READRN	CC,LL	in from C.Panel
READSTN	CC,LL	in from C.Panel
REPENDI	EE	
RFBN	AA	
ROMCR1-8	NN	
ROMCREN	NN	
ROMENB	BB	
RSLAN,BN,CN	RR	
RSL,N	RR	BUS (in from P.S.)
RSLF	RR	
RTCF,AN	PP	
RTCFZ1N	PP	in from P. Sup.
RUNF,N,A	PP	
RUNFZ0N,Z1N	PP	
RUNN	PP	in from C.Panel
RUNT3	RR	
S00-03	KK	
S00N-15N	KK	
SC003,07,11N	KK	
SCEIN	SS	BUS
SCEIT	SS	
SEQINH	V24	
SLOADN	KK	
SPA0-3	MM	
SPYC,A	TT	BUS
SPYCOKN	TT	
SPYCADEL	TT	
SSST	V24	
STAFCL,A	RR	
STAFZ0N	RR	
START,N	RR	in from C. Panel
STARTF	RR	
STOPNB	V24	
STOV	GG	
SYNCT6	EE	
SYNIMN	EE	
SYNMEMN	TT	
T 1-10	EE	
T1,3,5,6,8N	EE	
T2,5D	EE	
T2DREPN	EE	
T4T5N	EE	
T6DN,DEN	EE	
TC810,N	EE	
TDSN	V24	
TE0C	V24	
TESTN	CC	in from C.Panel
TIMEOUT,N	TT	
TMEF	TT	
TMEN	TT	BUS (in/out)
TMER,N	TT	
TMF,N	TT	
TMMOFN	TT	
TMMCY	TT	
TMMN	TT	
TMMU,D	TT	
TMPF	TT	
TMPN	TT	BUS (in/out)
TMPR,N	TT	
TMR,N	TT	BUS (in/out)
TMRF,D	TT	

Table 2-14 CPU Signal LIST (T-W)

Signal	Logic	Comment
TMRR,N	TT	
TOUTZ0N	TT	
TPMDLN	TT	
TPMN	TT	BUS (in/out)
TPMR	TT	
TPMRDEL	TT	
TRMN	TT	BUS (in/out)
TRMR	TT	
TROHLTN	V24	
TROUBLEN	V24	
TYAC	V24	
TYAD0-5	V24	address code
TYARE,N	V24	
UNLOCK,N	PP	in from C. Panel
VALK08N	V24	
VALNA0	CC	
WRITE	TT	BUS
WRITEFN	TT	
WSP,N	RR	
WSPRSLI	RR	

Table 2-15 Microinstruction Address Code

	Hexa	Binary
0	000	0000000000
	001	0000000001
	002	0000000010
	003	0000000011
	004	0000000100
	005	0000000101
	006	0000000110
	007	0000000111
	008	0000001000
	009	0000001001
10	00A	0000001010
	00B	0000001011
	00C	0000001100
	00D	0000001101
	00E	0000001110
	00F	0000001111
	010	0000010000
	011	0000010001
	012	0000010010
	013	0000010011
20	014	0000010100
	015	0000010101
	016	0000010110
	017	0000010111
	018	0000011000
	019	0000011001
	01A	0000011010
	01B	0000011011
	01C	0000011100
	01D	0000011101
30	01E	0000011110
	01F	0000011111
	020	0001000000
	021	0001000001
	022	0001000010
	023	0001000011
	024	0001001100
	025	0001001101
	026	0001001110
	027	0001001111
40	028	0001010000
	029	0001010001
	02A	0001010010
	02B	0001010011
	02C	0001010100
	02D	0001010101
	02E	0001010110
	02F	0001010111
	030	0001011000
	031	0001011001
50	032	0001011010
	033	0001011011
	034	0001011100
	035	0001011101
	036	0001011110
	037	0001011111
	038	0001111001
	039	0001111001
	03A	0001111011
	03B	0001111011
60	03C	0001111100
	03D	0001111101
	03E	0001111110
	03F	0001111111

	Hexa	Binary
64	040	0010000000
	041	0010000001
	042	0010000010
	043	0010000011
	044	0010001100
	045	0010001101
70	046	0010001110
	047	0010001111
	048	0010011000
	049	0010011001
	04A	0010011010
	04B	0010011011
	04C	0010011100
	04D	0010011101
	04E	0010011110
	04F	0010011111
80	050	0010100000
	051	0010100001
	052	0010100010
	053	0010100011
	054	0010101100
	055	0010101101
	056	0010101110
	057	0010101111
	058	0010111000
	059	0010111001
90	05A	0010111010
	05B	0010111011
	05C	0010111100
	05D	0010111101
	05E	0010111110
	05F	0010111111
	060	0011000000
	061	0011000001
	062	0011000010
	063	0011000011
100	064	0011001100
	065	0011001101
	066	0011001110
	067	0011001111
	068	0011010000
	069	0011010001
	06A	0011010010
	06B	0011010011
	06C	0011011100
	06D	0011011101
110	06E	0011011110
	06F	0011011111
	070	0011100000
	071	0011100001
	072	0011100010
	073	0011100011
	074	0011101100
	075	0011101101
	076	0011101110
	077	0011101111
120	078	0011111000
	079	0011111001
	07A	0011111010
	07B	0011111011
	07C	0011111100
	07D	0011111101
	07E	0011111110
	07F	0011111111

	Hexa	Binary
128	080	0100000000
	081	0100000001
130	082	0100000010
	083	0100000011
	084	0100001100
	085	0100001101
	086	0100001110
	087	0100001111
	088	0100010000
	089	0100010001
	08A	0100010010
	08B	0100010011
140	08C	0100011100
	08D	0100011101
	08E	0100011110
	08F	0100011111
	090	0100100000
	091	0100100001
	092	0100100010
	093	0100100011
	094	0100101100
	095	0100101101
150	096	0100101110
	097	0100101111
	098	0100111000
	099	0100111001
	09A	0100111010
	09B	0100111011
	09C	0100111100
	09D	0100111101
	09E	0100111110
	09F	0100111111
160	0A0	0101000000
	0A1	0101000001
	0A2	0101000010
	0A3	0101000011
	0A4	0101001100
	0A5	0101001101
	0A6	0101001110
	0A7	0101001111
	0A8	0101010000
	0A9	0101010001
170	0AA	0101010010
	0AB	0101010011
	0AC	0101011100
	0AD	0101011101
	0AE	0101011110
	0AF	0101011111
	0B0	0101100000
	0B1	0101100001
	0B2	0101100010
	0B3	0101100011
180	0B4	0101101100
	0B5	0101101101
	0B6	0101101110
	0B7	0101101111
	0B8	0101111000
	0B9	0101111001
	0BA	0101111010
	0BB	0101111011
	0BC	0101111100
	0BD	0101111101
190	0BE	0101111110
	0BF	0101111111

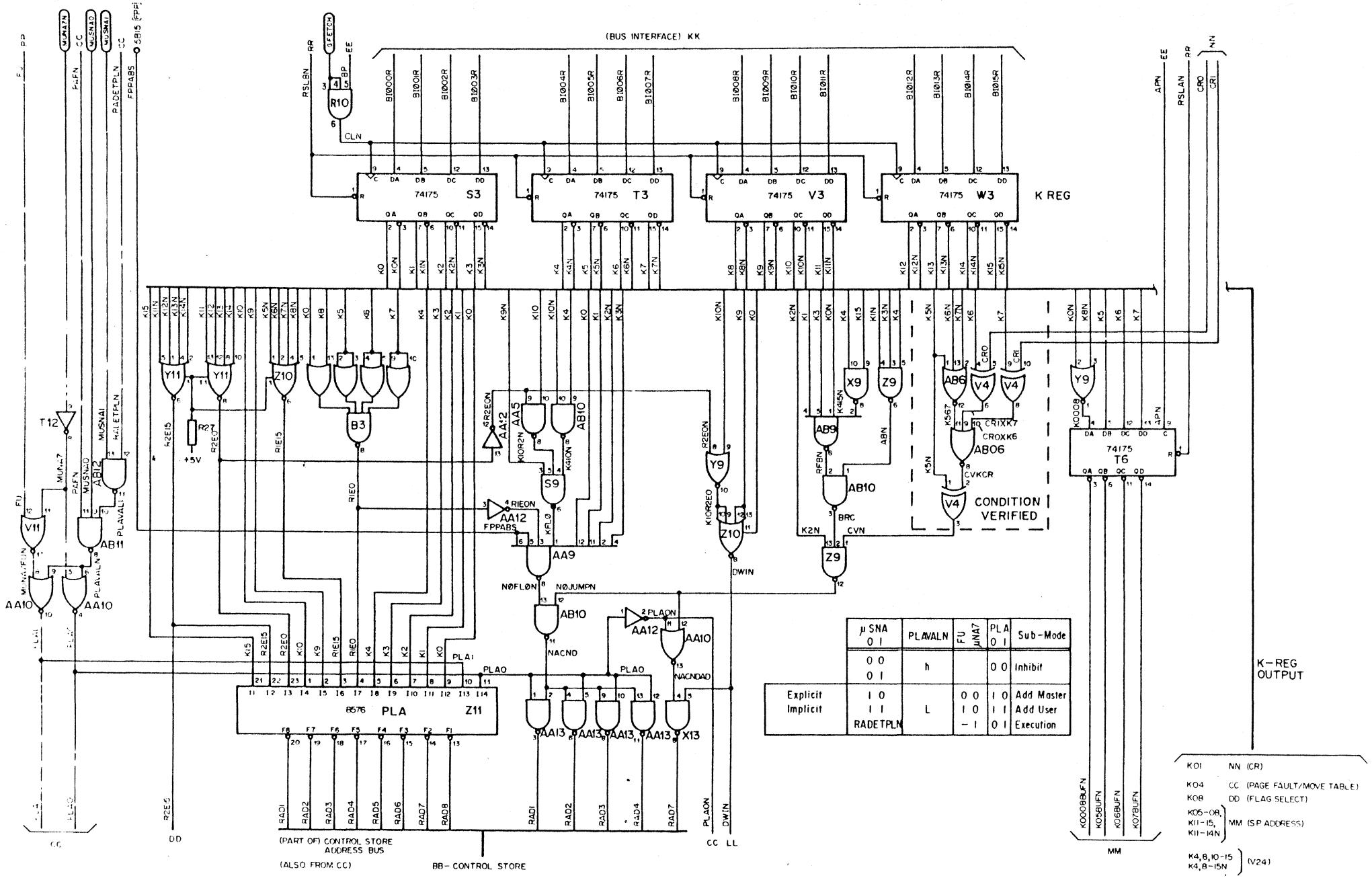
	Hexa	Binary
192	0C0	0110000000
	0C1	0110000001
	0C2	0110000010
	0C3	0110000011
	0C4	0110001100
	0C5	0110001101
	0C6	0110001110
	0C7	0110001111
200	0C8	0110010000
	0C9	0110010001
	0CA	0110010010
	0CB	0110010011
	0CC	0110011100
	0CD	0110011101
	0CE	0110011110
	0CF	0110011111
	0D0	0110100000
	0D1	0110100001
210	0D2	0110100011
	0D3	0110100011
	0D4	0110101100
	0D5	0110101101
	0D6	0110101110
	0D7	0110101111
	0D8	0110111000
	0D9	0110111001
	0DA	0110111010
	0DB	0110111011
220	0DC	0110111100
	0DD	0110111101
	0DE	0110111110
	0DF	0110111111
	0E0	0111000000
	0E1	0111000001
	0E2	0111000010
	0E3	0111000011
	0E4	0111001100
	0E5	0111001101
230	0E6	0111001110
	0E7	0111001111
	0E8	0111010000
	0E9	0111010001
	0EA	0111010010
	0EB	0111010011
	0EC	0111011100
	0ED	0111011101
	0EE	0111011110
	0EF	0111011111
240	0F0	0111100000
	0F1	0111100001
	0F2	0111100010
	0F3	0111100011
	0F4	0111101100
	0F5	0111101101
	0F6	0111101110
	0F7	0111101111
	0F8	0111111000
	0F9	0111111001
250	0FA	0111111010
	0FB	0111111011
	0FC	0111111100
	0FD	0111111101
	0FE	0111111110
	0FF	0111111111

	Hexa	Binary
256	100	1000000000
	101	1000000001
	102	1000000010
	103	1000000011
260	104	1000001100
	105	1000001101
	106	1000001110
	107	1000001111
	108	1000010000
	109	1000010001
	10A	1000010010
	10B	1000010011
	10C	1000011100
	10D	1000011101
270	10E	1000011110
	10F	1000011111
	110	1000100000
	111	1000100001
	112	1000100010
	113	1000100011
	114	1000101100
	115	1000101101
	116	1000101110
	117	1000101111
280	118	1000111000
	119	1000111001
	11A	1000111010
	11B	1000111011
	11C	1000111100
	11D	1000111101
	11E	1000111110
	11F	1000111111
	120	1001000000
	121	1001000001
290	122	1001000010
	123	1001000011
	124	1001001100
	125	1001001101
	126	1001001110
	127	1001001111
	128	1001010000
	129	1001010001
	12A	1001010010
	12B	1001010011
300	12C	1001011100
	12D	1001011101
	12E	1001011110
	12F	1001011111
	130	1001100000
	131	1001100001
	132	1001100010
	133	1001100011
	134	1001101100
	135	1001101101
310	136	1001101110
	137	1001101111
	138	1001111000
	139	1001111001
	13A	1001111010
	13B	1001111011
	13C	1001111100
	13D	1001111101
	13E	1001111110
	13F	1001111111

	Hexa	Binary
320	140	1010000000
	141	1010000001
	142	1010000010
	143	1010000011
	144	1010001100
	145	1010001101
	146	1010001110
	147	1010001111
	148	1010010000
	149	1010010001
330	14A	1010010010
	14B	1010010011
	14C	1010011100
	14D	1010011101
	14E	1010011110
	14F	1010011111
	150	1010100000
	151	1010100001
	152	1010100010
	153	1010100011
340	154	1010101100
	155	1010101101
	156	1010101110
	157	1010101111
	158	1010111000
	159	1010111001
	15A	1010111010
	15B	1010111011
	15C	1010111100
	15D	1010111101
350	15E	1010111110
	15F	1010111111
	160	1011000000
	161	1011000001
	162	1011000010
	163	1011000011
	164	1011001100
	165	1011001101
	166	1011001110
	167	1011001111
360	168	1011010000
	169	1011010001
	16A	1011010010
	16B	1011010011
	16C	1011011100
	16D	1011011101
	16E	1011011110
	16F	1011011111
	170	1011100000
	171	1011100001
370	172	1011100010
	173	1011100011
	174	1011101100
	175	1011101101
	176	1011101110
	177	1011101111
	178	1011111000
	179	1011111001
	17A	1011111010
	17B	1011111011
380	17C	1011111100
	17D	1011111101
	17E	1011111110
	17F	1011111111

	Hexa	Binary
384	180	1100000000
	181	1100000001
	182	1100000010
	183	1100000011
	184	1100001100
	185	1100001101
390	186	1100001110
	187	1100001111
	188	1100010000
	189	1100010001
	18A	1100010010
	18B	1100010011
	18C	1100011100
	18D	1100011101
	18E	1100011110
	18F	1100011111
400	190	1100100000
	191	1100100001
	192	1100100010
	193	1100100011
	194	1100101100
	195	1100101101
	196	1100101110
	197	1100101111
	198	1100111000
	199	1100111001
410	19A	1100111010
	19B	1100111011
	19C	1100111100
	19D	1100111101
	19E	1100111110
	19F	1100111111
	1A0	1101000000
	1A1	1101000001
	1A2	1101000010
	1A3	1101000011
420	1A4	1101001100
	1A5	1101001101
	1A6	1101001110
	1A7	1101001111
	1A8	1101010000
	1A9	1101010001
	1AA	1101010010
	1AB	1101010011
	1AC	1101011100
	1AD	1101011101
430	1AE	1101011110
	1AF	1101011111
	1B0	1101100000
	1B1	1101100001
	1B2	1101100010
	1B3	1101100011
	1B4	1101101100
	1B5	1101101101
	1B6	1101101110
	1B7	1101101111
440	1B8	1101111000
	1B9	1101111001
	1BA	1101111010
	1BB	1101111011
	1BC	1101111100
	1BD	1101111101
	1BE	1101111110
	1BF	1101111111

	Hexa	Binary
448	1C0	1110000000
	1C1	1110000001
450	1C2	1110000010
	1C3	1110000011
	1C4	1110001100
	1C5	1110001101
	1C6	1110001110
	1C7	1110001111
	1C8	1110010000
	1C9	1110010001
	1CA	1110010010
	1CB	1110010011
460	1CC	1110011100
	1CD	1110011101
	1CE	1110011110
	1CF	1110011111
	1D0	1110100000
	1D1	1110100001
	1D2	1110100010
	1D3	1110100011
	1D4	1110101100
	1D5	1110101101
470	1D6	1110101110
	1D7	1110101111
	1D8	1110111000
	1D9	1110111001
	1DA	1110111010
	1DB	1110111011
	1DC	1110111100
	1DD	1110111101
	1DE	1110111110
	1DF	1110111111
480	1E0	1111000000
	1E1	1111000001
	1E2	1111000010
	1E3	1111000011
	1E4	1111001100
	1E5	1111001101
	1E6	1111001110
	1E7	1111001111
	1E8	1111010000
	1E9	1111010001
490	1EA	1111010010
	1EB	1111010011
	1EC	1111011100
	1ED	1111011101
	1EE	1111011110
	1EF	1111011111
	1F0	1111100000
	1F1	1111100001
	1F2	1111100010
	1F3	1111100011
500	1F4	1111101100
	1F5	1111101101
	1F6	1111101110
	1F7	1111101111
	1F8	1111111000
	1F9	1111111001
	1FA	1111111010
	1FB	1111111011
	1FC	1111111100
	1FD	1111111101
510	1FE	1111111110
	1FF	1111111111



μ SNA 0 1	PLAVALN	FU	μNA7	PLA 0 1	Sub-Mode
0 0	h			0 0	Inhibit
0 1					
1 0			0 0	1 0	Add Master
1 1	L		1 0	1 1	Add User
RADETPLN			- 1	0 1	Execution

Explicit / Implicit

Figure 2-8AA Instruction Word Logic

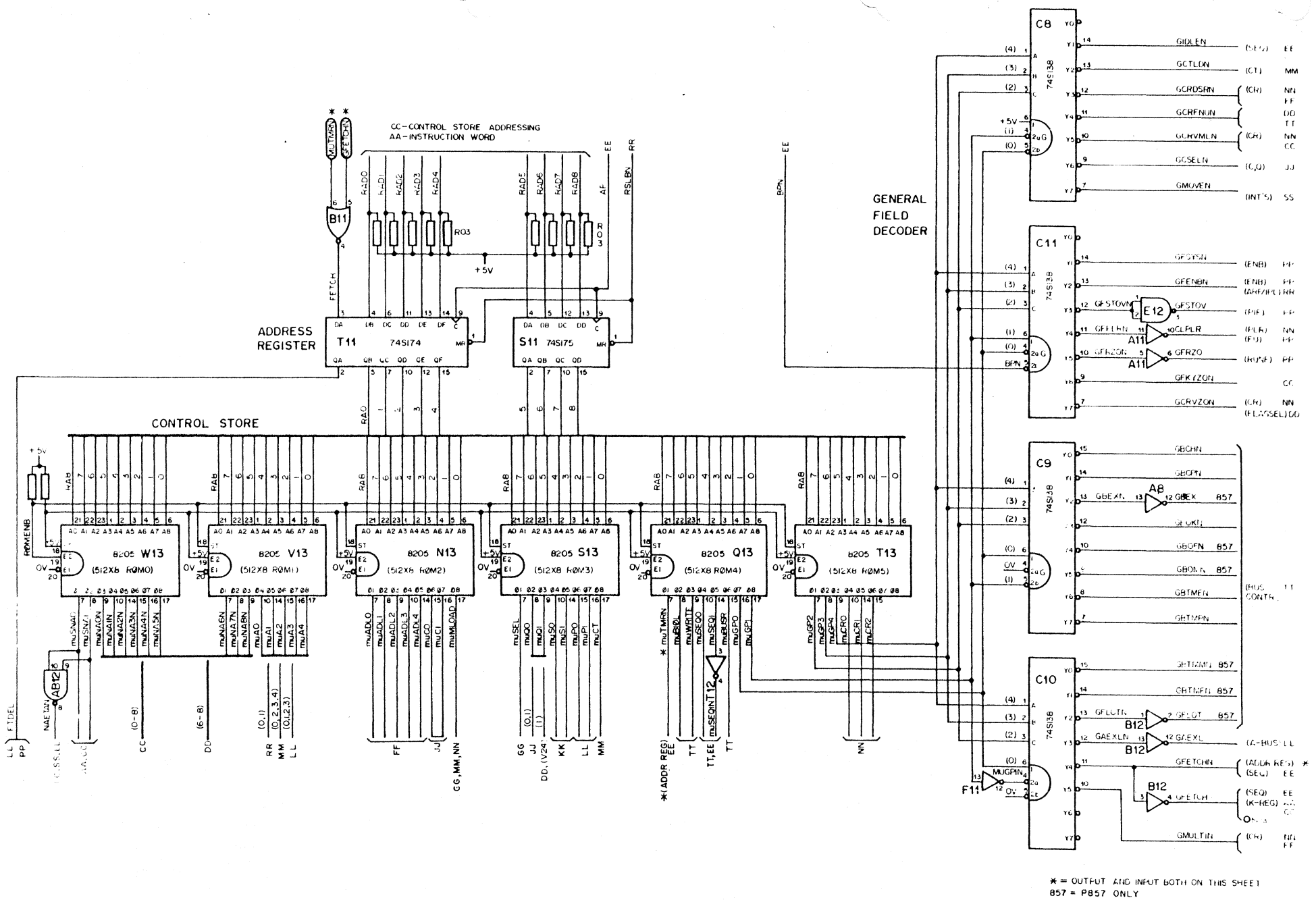
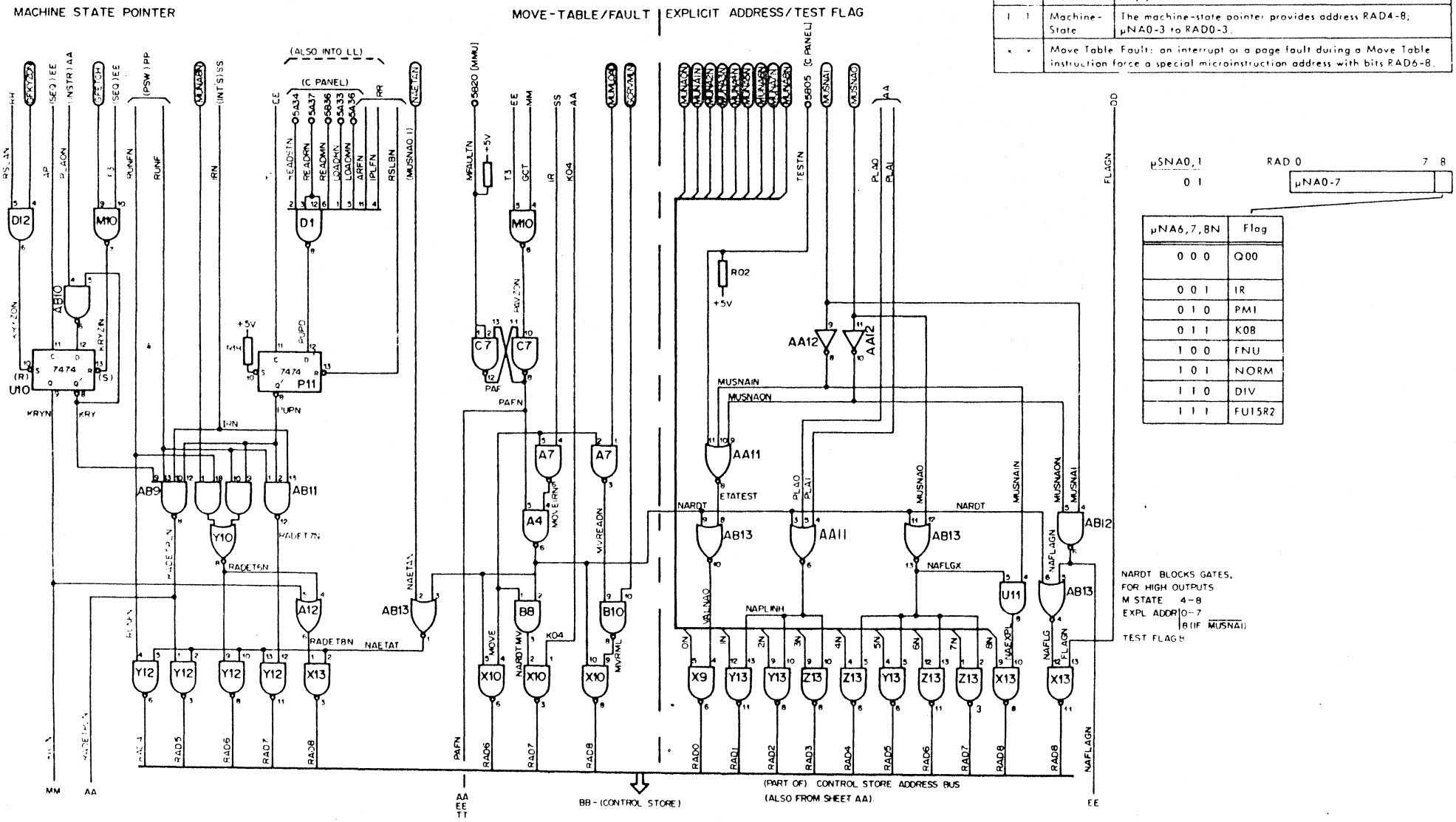
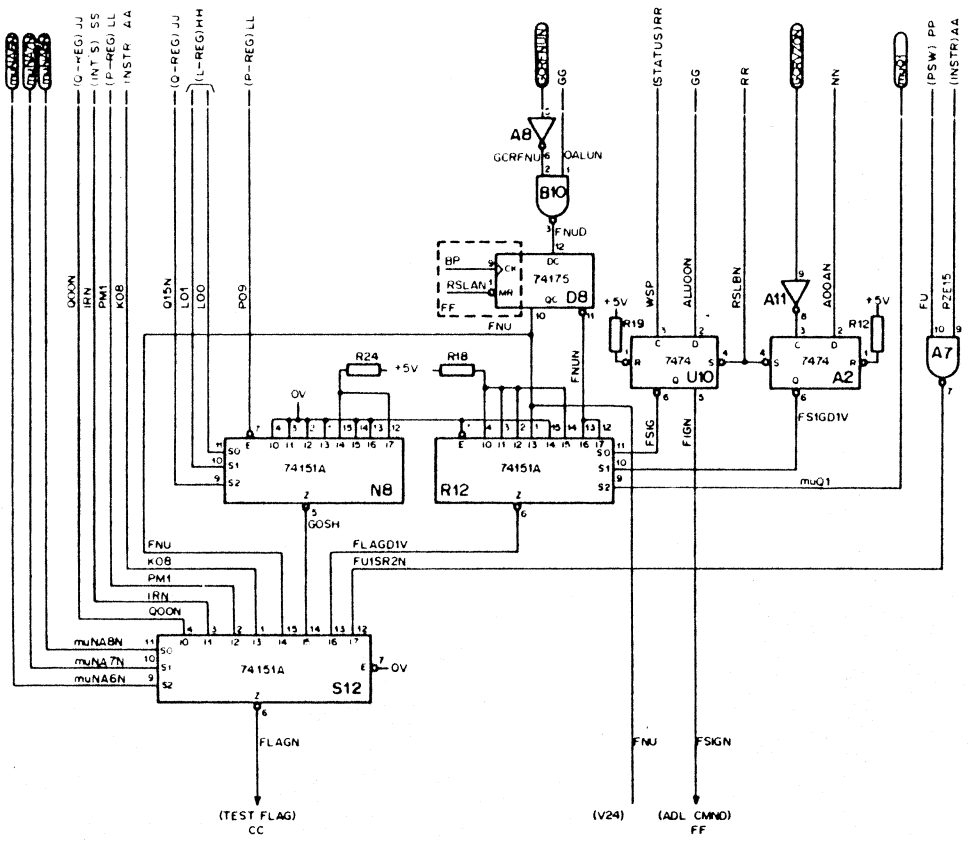


Figure 2-8BB Microcommand Control-Store Logic



μSNA0,1	Mode	Function
0 0	Explicit	Explicit address is μNA0-8.
0 1	Flag	Flag from execution-pointer tests (selected by μNA6-8) sets RAD8; μNA0-7 to RAD0-7.
1 0	Instruction Word (PLA)	Instruction word (K-reg, decoder) provides address RAD1-8; μNA7 modifies the decoder for fetch or execution.
1 1	Machine-State	The machine-state pointer provides address RAD4-8; μNA0-3 to RAD0-3.
x x	Move Table Fault: an interrupt or a page fault during a Move Table instruction force a special microinstruction address with bits RAD6-8.	

Figure 2-8CC Control Store Addressing



GOSH Select

Q15N S2	L01 S1	L00 S0		
L	0	0	0	0
L	0	1	1	0
L	1	0	2	0
L	1	1	3	0
h	0	0	4	+5
h	0	1	5	0
h	1	0	6	0
h	1	1	7	+5

FLAGDIV Select

	μQ1 S2	FSIGDIV S1	FSIG S0		
DIVB	0	0	0	0	+5
	0	0	1	1	+5
	0	1	0	2	+5
	0	1	1	3	FNU --- FSIGDIV.FSIG.FNUN
DIVA	1	0	0	4	0 --- FSIGDIV.FSIG
	1	0	1	5	+5
	1	1	0	6	FNUN
	1	1	1	7	FNUN --- FSIGFIV.FNU

Figure 2-8DD Flag Select

μSEQ0 S2	FLOACT S1	BSYDL S0	T6DN Generation Input	Function
0	0	0	1	Internal CPU operations (T6 follows T5)
0	0	1	1	
0	1	0	DONEF	Floating Point instruction execution
0	1	1	0	not used
1	0	0	0	
1	0	1	SYNCT6	Bus and Bus I/O cycles (SEQBUS, SEQBIO)
1	1	0	0	not used
1	1	1	0	

mu SEQ 0,1	Mnemonic	Function
0 0	LOGIC	Internal CPU Operations
0 1	REPEAT	Short Execution Cycle
1 0	SEQBUS	GP-Bus Cycles
1 1	SEQBIO	I/O Cycles with Bus not released

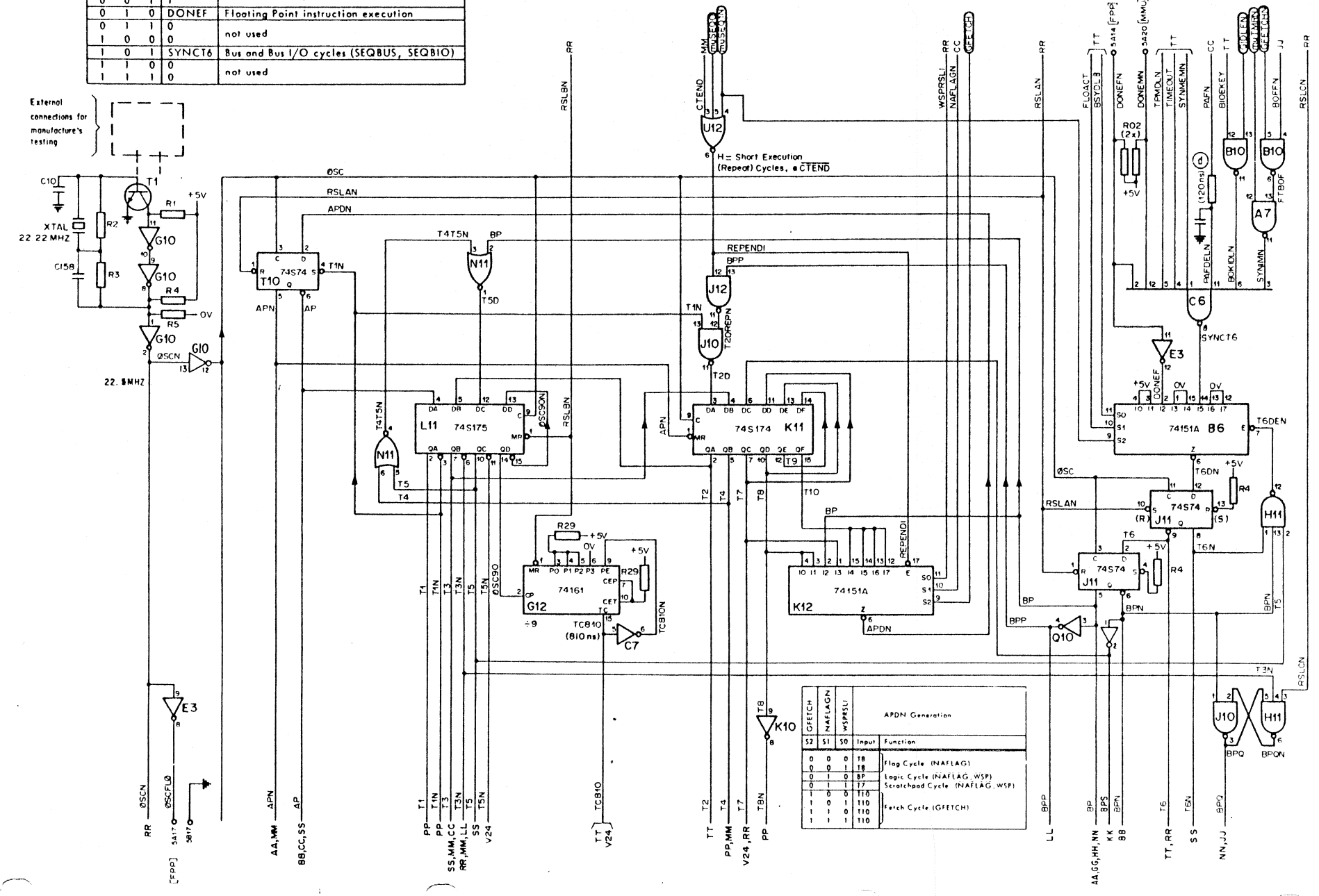
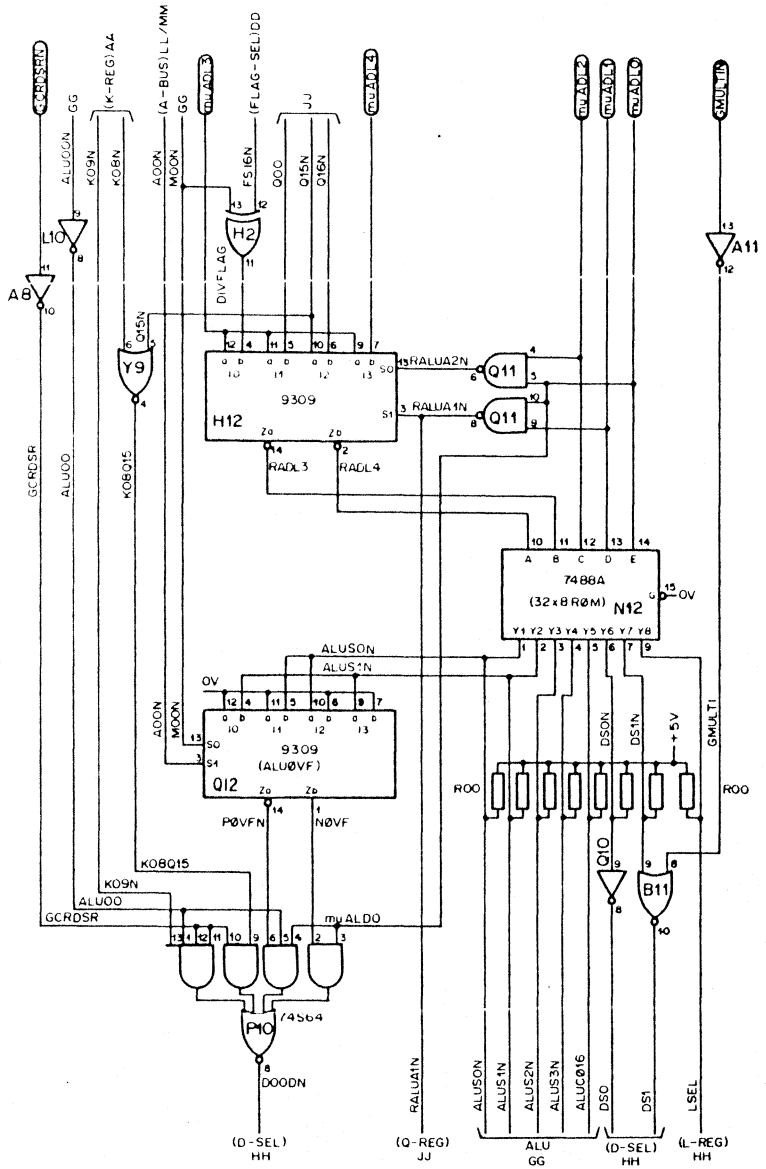


Figure 2-8FE Sequensor (CPU Clock)



H12 Multiplexer

Multiplexer Select Input				Multiplexer Output to ADL Command ROM	
μADL: 0, 1, 2			RALUA: 1N, 2N	RADL3 (B)	RADL4 (A)
0	0	0	1 1	μADL3N	μADL4N
0	0	1	1 1	μADL3N	μADL4N
0	1	0	1 1	μADL3N	μADL4N
0	1	1	1 1	μADL3N	μADL4N
1	0	0	1 1	μADL3N	μADL4N
1	0	1	1 0	Q15	Q16
1	1	0	0 1	μADL3N	FSIGN
1	1	1	0 0	μADL3N	DIVFLAGN

DIVFLAG = FSIGN ⊕ M00N

M Select (Logic GG)

Enable Clock	Select C or Q	Mnemonic	Data Source
μMLOAD	μMSEL		
0	-	No Op	Off; previously stored data available at output.
1	0	MYC	C 00 15
1	1	MYQ	Q 00 15
			M 00 15

D Select (Logic HH)

S1	S0	DS0, 1		
0	0 :	ALU 00-15N		ALU direct
0	1 :	ALU 08-15N	ALU 00-07N	Exchange ALU characters
		D00DN		
1	0 :		ALU 00-14N	ALU shift right
1	1 :		BIO 00-15AN	BIO direct
	D	00 07	08 15	N

L Select (Logic HH)

LSEL	Data Source		Function
0	D 00-15		D direct
1	D 01-15	Q00	D shifted left
L	00 —— 14	15	

ALU Function Table (Logic GG)

	ADL-Control ROM						
μADL4	ALUCO16	ALUSO-----3				Operation	
CE	CIN	S3	S2	S1	S0		
0	0	1	0	0	1	A plus B	ARITHMETIC
0	0	1	0	1	1	A or B	
0	0	1	1	0	0	A plus A	
0	1	0	0	0	1	A and B	
0	1	0	0	1	1	Zero	
0	1	0	1	1	0	A minus B	
1	-	0	1	0	1	B inverted	LOGIC
1	-	1	0	0	1	A ⊕ B	
1	-	1	0	1	0	B	
1	-	1	1	1	1	A	
1	-	1	0	0	1	A ⊕ B + 1	

Control signals are all active high. Functions are for active-low data in and out.

Figure 2-8FF A, D, L Command Logic

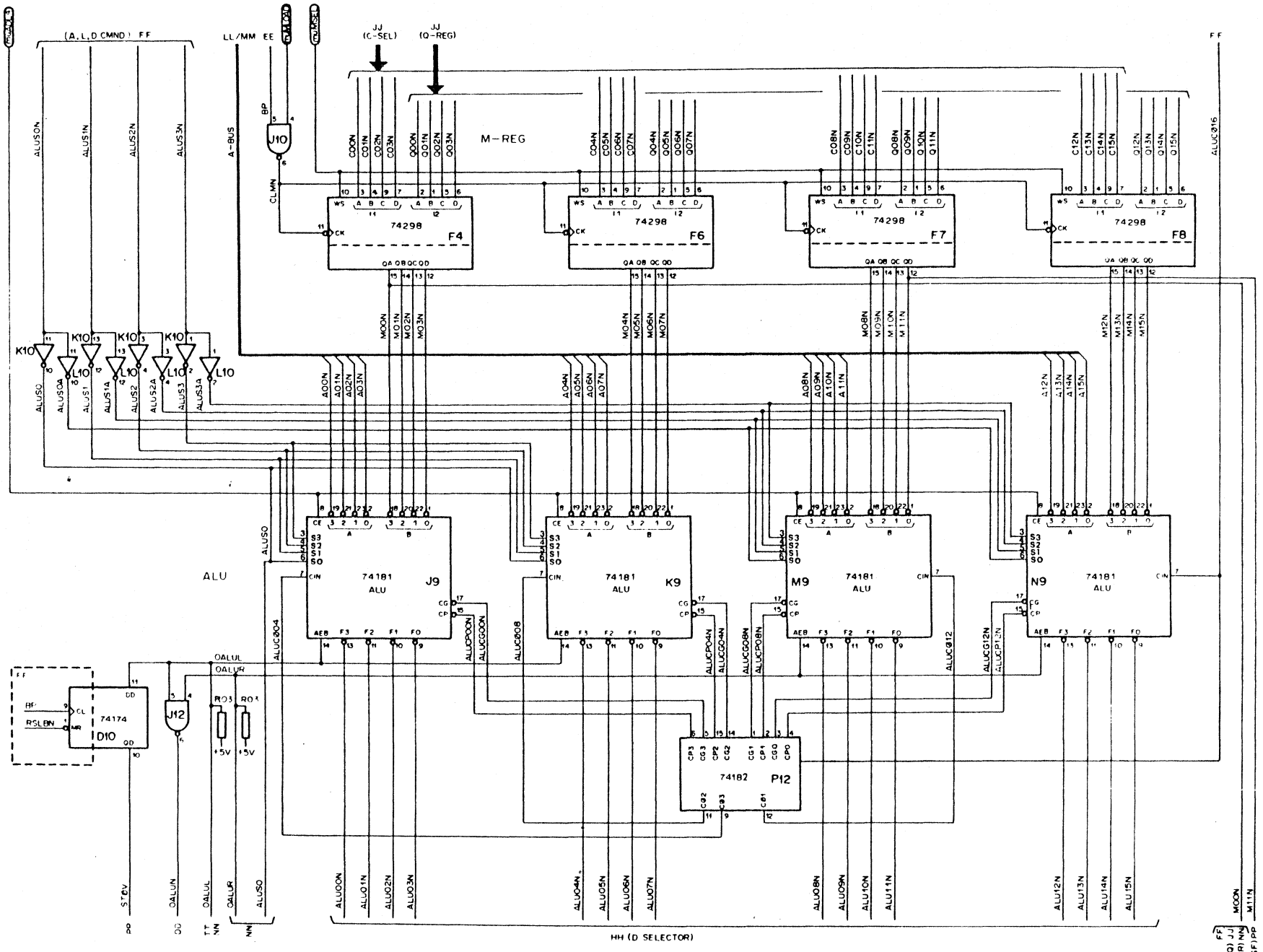


Figure 2-8GG ALU, M Register

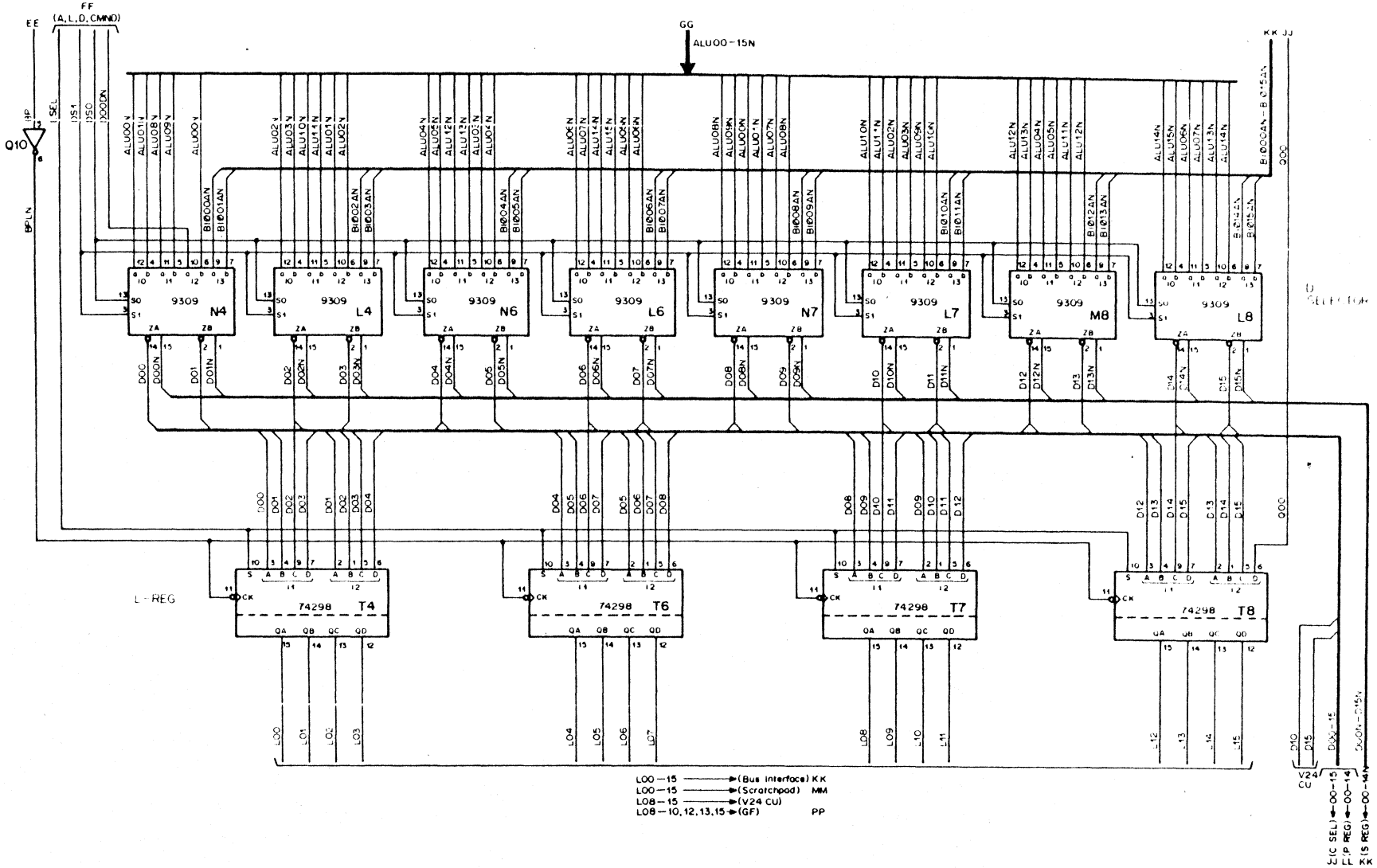
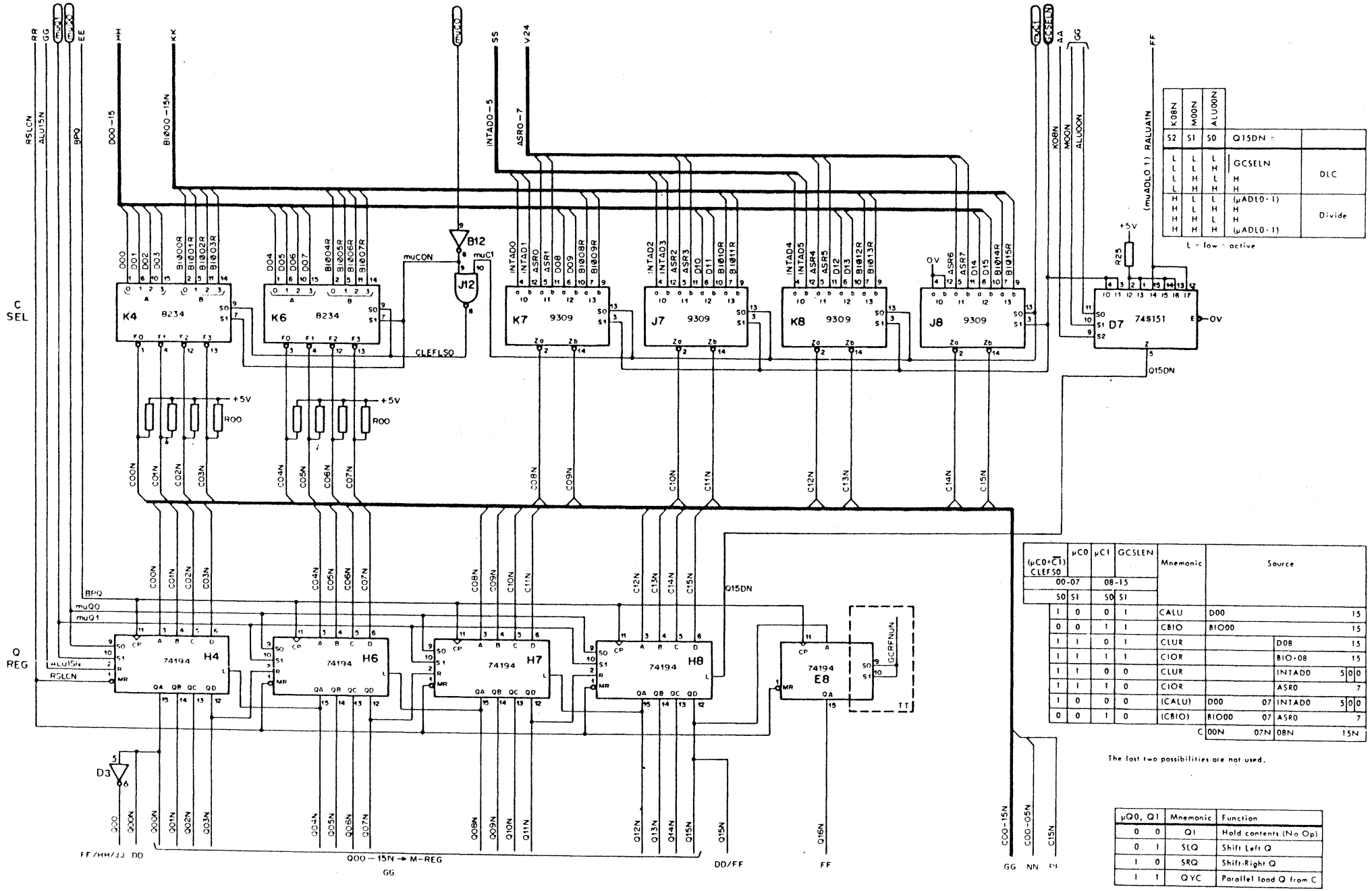


Figure 2-8HH D-Selector, L-Register



K0BN	M0ON	ALU0ON		
S2	S1	S0	Q15DN =	
L	L	L	GCSELN	DLC
L	L	H	H	
L	H	H	H	
H	L	L	(μADL0-1)	Divide
H	L	H	H	
H	H	L	H	
H	H	H	(μADL0-1)	

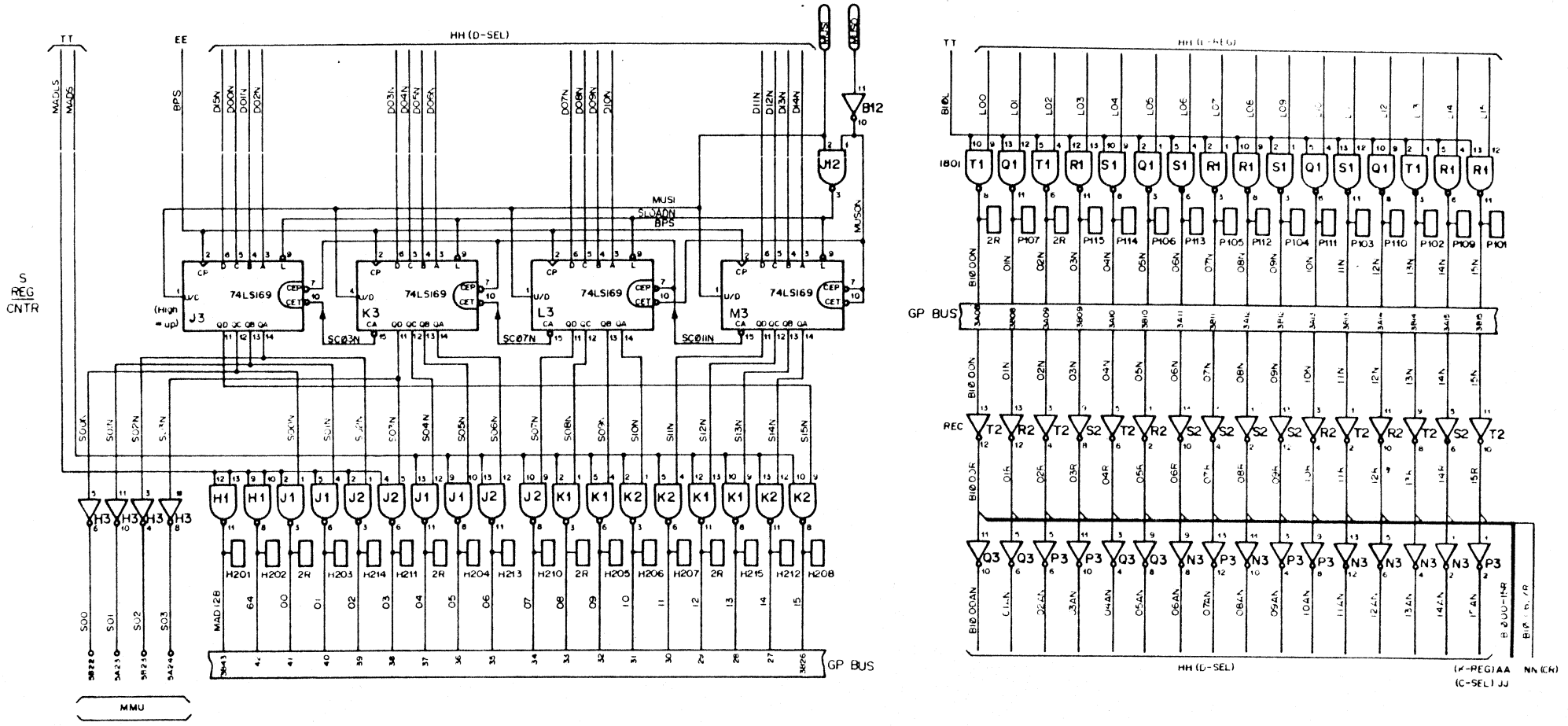
L = low = active

(μC0+C1) CLEFS0		μC0	μC1	GCSLEN	Mnemonic	Source		
00-07		08-15						
S0	S1	S0	S1					
1	0	0	1		CALU	D00		15
0	0	1	1		CBIO	BIO00		15
1	1	0	1		CLUR		D08	15
1	1	1	1		CIOR		BIO-08	15
1	1	1	0		CLUR		INTAD0	5 0 0
1	1	1	0		CIOR		ASR0	7
1	0	0	0		(CALU)	D00 07	INTAD0	5 0 0
0	0	1	0		(CBIO)	BIO00 07	ASR0	7
				C	00N	07N	08N	15N

The last two possibilities are not used.

μQ0, Q1		Mnemonic	Function
0	0	Q	Hold contents (No Op)
0	1	SLQ	Shift Left Q
1	0	SRQ	Shift-Right Q
1	1	QYC	Parallel load Q from C

Figure 2-8JJ C-Selector, Q-Register



µS0, S1	Mnemonic	Function
0 0	SI	Inhibit counting or loading
0 1	SYD	Load S0-15N with D0-15N
1 0	SP2	S plus 2 (count down)
1 1	SM2	S minus 2 (count up)

Figure 2-8KK S-Register/Counter, Bus Interface

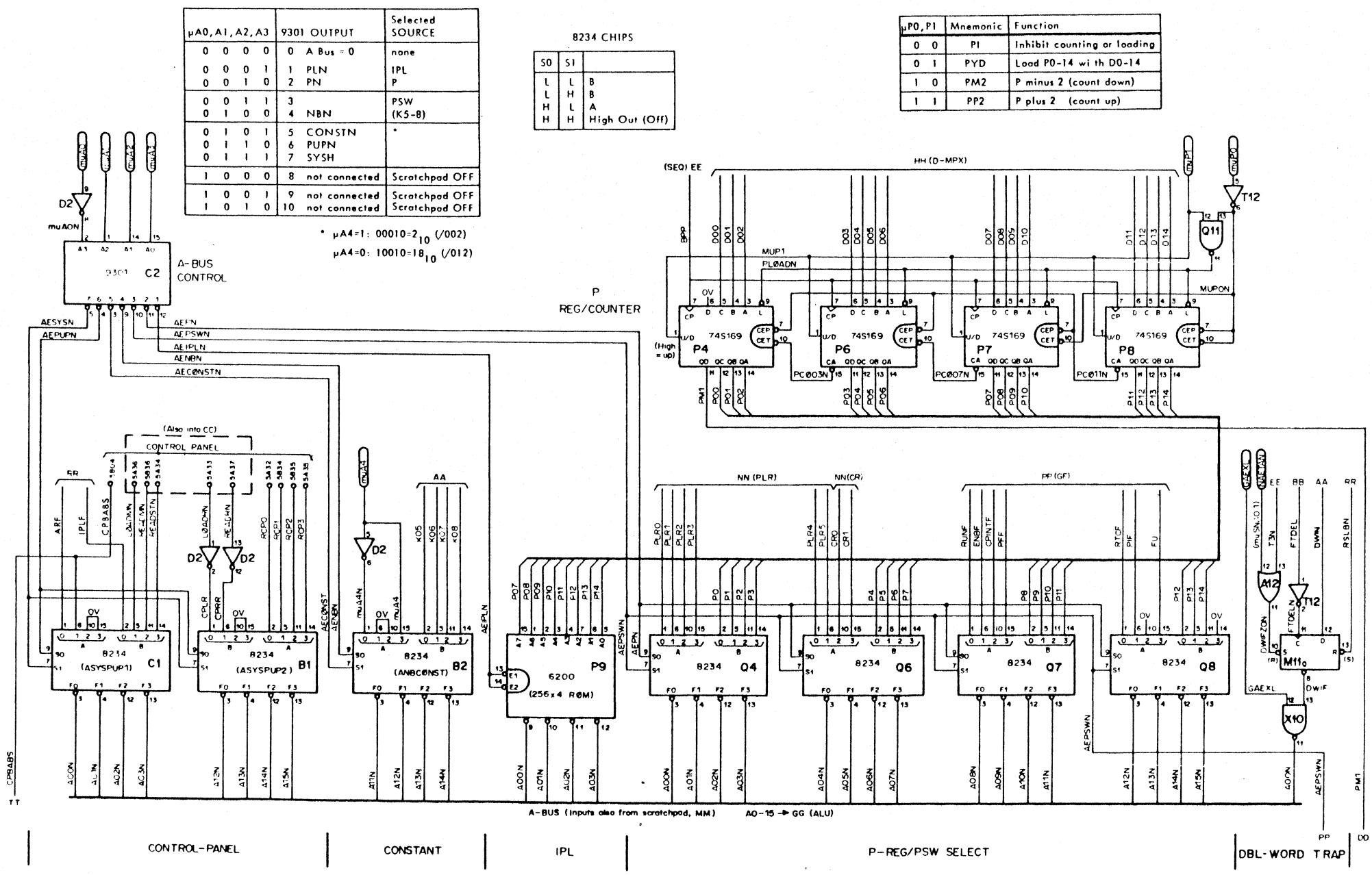
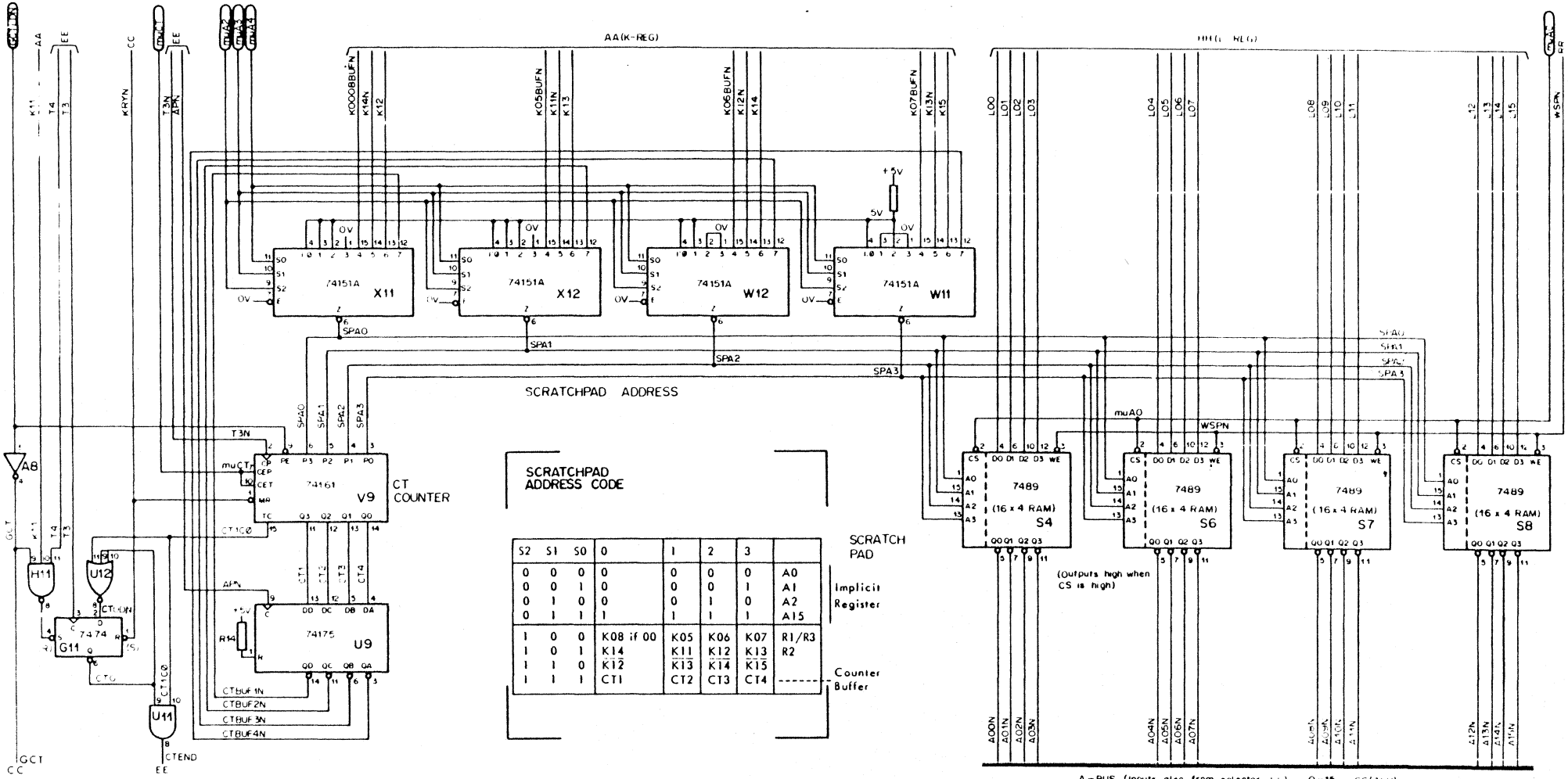


Figure 2-8LL A-Bus Selection, IPL, P-Register/Counter



S2	S1	S0	0	1	2	3	
0	0	0	0	0	0	0	A0
0	0	1	0	0	0	1	A1
0	1	0	0	0	1	0	A2
0	1	1	1	1	1	1	A15
1	0	0	K08 if 00	K05	K06	K07	R1/R3
1	0	1	K14	K11	K12	K13	R2
1	1	0	$\overline{K12}$	$\overline{K13}$	$\overline{K14}$	$\overline{K15}$	
1	1	1	CT1	CT2	CT3	CT4	

CT0D = CARRY+CT0:
CT0, 1, 2, 3, 4
0 1 1 1 0
0 1 1 1 1 (carry)
1 0 0 0 0
1 0 0 0 1

μCT (H-1)	GCTLDN (L-1)	Function
0	0	No change
0	1	Load CT1-4 from SPA0-3; CT0 from K11
1	0	Count CT at each T3N

Figure 2-8MM Scratchpad

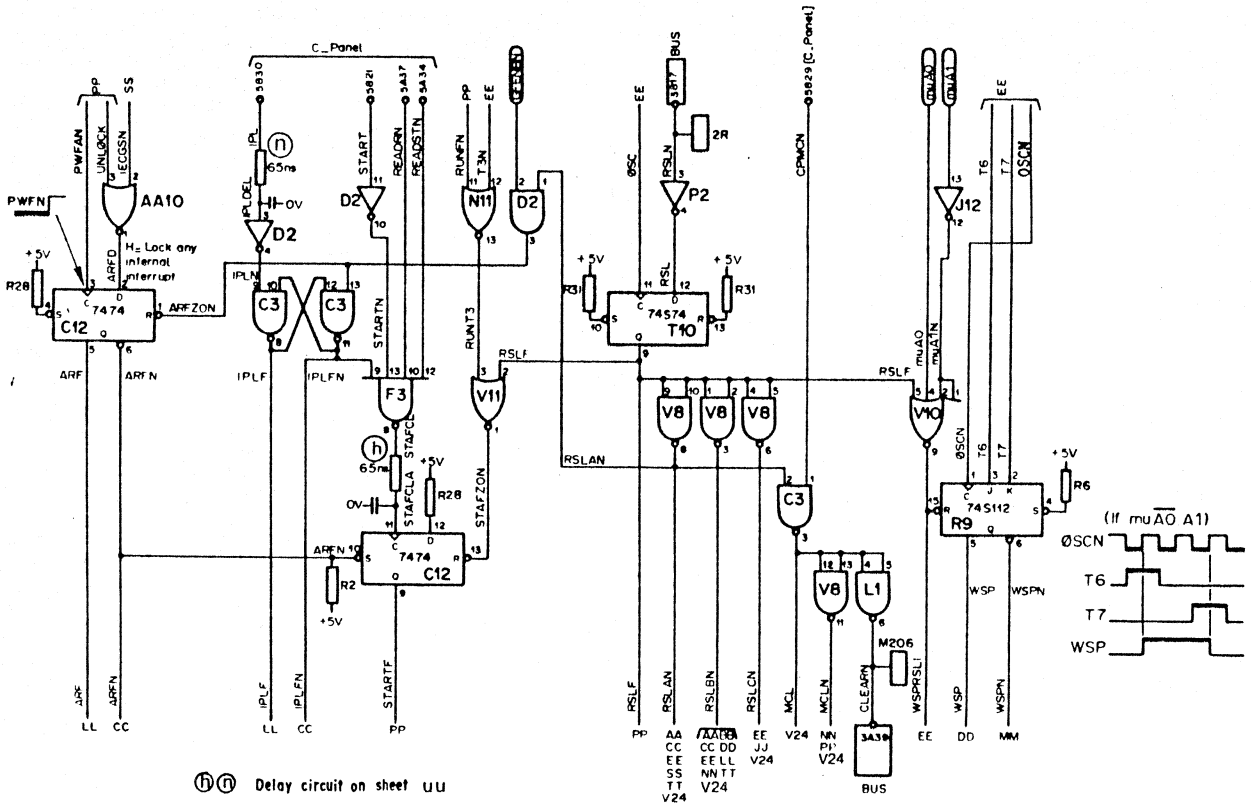
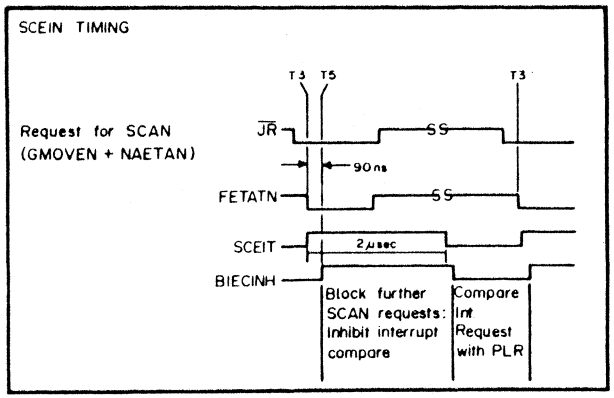


Figure 2-8RR Start, Reset



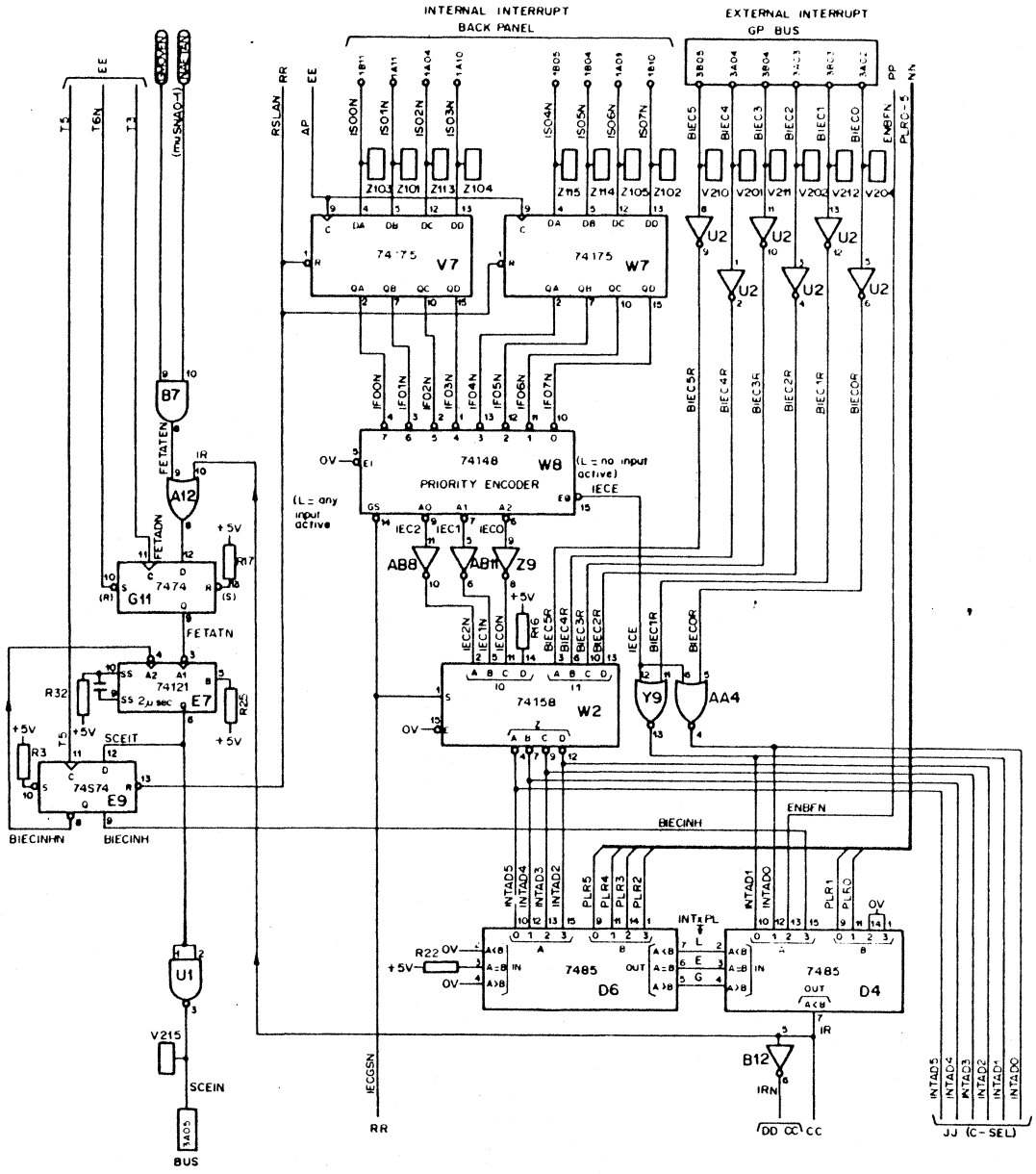


Figure 2-8SS Interrupt Logic

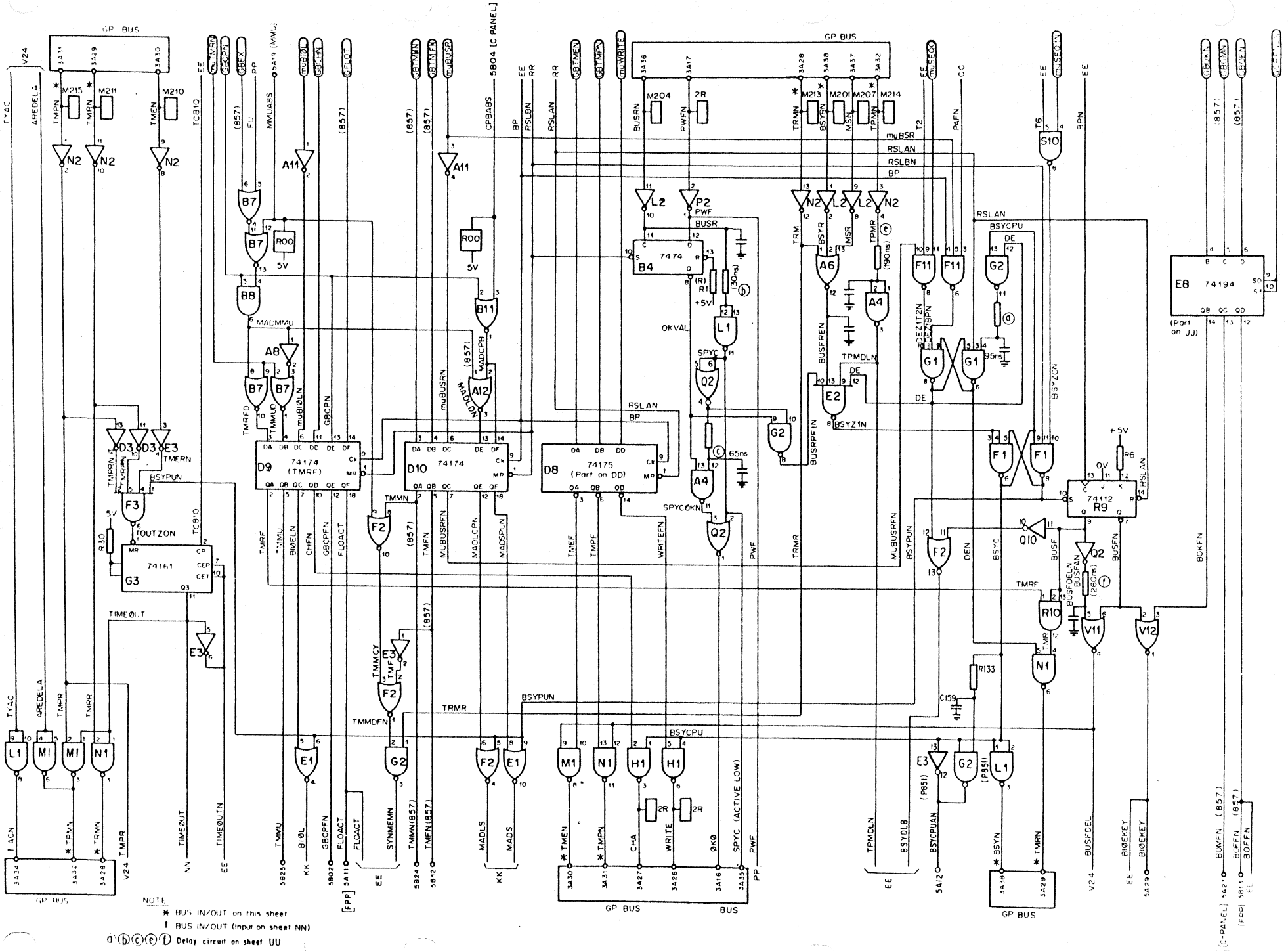
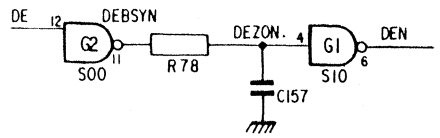
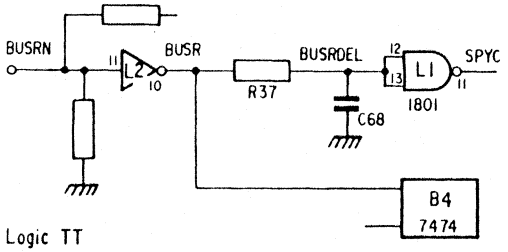
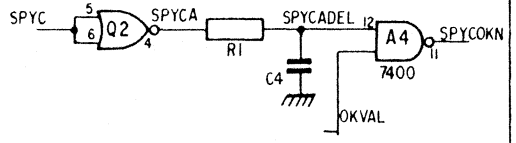
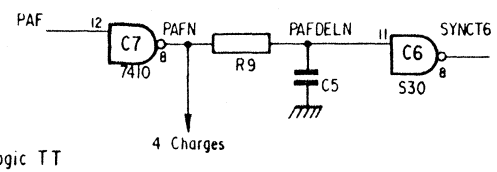
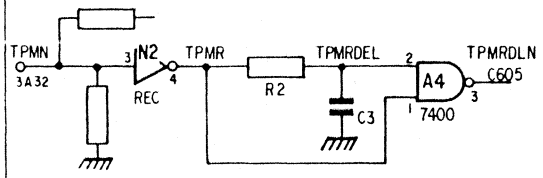


Figure 2-8TT Bus Controller

SIGNAL	LOGIC SHCEMATIC	DELAY nS nominal	DELAY nS measured	COMPONENTS
ⓐ DEZO	 Logic TT	95nS	100nS	R = 148Ω 1% 1/8W C = 510 pF ±1% 250V 2222 426 45101 micropoco
ⓑ SPYC	 Logic TT	30nS	40nS	R = 100Ω 1% 1/8W C = 200pF ±1% 500V 2222 427 42001 micropoco
ⓒ SPYCOK	 Logic TT	65nS	70nS	R = 110Ω 1% 1/8W C = 430pF ±1% 250V 2222 426 44301 micropoco
ⓓ PAF	 Logic TT	12 onS	12 onS	R = 148Ω 1% 1/8W C = 620pF 1% 250V 2222 426 46201 micropoco
ⓔ TPMRDEL	 Logic TT	190 nS	200nS 190 nS	R = 110Ω 1% 1/8W C = 1,8nF ±1% 2222 424 41802 micropoco

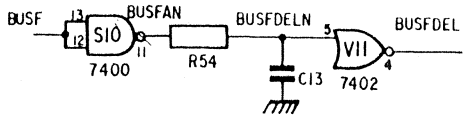
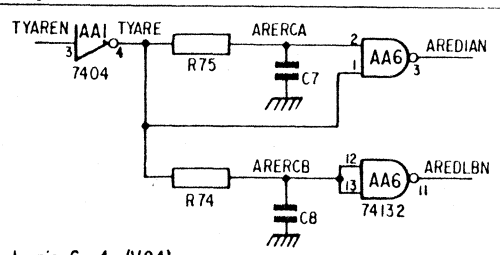
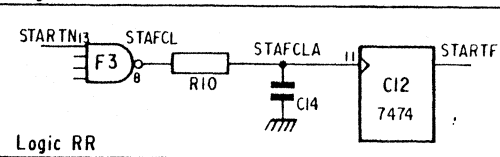
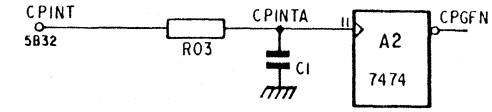
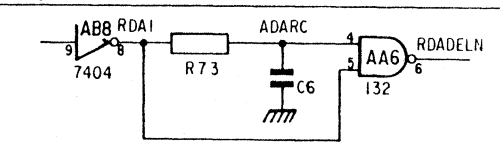
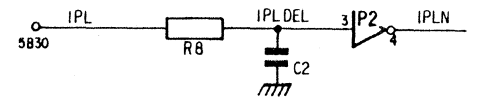
SIGNAL	LOGIC SCHEMATIC	DELAY nS nominal	DELAY nS measured	COMPONENTS
ⓕ BUSFDEL	 Logic TT	260nS	280nS	R = 100Ω 1% 1/8W C = 2nF 1% 2222 424 42002 micropoco
ⓖ DIALB	 Logic 6-4 (V24)	200 nS 60nS	240nS 85nS	R = 100Ω 1% 1/8W C = 1,3 nF 1% 63V 2222 424 41302 micropoco R = 100Ω 1% 1/8W C = 390pF 1% 250V 2222 426 43901 micropoco
ⓗ STAFCLA	 Logic RR	65nS	75 nS	R = 110Ω 1% 1/8W C = 620pF 1% 250V 2222 426 46201 micropoco
ⓚ CPGF	 Logic PP	65	75nS	R = 110Ω 1% 1/8W C = 620pF 1% 250V 2222 426 46201
ⓜ CHIPA	 Logic 6-4 (V24)	200nS	240nS	R = 110Ω 1% 1/8W C = 1,3nF 1% 63V 2222 424 41302 micropoco
ⓝ IPLDEL	 Logic RR	65nS		R = 110Ω 1% 1/8W C = 430pF 1% 25W

Figure 2-8UU Logic Delay Circuit Details