APPENDIX B

I/O PROCESSOR

SERVICE MANUAL

Effective Pages February 1977

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APPENDIX B

I/O PROCESSOR

B.1 GENERAL

The Input/Output Processor (IOP channel (Figure B-1) manages data transfers directly between memory and up to eight multiplexed control-unit/device channels. The IOP contains a pair of address/length control-word registers for each of its eight channels. At the beginning of a transfer for one device, the CPU program uses two WER instructions to load this register pair with the starting address and the block length (Figure B-2). The IOP logic then provides all GP Bus timing signals to control the data transfers directly between the memory and the CU.

B.2 For input or output data transfers, a CU signals that it is ready with a Break Request (BR) to the IOP. The IOP makes a Bus Request to obtain control of the GP Bus. The IOP then sends a simulated INR or OTR command to the CU to initiate one word transfer. The INR/OTR command is simulated in that it is generated by the IOP and is not a CPU programmed instruction. The IOP logic updates its control-word register for each data word. When the block length is counted down to One, the IOP sends End of Record (EOR) to the CU along with the last simulated INR/OTR data transfer. The data block transfer is ended with an SST command and status transfer between the CU and CPU.

B.3 The IOP is provided in two versions:

- version with card marked MX is for P852 only.
- version with card marked IOP is for P852/856/857.

The function and the logic is identical for both versions. The two cards differ in layout and in the location of components. Two sets of logic diagrams are thus provided to show the component locations for each version.

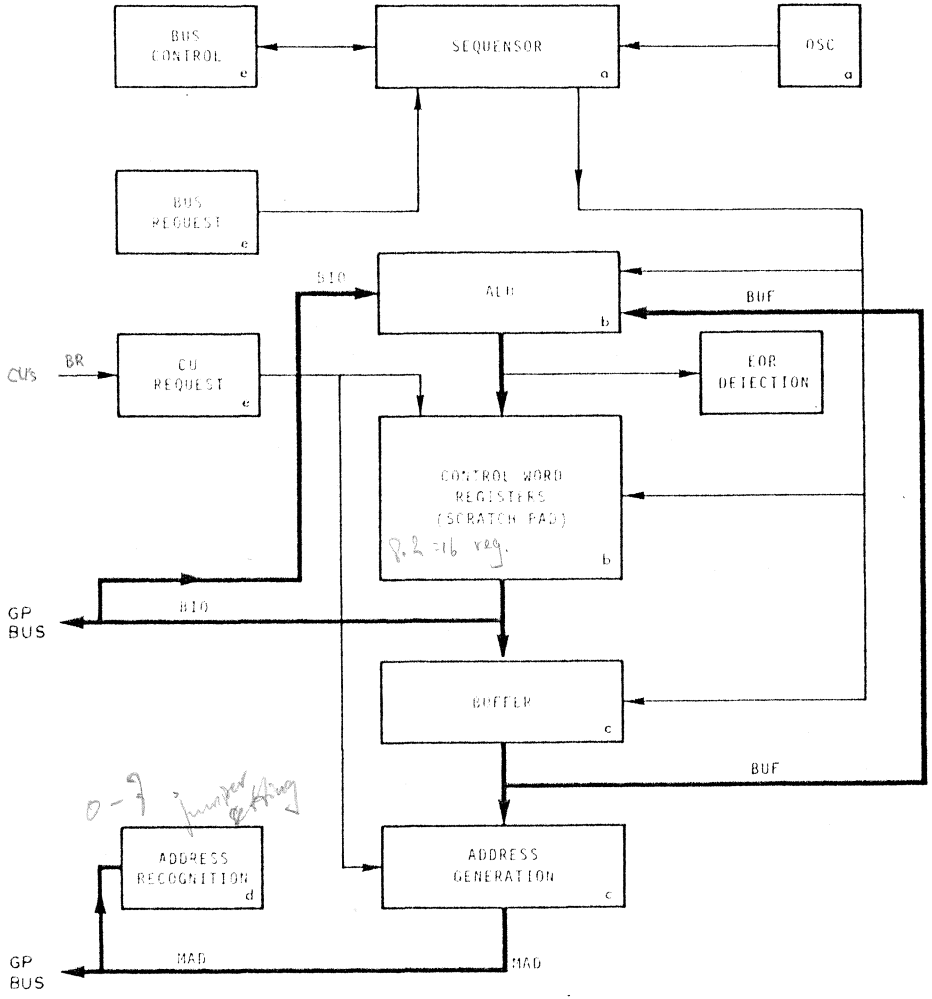


Figure B-1 I/O Processor Block Diagram

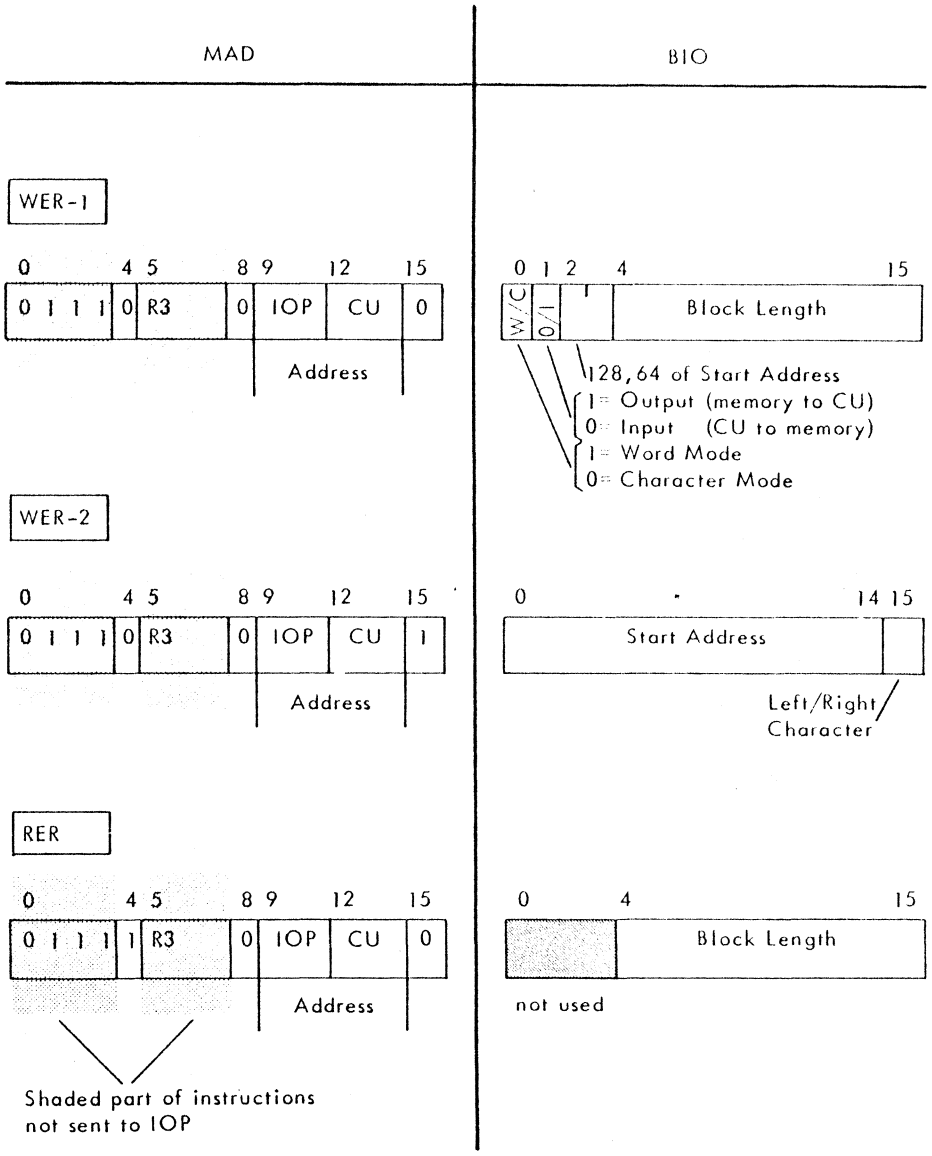


Figure B-2 Bus Content During CPU Mode (WER/RER)

B.4 CU/Device Priority

Priority of the eight CU/Device channels is established by the connection of the Break Request lines. Refer to paragraph B.18.

B.5 WER Instruction

Two Write External Register (WER) instructions (Figure B-2) are used to load the two control words for a device into a pair of IOP registers. Bits 04, 08-15 of the instructions are sent to the IOP on the MAD lines; bit-15 of each instruction specifies WER-1 or WER-2. The R3 field of each instruction specifies a CPU accumulator (A1-A7) that contains the block-length or start-address control word which is sent to the IOP on the BIO lines.

B.6 RER Instruction

A single Read External Register (RER) instruction (Figure B-2) is used when the CPU wants to test the remaining block length of an incomplete data-transfer operation. Bits 04, 08-15 of the instruction are sent to the IOP on the MAD lines; bit 15 = 0 accesses the control-word-1 (block length) register in the IOP. The R3 field of the instruction specifies the CPU accumulator (A1-A7) where the control-word information placed on the BIO lines is to be loaded (bits 4-15).

B.7 Logic Description and Diagrams

The IOP logic is described in the sequence of its operation, in the section IOP Operating Modes. Operation of some of the more complex logic units (sequensor, ALU, scratchpad) is given also in the section Functional Units. Logic diagrams (Figure B-9, sheets a-e) are provided at the end of the logic description. These diagrams are referenced on the block diagram and in the text by the sheet number, for example: "logic c" refers to Figure B-9, sheet c.

B.8 IOP OPERATING MODES

The IOP operates in three modes:

- Sampling Mode -- The IOP sequensor logic monitors the IOP status and tests for CU Break Requests or CPU commands.
- CPU Mode -- Set upon receipt of a CPU command (WER or RER instruction). Control-word register information is transferred between the CPU and IOP, with the CPU as master to control the GP BUS.
- Exchange Mode -- Set upon receipt of a Break Request from a CU (with Bus Obtained. One data word is transferred directly between the CU and memory, with the IOP as master to control the GP Bus.

B.9 Sampling Mode

The IOP waits in Sampling Mode whenever there is no instruction or data-exchange operation being performed. The sequensor logic is set to the Scan cycle (Figure B-3); timing signals AP and T1 are repeated continuously. The AP signal is used to test every 200ns for instructions from the CPU and Break Requests from the Control Units. Detection of the address-recognized signal AK indicates a CPU command, and the IOP sets CPU mode with signal NCPU. Detection of a Break Request sets the IOP to exchange mode. The ENB flip-flop (set at the end of an Exchange operation) remains set during Sampling Mode (logic e) to enable a Bus request if a BR is detected.

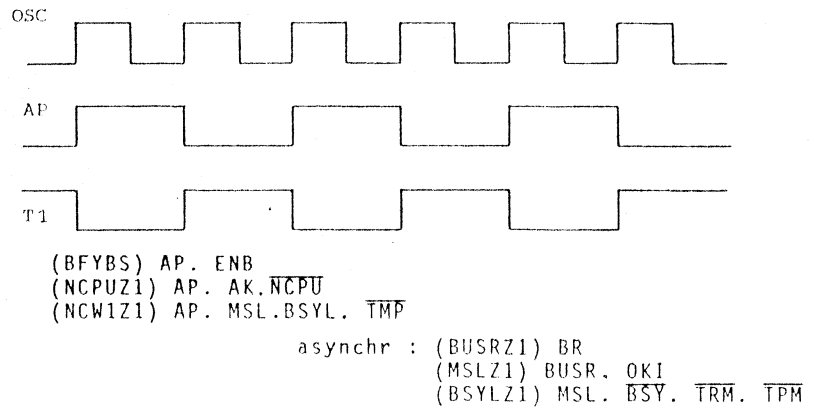


Figure B-3 Scan-Cycle Timing

B.10 CPU Mode

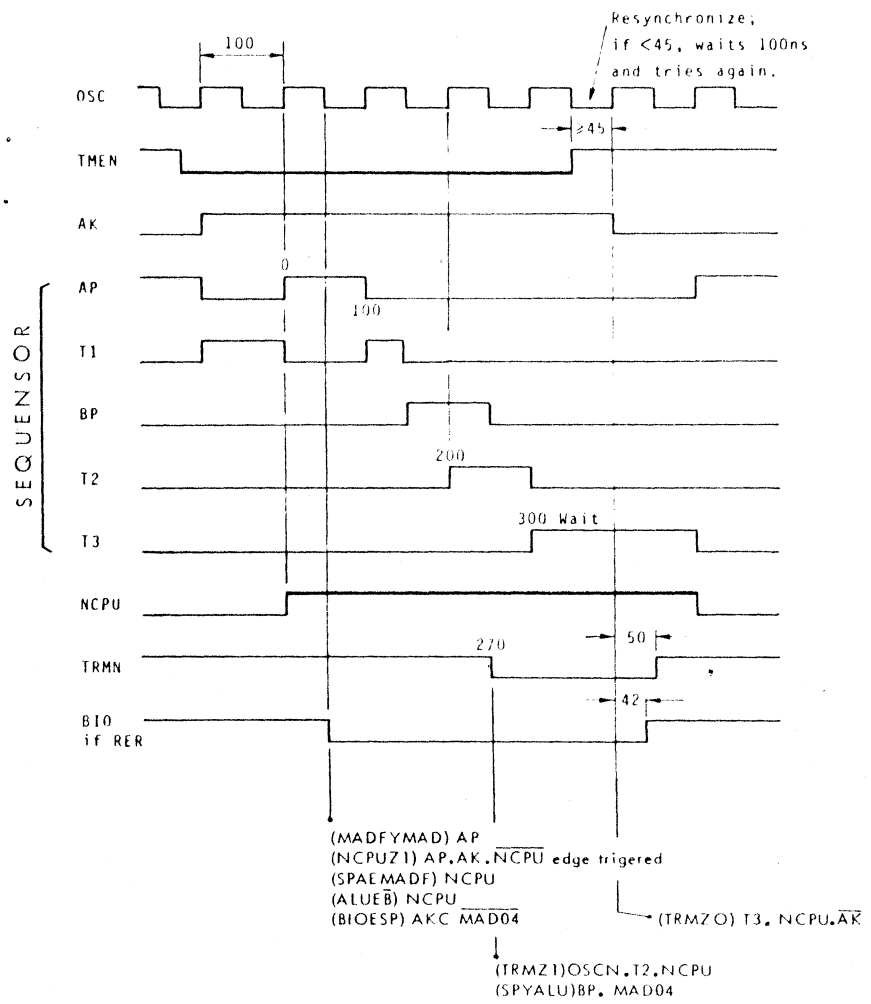
The CPU mode is used by the IOP logic to perform the WER or RER instruction from the CPU. The CPU sends part of the instruction word (including the IOP address) to the IOP (Figure B-2), with timing signal TMEN. The CPU mode is set when the IOP, in Sampling Mode, detects its address-recognized signal AK.

B.11 Addressing. A WER/RER instruction can address up to 256 external registers with MAD 08-15 (Figure B-2). With bit 08 = 0 for IOP operations, up to 128 external registers can be specified, with 16 registers for each IOP. Bits 12-14 address the register pair for a specific CU/Device channel; bit 15 indicates register-1 or register-2 for the selected device, corresponding to the first or second control word for the channel.

B.12 CPU-Cycle Operation. CPU-cycle timing is shown in Figure B-4. The IOP compares the address on MAD08-11 with its own address code set by U-links (logic d). An address compare (AKC) is set into the AKCF flip-flop on the rising edge of OSC. The AK signal sets flip-flop NCPU on the rising edge of AP (logic d), if NCPU is not already set. This constraint avoids repeating a CPU cycle. NCPU and AK are used by the Sequensor CPU-cycle: AP-T1-BP-T2-T3.

B.13 For an RER instruction (MAD04 = 1), AK activates BIOVALN (logic d) to gate the control-word register contents onto the BIO lines to the CPU (Scratchpad, logic b). The active RCWN signal inhibits writing into the scratchpad.

B.14 For a WER instruction (MAD04 = 0), BIOVALN and RCWN are blocked (logic d) and WCWIN is conditioned. The Arithmetic unit (ALU, logic b) is set to logic operation $\overline{B}$ by the selection signals CW2, 1 = 1, 0. The control word on the BIO lines is thus connected through the ALU B-input to the scratchpad. The control word is clocked into the addressed scratchpad register by the BP pulse during the CPU-cycle timing.



Note : Times shown in ns

Figure B-4 CPU-Cycle Timing

B.15 The scratchpad-address multiplexer (SPA0-3N) is switched by NCPU so that the MAD lines 12-15 select the register address. In the middle of T2 time, TRMX is set and the timing-response signal TRMN is sent back to the CPU (logic e).

B.16 The IOP waits with sequensor-cycle T3 until TMEN from the CPU is terminated. AK is reset on the next OSC after TMEN drops. The loss of AK activates APJN (logic a) which resets TRMX, dropping TRMN, and enables AP to be set on the next OSC. The CPU Mode is finished when AP is set and the IOP is switched to the Sampling Mode.

B.17 Exchange Mode

The Exchange Mode is used by the IOP logic to perform a data transfer between a CU and memory. The exchange can be either input (CU to memory) or output (memory to CU). The IOP operates as System Master to obtain control of the GP Bus and control the operation. The operation is performed in two logic sequensor cycles: CW1 and CW2. The Exchange Mode is set when the IOP, in Sampling Mode, detects a Break Request (BR) from one of the CUs (Figure B-5).

B.18 Break Requests. The CU priority is established when the Break Request (BR) lines from the CUs are connected to the IOP, with BR00 the highest priority and BR07 the lowest. The BR lines are examined whenever Enable flip-flop ENB is set (logic e). ENB is reset at the start of an Exchange operation (T1 of CW1, Figure B-6) to prevent a higher-priority BR from altering the conditions after an operation has started. ENB is set near the end of the Exchange, and remains set during the Sampling Mode, to enable a BR to initiate a Bus-Request sequence.

B.19 A Bus Request is initiated if any BR is active when ENB is set. This may happen any time during Sampling Mode, or in the middle of the previous Exchange cycle CW2. Starting a new Bus Request before the previous Exchange has been completed enables data-exchange operations to be linked together to save time.

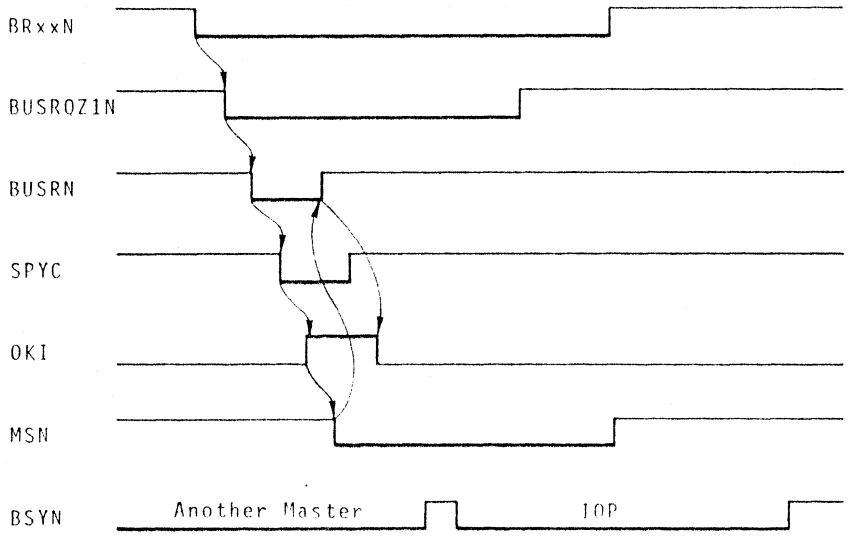


Figure B-5 Bus Request Sequence

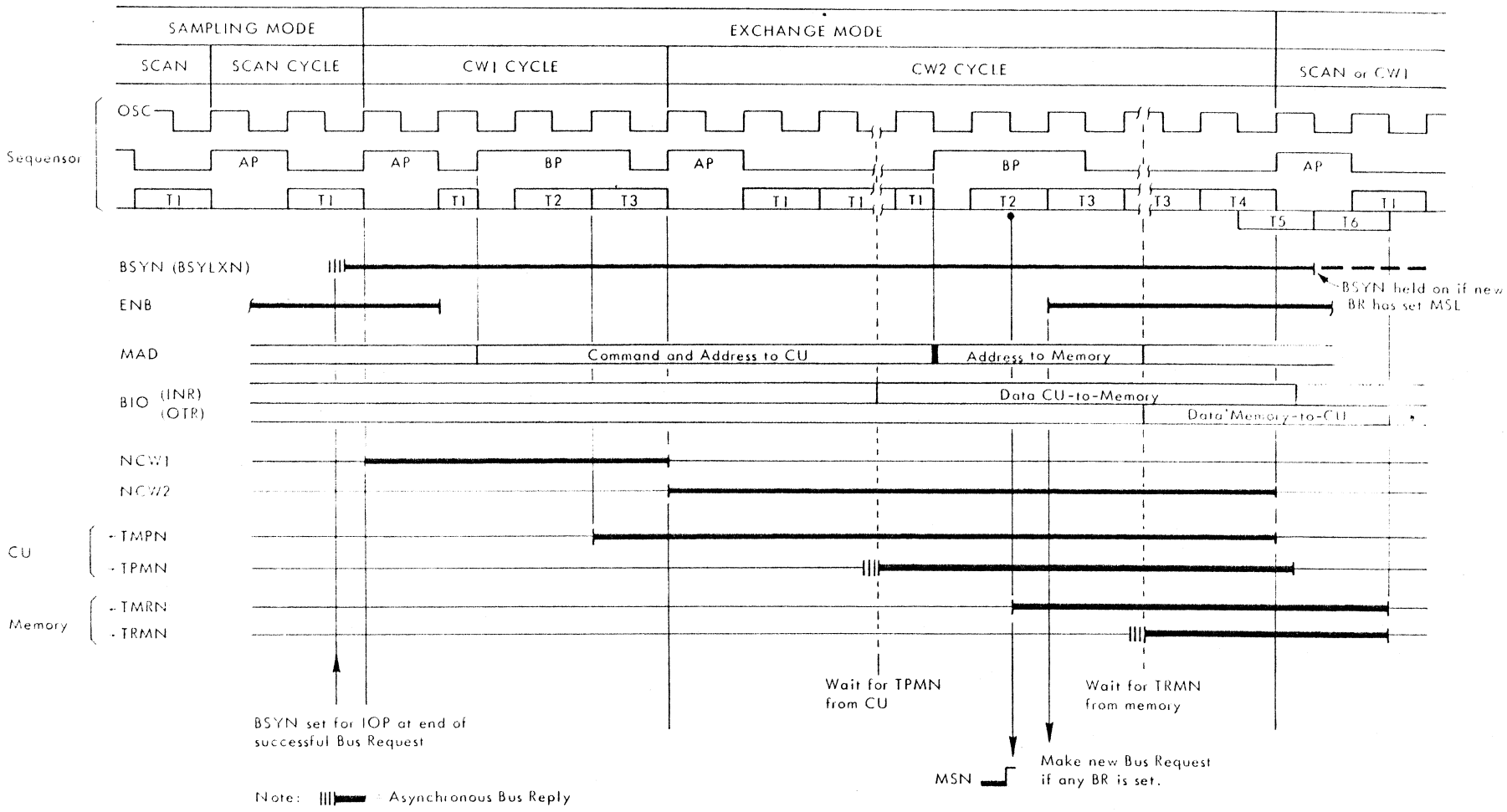


Figure B-6 Exchange-Cycle Timing (CW1/CW2)

B.20 With ENB set, any active BR signal is set into the FBR register (logic e) by the leading edge of AP, which occurs every 200ns during Sampling Mode, or at the end of Exchange cycle CW2. The priority encoder circuit (74148) indicates the code of the highest-priority BR stored in FBR. This code (BRENC0-2) is used to select the external-register (scratchpad) address.

B.21 Bus Request Logic. The Bus Control sequence, with the IOP as Master, is shown in Figure B-5. BUSRQZ1N from the detected BR is gated into the Bus-Request logic (logic e) as BUSRQ if no other operation is active (BUSRQN high). BUSRQ sends BUSRN to request the GP Bus.

B.22 The active-low SPYC response (scan priority chain) sets the OKA flip-flop. OK1 is received if no higher-priority unit takes control of the Bus. OK1 sets the MSL (master selected local) flip-flop, while OKAN blocks the sending of OKO to the next unit on the Bus. MSL sends the Master-Selected signal MSN onto the Bus, and terminates BUSRN. The CPU responds to the end of BUSRN by dropping SPYC and OK1.

B.23 The IOP may have to wait, with MSL set, until the Bus becomes free of any current operation (TRMN, TPMN, and BSYN all inactive). When the Bus is free, MSL sets BSYLX which puts BSYN onto the Bus to take Bus control for the IOP. The IOP switches to the CW1 cycle at the first AP after BSYLX is set.

B.24 Register Addressing. Two control-word registers must be accessed in the scratchpad during the Exchange Mode. The registers contain data transfer information (control and address) and must be updated during the operation. The scratchpad-address multiplexer (logic b) is switched by $\overline{\text{NCPU}}$ so that the BR priority encoder and NCW1 select the register address. The three most-significant bits (SPA1-3) are selected by BRENC2-0N; the least-significant bit (SPA0) is selected by NCW1 (1 for cycle CW1 and 0 for cycle CW2).

B.25 First Control Word. The first control-word sequence (Figure B-6) begins with the first AP pulse following the setting of BSYLX. The sequensor CW1 cycle is AP-T1-BP-T2-T3, with AP of the CW2 cycle following directly after T3. The NCW1 flip-flop (logic d) is set by the leading edge of AP after BSYLX is set.

B.26 With NCW1 set, the ALU mode selected is A minus 1 (for bits 04-15 only). The first control word is gated from the scratchpad into the buffer register (BUF, logic c) by the leading edge of BP. The BUF contents are immediately applied to the ALU where the block-length is decremented and bits 00-03 are transferred directly. If the block length is decremented to One by this operation, ENDN is active. At the end of BP, the updated control word is gated back into the scratchpad.

B.27 The Input/Output control bit (ALU01N) and the ENDN signal are set into a two-bit register (logic b) as BUFIN and BUFEOR. These two bits are written into the auxiliary scratchpad as SPINN and SPEORN, and are used to minimize delay in the generation of the MAD signals to the CU.

B.28 The IOP command to the CU is placed on the MAD lines (Figure B-7) via the MADSL multiplexer (logic c). The Input/Output control (SPIN) and EOR (SPEOR) bits are sent on MAD04 and 03 respectively. The IOP address (MXAD0-2) placed on MAD10-12 is taken directly from the IOP address U-links. The CU address from the priority encoder (BRENC0-2) is sent on MAD13-15.

B.29 The IOP generates Bus timing signal TMPN (logic e) at the end of time T2 (the first OSC after flip-flop TMPX is set). TMPN goes active 160ns after the MAD lines are set. The CU uses TMPN to validate the address and control information on the MAD lines. The CW1 cycle for the first control word is completed at the end of T3, before the CU has responded to TMPN.

B.30 Second Control Word. The second control-word sequence (Figure B-6) begins with the AP pulse immediately following T3 of CW1. The sequensor CW2 cycle is AP-T1* -BP-T2-T3* -T4-T5-T6, with a waiting loop before BP and before T4. Flip-flop NCW2 (logic d) is conditioned by the TMPN signal (TMPXA) and set on the leading edge of AP.

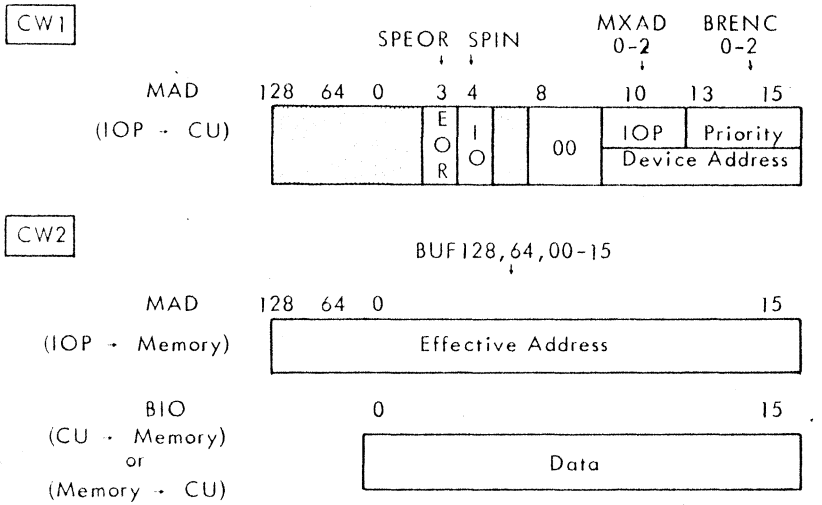


Figure B-7 Bus Content During Exchange Mode (CW1/CW2)

B.31 The second control word is available at the scratchpad output (logic b) as soon as NCW1 goes off. With the control flip-flops NCW1-NCW2 at 0-1, the ALU mode selected is A plus 1 for incrementing the effective character address. To realize A plus 2 for updating the effective word address, CW2WN forces a carry-in to bit 15, resulting in the least-significant bit set to 0 for the even-character word addressing.

B.32 The IOP waits for the CU response TPMN, with the sequensor blocked at T1 before the generation of BP. The CU receives TMPN and its address and command on the MAD lines (sent at the end of CW1), places data on the BIO lines (for an input transfer), drops its BR for that exchange, and sends TPMN back to the IOP. TPMN is clocked into TPMNRA (logic a) on the leading edge of OSC preceeding BP to ensure the guard time of BIO for input transfers.

B.33 Before the IOP starts the memory transfer, it ensures that any preceeding memory response signal TRMN is inactive (important in the case of linked exchanges). The BP pulse gates the 18-bit effective address (control word 2) from the scratchpad into the buffer (logic c). This memory address is switched via the MADSL multiplexer onto the MAD lines. The selection signal MADSEL is set at BP of CW2. At the same time, the read/write and word/character control signals are sent to the memory via Bus signals WRITE and CHA. These two control bits were read from the first control word and stared as BUFIN (logic b) and BUFCH (logic c) during CW1.

B.34 The IOP sets TMRX (logic e) in the middle of time T2 to send TMRN to the memory. The memory uses TMRN to validate the address on MAD (from the IOP) and the data on BIO (from the CU, if input transfer). The IOP must now wait for memory response TRMN.

B.35 The Bus control flip-flops OKA and MSL (logic e) are reset as a result of TMRN dropping MSN and freeing the Bus for a new selection. The reset occurs when TMRX sets the MSLRF flip-flop, and generates MSLRN. The reset MSLN flip-flop in turn resets MSLRF. BSYN is held active until time T6 so that the IOP maintains Bus control until its operation is complete. Enable flip-flop ENB (logic e) is set on the first OSC after T2 to permit acceptance of a new BR from any of the CUs.

B.36 If any BR is active when ENB is set, a new Bus Request sequence is initiated (paragraph B-20). If OKI is received without being blocked by another unit on the Bus, another IOP Exchange cycle (CW1-CW2) is linked to the end of this exchange. MSL is again set by OKI and holds BYSN on at time T6 instead of allowing it to be reset as in a normal ending.

B.37 The IOP waits for the memory response TRMN, with the sequensor blocked at T3 before the generation of T4. The TMPN signal to the CU remains active during the memory-transfer operation to enable the BIO-line data at the CU while TMRN enables BIO at the memory.

B.38 The TRMN response from memory is set into flip-flop TRMNRA (logic a) on any leading or trailing edge of OSC. Time T4 is then set on the next leading edge of OSC to continue the CW2 cycle. At time T4, flip-flops TMPX and TMPENB (logic e) are reset and TMPN to the CU drops (providing suitable guard time for the CU to read data on the BIO lines). The CU drops TPMN after TMPN goes inactive.

B.39 For read operations (output, memory to CU): the memory validates the data on the BIO lines with TRMN, the IOP validates the BIO data at the CU with the trailing edge of TMPN. For write operations (input, CU to memory): the CU validates the BIO-line data with TPMN, the IOP validates the BIO data at the memory with the leading edge of TMRN.

B.40 FUNCTIONAL UNITS

A block diagram of the IOP is given in Figure B-1. The control words are loaded into the Control Word Registers (scratchpad), via the ALU, by WER instructions. The CPU reads a Control Word from the scratchpad by means of an RER instruction. During data-transfer operations (Exchange Mode), the Control Words are accessed and updated via the processing loop: scratchpad--buffer--ALU--scratchpad. The address-generation logic sends the CU address/command and then the memory address for each data transfer.

B.41 Sequensor

The sequensor (logic a) is driven from a constantly-running oscillator to provide the IOP timing signals AP, BP, T1, T2, T3, T4, T5, T6. The oscillator frequency at QUARTZ is 20 MHz and OSC is 10 MHz. Sequensor cycles for the different Operating Modes are:

Operating Mode	Seq. Cycle	
Sampling	Scan	AP-T1, repeated until CPU or Exchange Mode is set.
CPU	CPU	AP-T1-BP-T2-T3*, waiting at T3 until the first OSC after TMEN is received from CPU.
Exchange	CW1	AP-T1-BP-T2-T3, followed by the CW2 cycle.
Exchange	CW2	AP-T1*-BP-T2-T3*-T4-T5-T6, with waiting loop before BP and T4. AP of next cycle (Scan/CW1) follows T4, overlapping T5-T6.

Signals AP, T1-T4, T6 are clocked on the rising edge of OSC. Signals BP and T5 are clocked on the falling edge of OSC and thus shifted one-half OSC cycle from the other sequensor signals. All sequensor timing signals have a duration of one or more 100ns OSC cycles, as follows:

- AP, T2, T4, T5, T6 are always 100ns.
- BP is 100ns (CPU cycle) or 200ns (CW1/CW2 cycles).
- T1 or T3 may last for one or more multiples of 100ns during the waiting conditions for BP or T4 during the CW2 cycle.

B.42 The conditions for the Sequensor timing signals are:

- AP (first pulse of every cycle)

Condition	
Scan T1	Start of Scan or CW1 cycle, depending on conditions for BP.
CPU T3.AKN	Start of Scan cycle; Sequensor waits at T3 of CPU cycle until AKN indicates the end of the CPU command, to avoid branching back into a CPU cycle if TMEN is delayed.
CW1 T3	Start of CW2 cycle always follows T3 of CW1.
CW2 T4	Start of Scan or new CW1 cycle follows T4, although T5-T6 of CW2 are not complete.

- T1

AP	T1 follows AP for all cycles
$\overline{BP}$	Wait at T1 until BP is set (CW2 cycle)

- BP

Cycle	Selection S0 NCW1	Selection S1 NCPU		Set (BPJ)	Reset (BPK)	
CW2	0	0	10	TPMNRA	T3	Wait at T1 until TPMN received
CW1	1	0	11	1	T3	
CPU	1	1	12	1	T2	

BPJ enabled by BPJE2N: SCANN.T1.(CW2+TRMN.TMPENB)

- T2 follows BP (CPU, CW1, CW2 cycles)
- T3 follows T2 and stays on until AP (CPU, CW1 cycles) or T4 (CW2 cycle) is set.
- T4 follows T3 directly (CPU, CW1 cycles) or waits for receipt of TRMN (CW2 cycle).
- T5 (CW2 cycle) ends the command to the CU.
- T6 (CW2 cycle) ensures data guard time for ending the memory transfer.

B.43 Arithmetic Unit (ALU)

The ALU (logic b) is used to load control words from the CPU and to update the control words during Exchange Mode. The type 9341 or 74181 ALU circuits operate in one of three modes, controlled by flip-flops NCW1-NCW2, as follows:

Operating Mode	Control NCW1,2 = CW1N,2	Selection S3,2,1,0-CIN-CE	Operation
CPU	0 0 1 0	L H L H L H	$\bar{B}$
Exch-CW1	1 0 0 0	L L L L L L	A - 1*
Exch-CW2	0 1 1 1	H H H H H H	A + 1

* Decrement bits 04-15 only; carry-in to bit 03 blocked by $\overline{NCW2}$ so that bits 03-00 are transferred without change.

- CPU mode loads the WER control words via ALU operand B from the BIO lines to the scratchpad.
- Exchange-Mode/CW1-cycle decrements the block-length control word in the processing loop, via ALU operand A.
- Exchange-Mode/CW2-cycle increments the effective-address control word in the processing loop, via ALU operand A.

B.44 Scratchpad

The 16-word scratchpad (logic b) stores the two control-words for each of the eight Control Units (Figure B-8).

B.45 Scratchpad Addressing. A type 74157 multiplexer circuit provides the scratchpad-addressing signals SPA0-3N, as follows:

Operating Mode	S-Input	Address Source for SPA0-3N
CPU	NCPU	MAD15-12RF from CPU (MAD lines); active low.
Exch-CW1	$\overline{NCPU}$	NCW1, BRENC2-0N; control-word-1 specified by the CU priority-level code.
Exch-CW2	$\overline{NCPU}$	$\overline{NCW1}$, BRENC2-0N; control-word-2 specified by the CU priority-level code.

B.45 128-64, EOR Bits. A type 74157 selector (SPIN) is used to transfer some bits from one control word to the other. The SPIN selector is controlled by signal SPA0N, as follows:

Cycle	Generation of SPA0N
CPU	MAD15 = 0, MAD15RF-high, SPA0N-high: first control word.
CPU	MAD15 = 1, MAD15RF-low, SPA0N-low: second control word.
CW1	NCW1-high, SPA0N-high: first control word.
CW2	NCW1-low, SPA0N-low: second control word.

SPIN Selection	Source IC	IB	IA
SPA0N-high	ENDN	ALU03N	ALU02N
SPA0N-low	ALU02N	ALU64N	ALU128N
Output:	SPIN02	SPIN64	SPIN128

- During the first WER instruction (SPA0N-high), address bits 128-64 are loaded via SPIN into scratchpad bits 128-64 for the second control word.
- During Exchange-Mode/CW1-cycle (SPA0N-high), the decremented block length is tested for a count of ONE, and the resulting ENDN bit is loaded via SPIN into scratchpad bit 02.

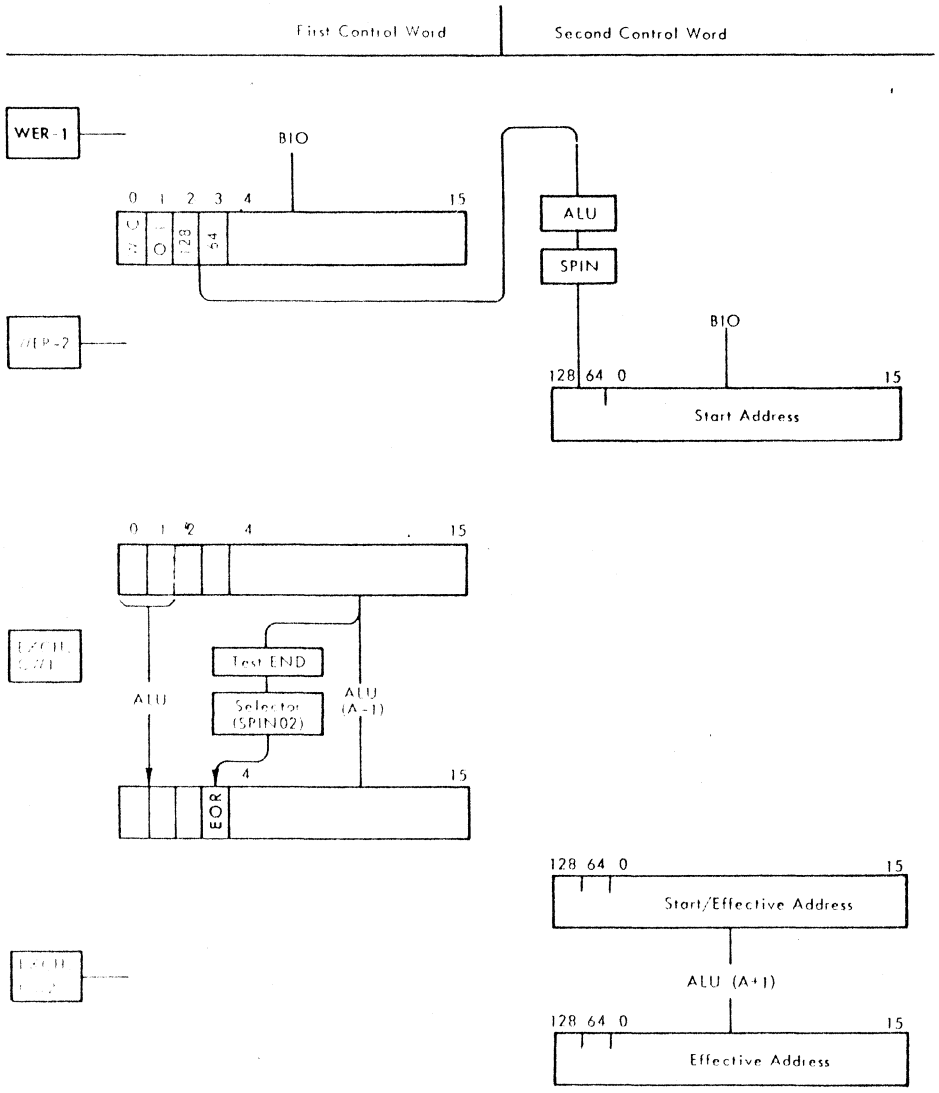


Figure B-8 Scratchpad Contents (IOP)

- During operations with the second control word (SPA0N-low), the effective address is loaded from BIO (via ALU $\bar{B}$) or incremented through the processing loop (via ALU A + 1).

B.47 In/Out, EOR bits. The Input/Output and End-of-Record (EOR) control bits are sent to the CU on the MAD lines during Exchange Mode, cycle CW1 (Figure B-7). These two bits are obtained via the ALU during the processing loop of the CW1 cycle: the In/Out bit from ALU01N; the EOR bit from testing block-length bits 04-15 for One (ENDN). ALU01N and ENDN are gated via the type 7475 circuit (as BUFIN and BUFEOR) and loaded into auxiliary scratchpad as SPINN and SPEORN. These two command bits are gated onto MAD04 and 03 along with the control-unit address code during the CW1 cycle (which is held until the TPMN response during the CW2 cycle).

B.48 Other Logic Units

The remaining logic units are described with the IOP Operating Modes. The following list is a guide to the uses of the different logic units.

Logic		Text Paragraph	
Address Recognition	d	CPU-Cycle	B.12
CU Request logic	e	Exch/Break Requests	B.18
Bus Request logic	e	Exch/Bus Request Exch/2nd CW	B.21 B.35
Execution Cycle logic	d	Exch/1st CW Exch/2nd CW	B.25 B.30
Bus Control logic	e	Exch/1st CW Exch/2nd CW	B.29 B.34
Buffer	c	Exch/2nd CW	B.32

B.49 PHYSICAL

The Units are contained on printed-circuit cards (Figure B-10) of the standard P852/856/857 system size. The parts lists are provided in Table B-1. The IOP interfaces the other system elements (CPU, control units, and memory) via the GP Bus, via connector-3.

B.50 U-Links

Adjustable U-links are provided for decoding the IOP address (logic d). The locations of the U-links are shown on Figure B-10.

B.51 Break-Request (BR) Signals

The BR signal connections are shown in Figure B-11. The internal BR signals, from CUs in the same chassis with the IOP, are attached to connector-4B. The external BR signals, from CUs in the extension chassis, are attached to connector 5, and are strapped from connector-4A to 4-B. Priority of the control units is determined by the order of the connections to connector-4B.

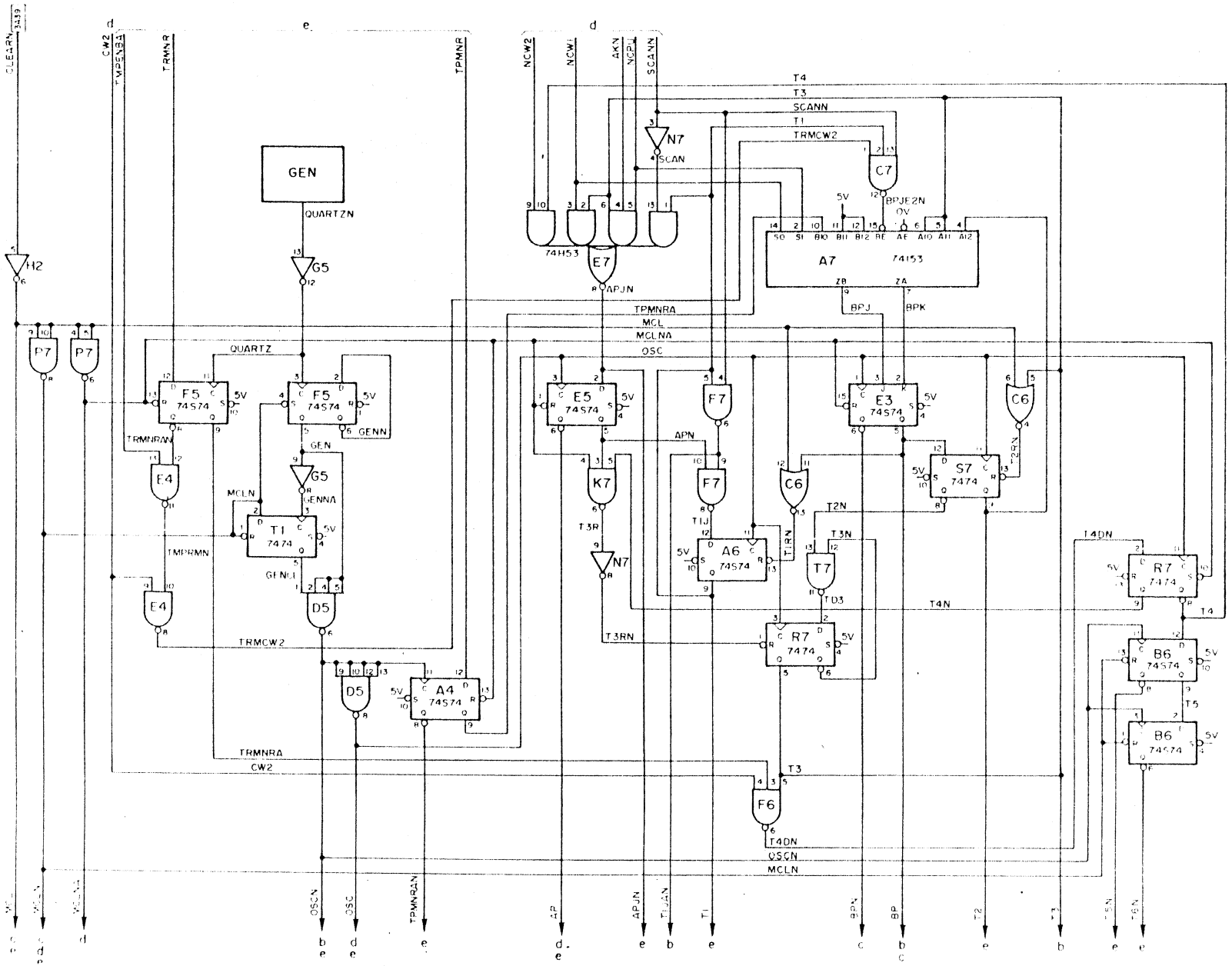


Figure B-9a Clock/Sequencer (MX)

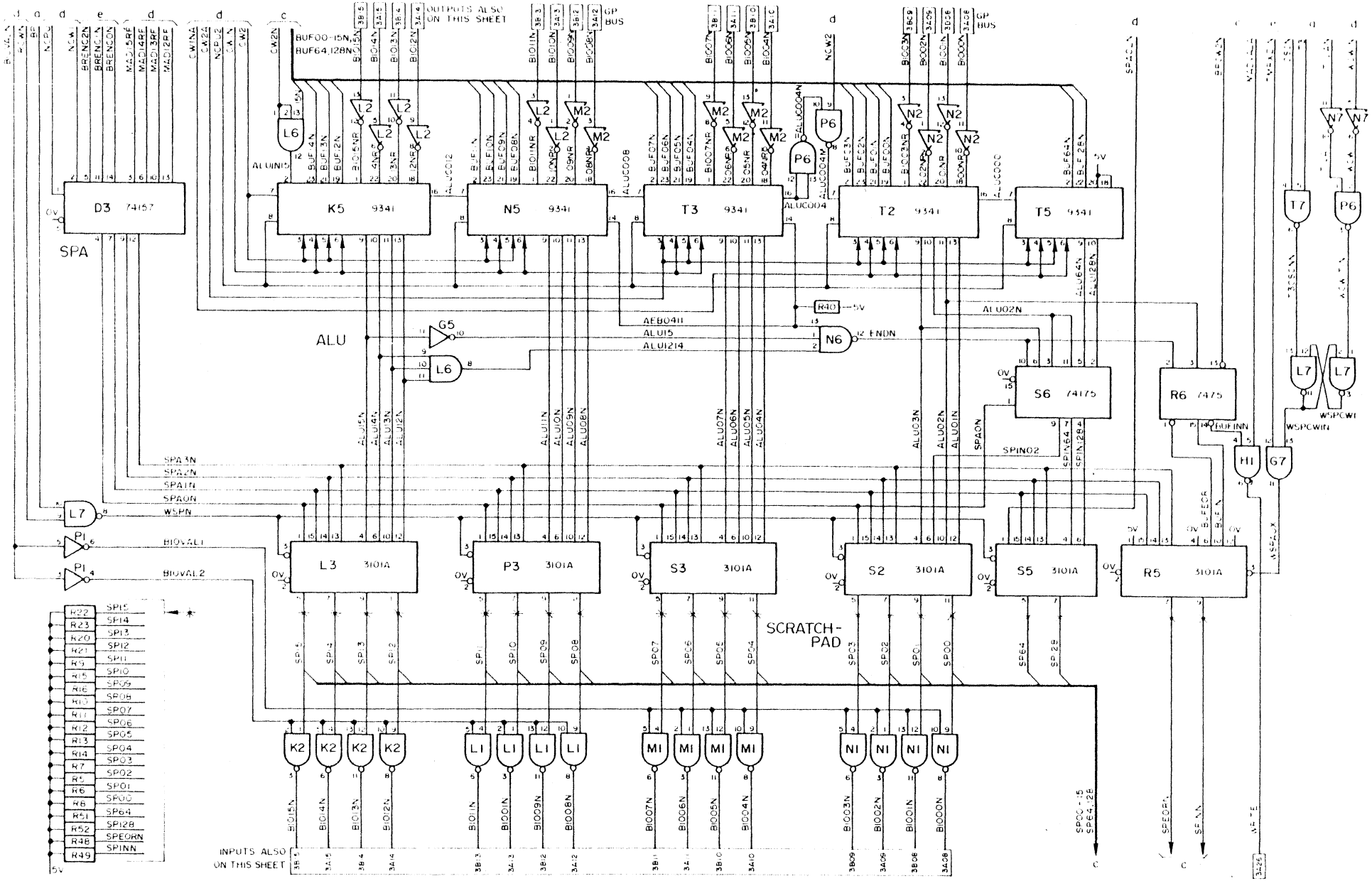


Figure B-9b ALU, Scratchpad (MX)

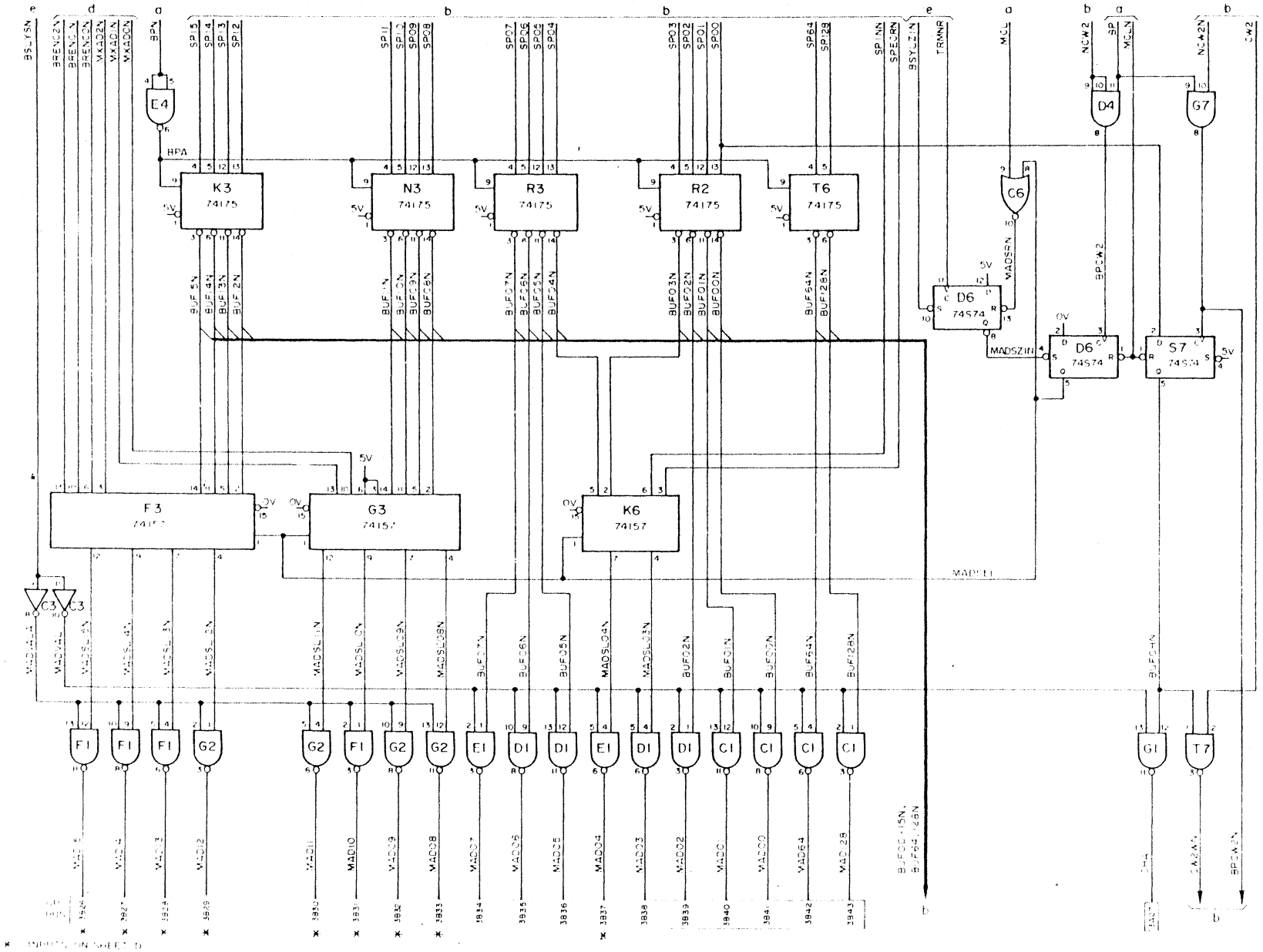


Figure B-2 ... Address Generation (M...

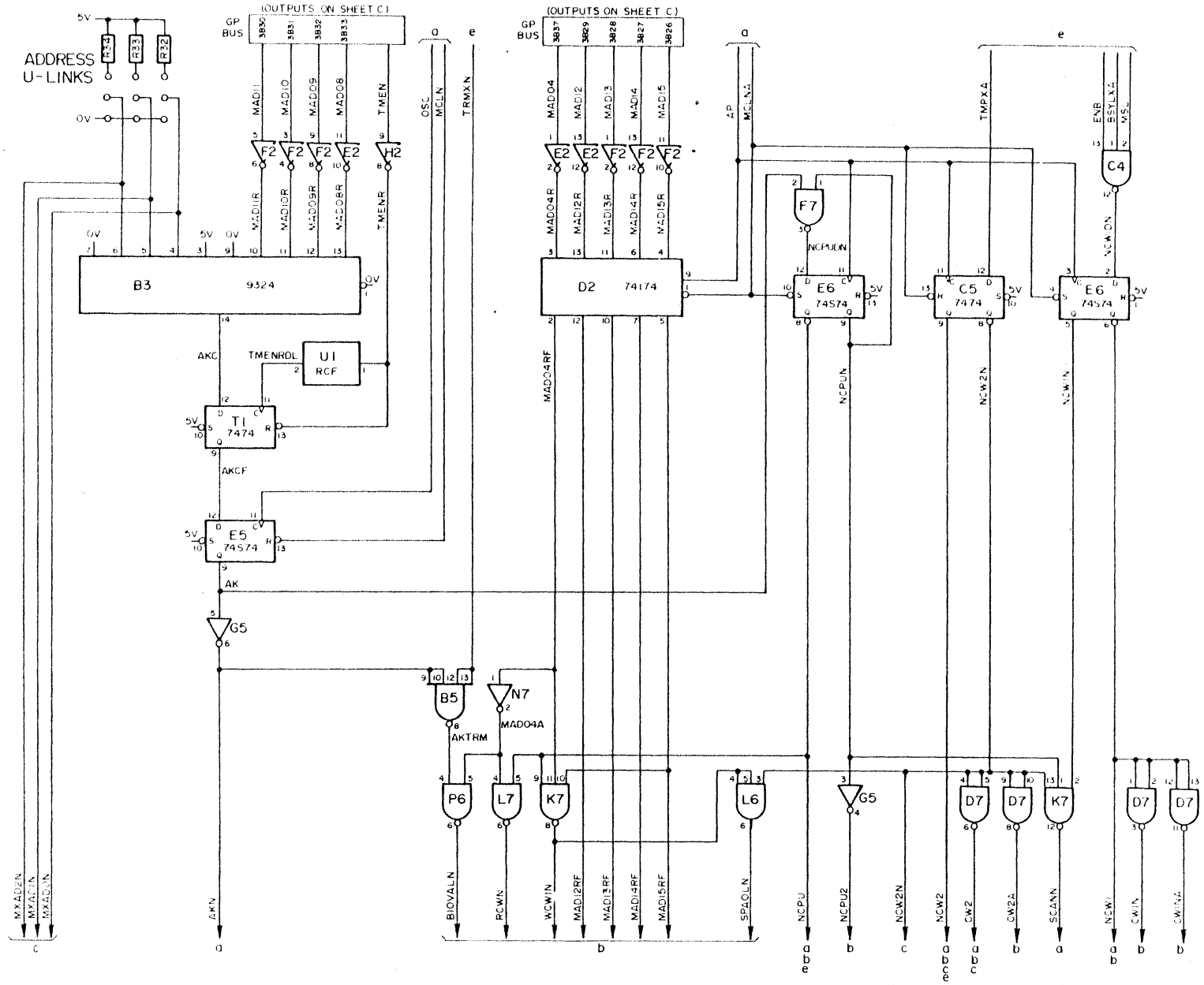


Figure B-9d Address Recognition, Execution Cycle (MX)

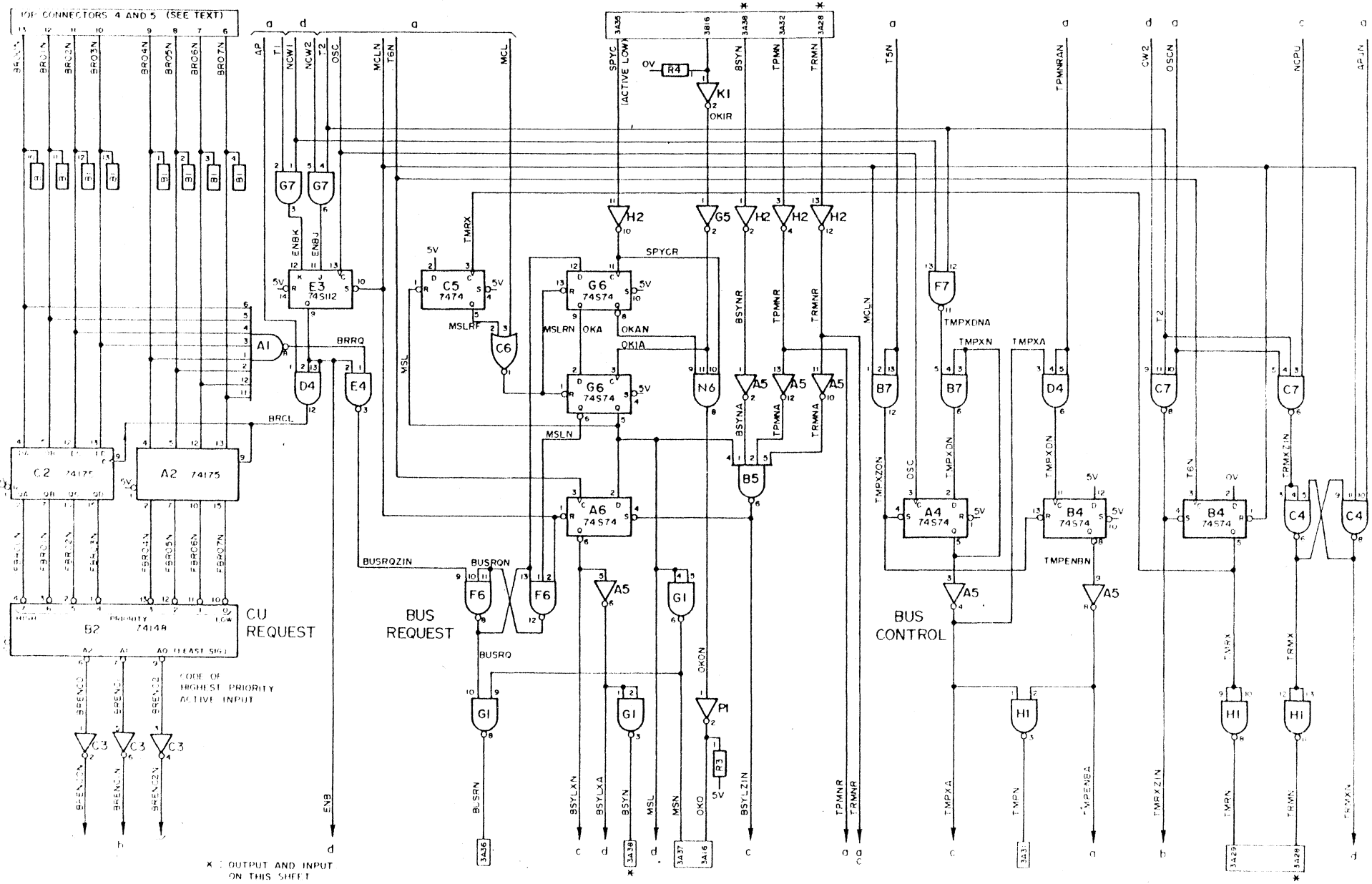


Figure B-2e. Input Output Control (3A)

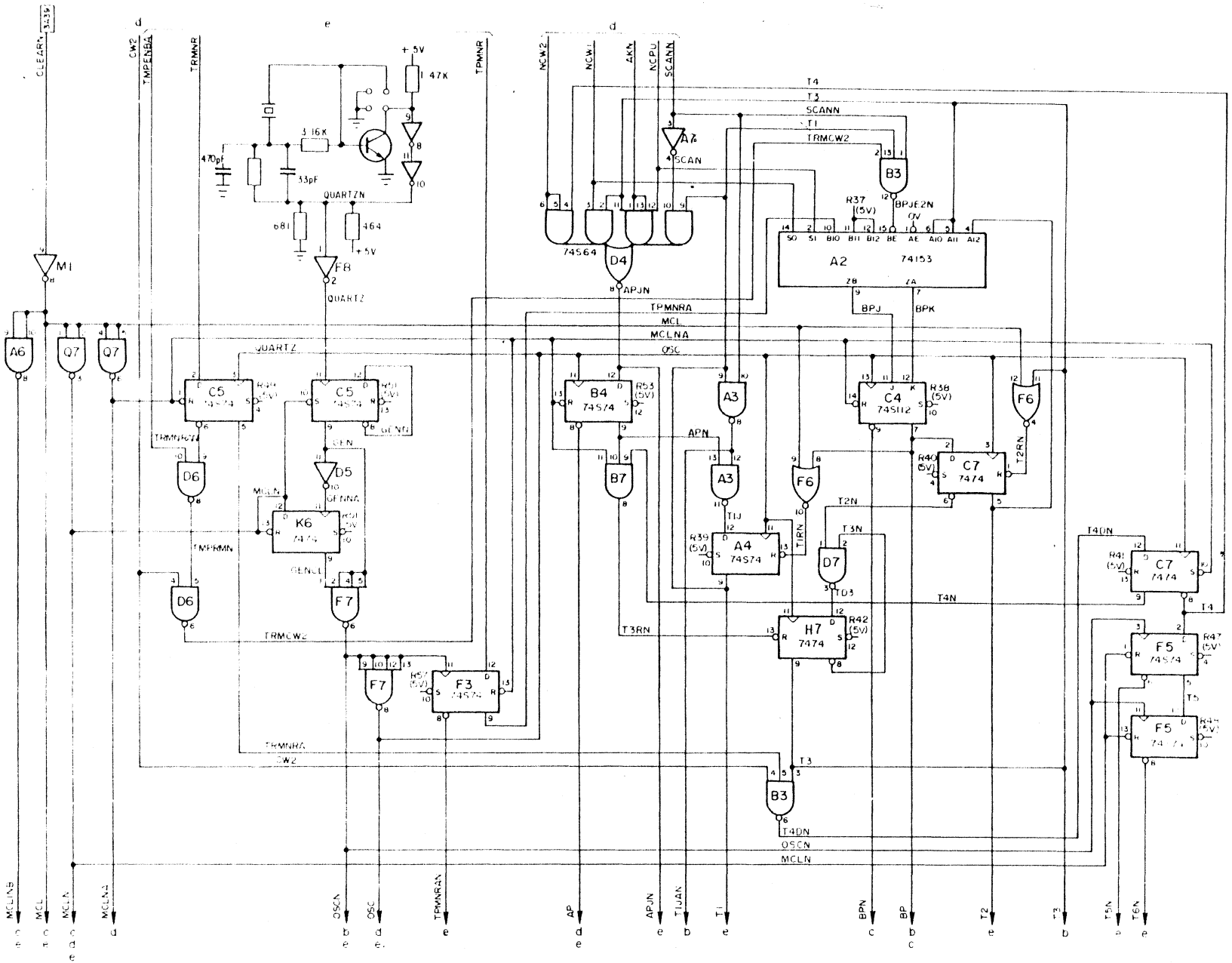


Figure B-9a Clock/Sequensor (IOP)

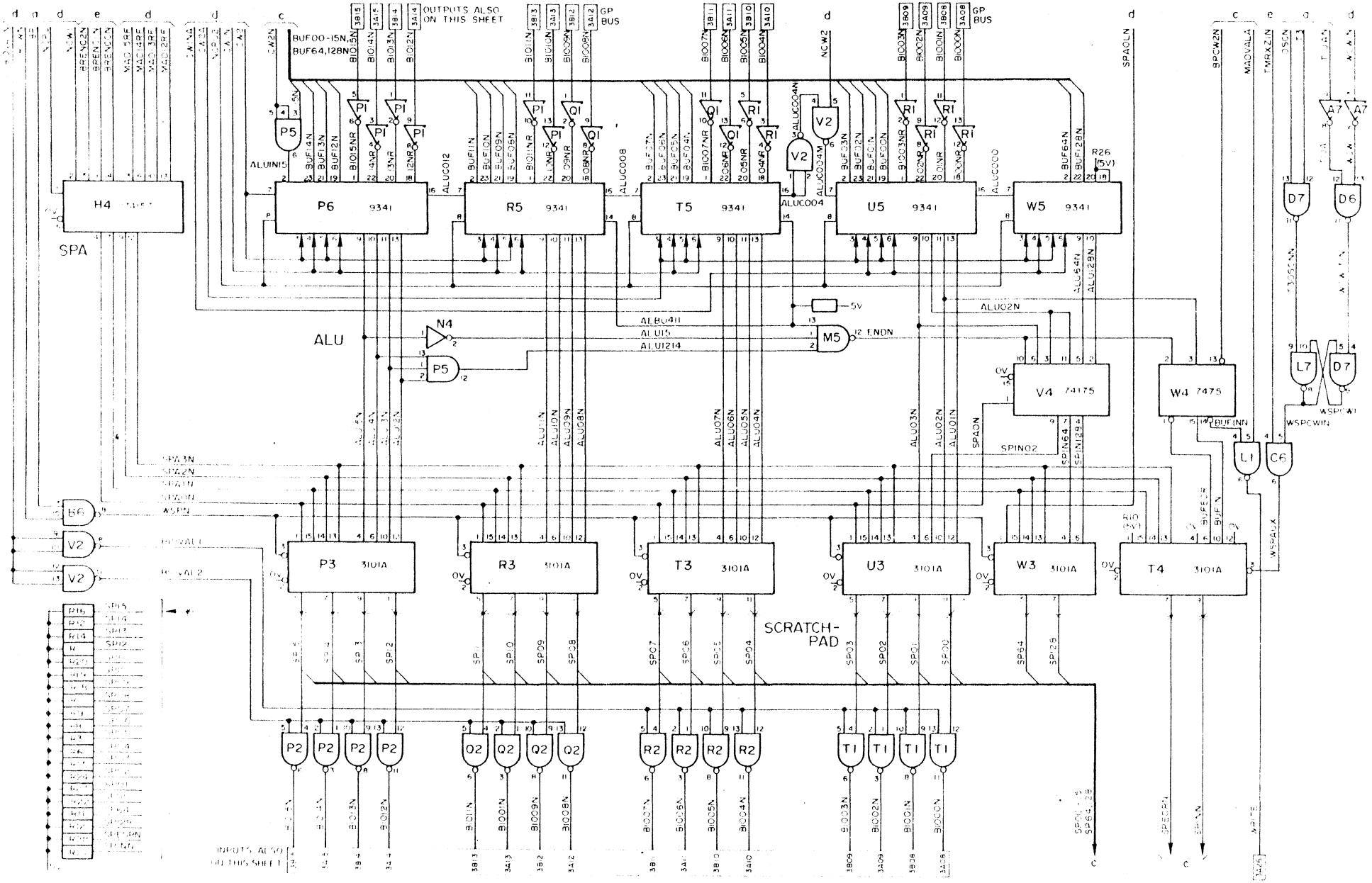


Figure B-9b ALU Scratchpad (1/2)

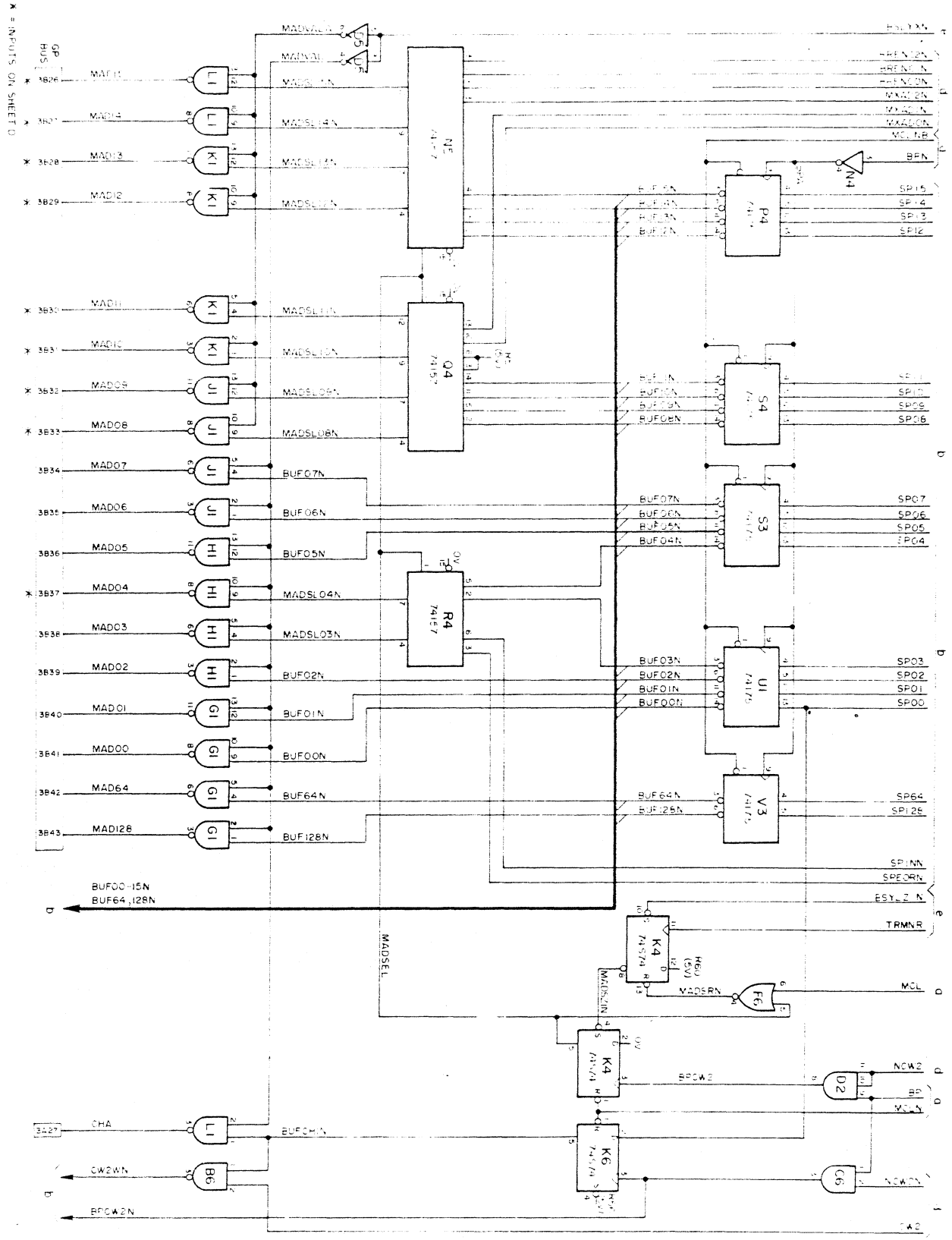
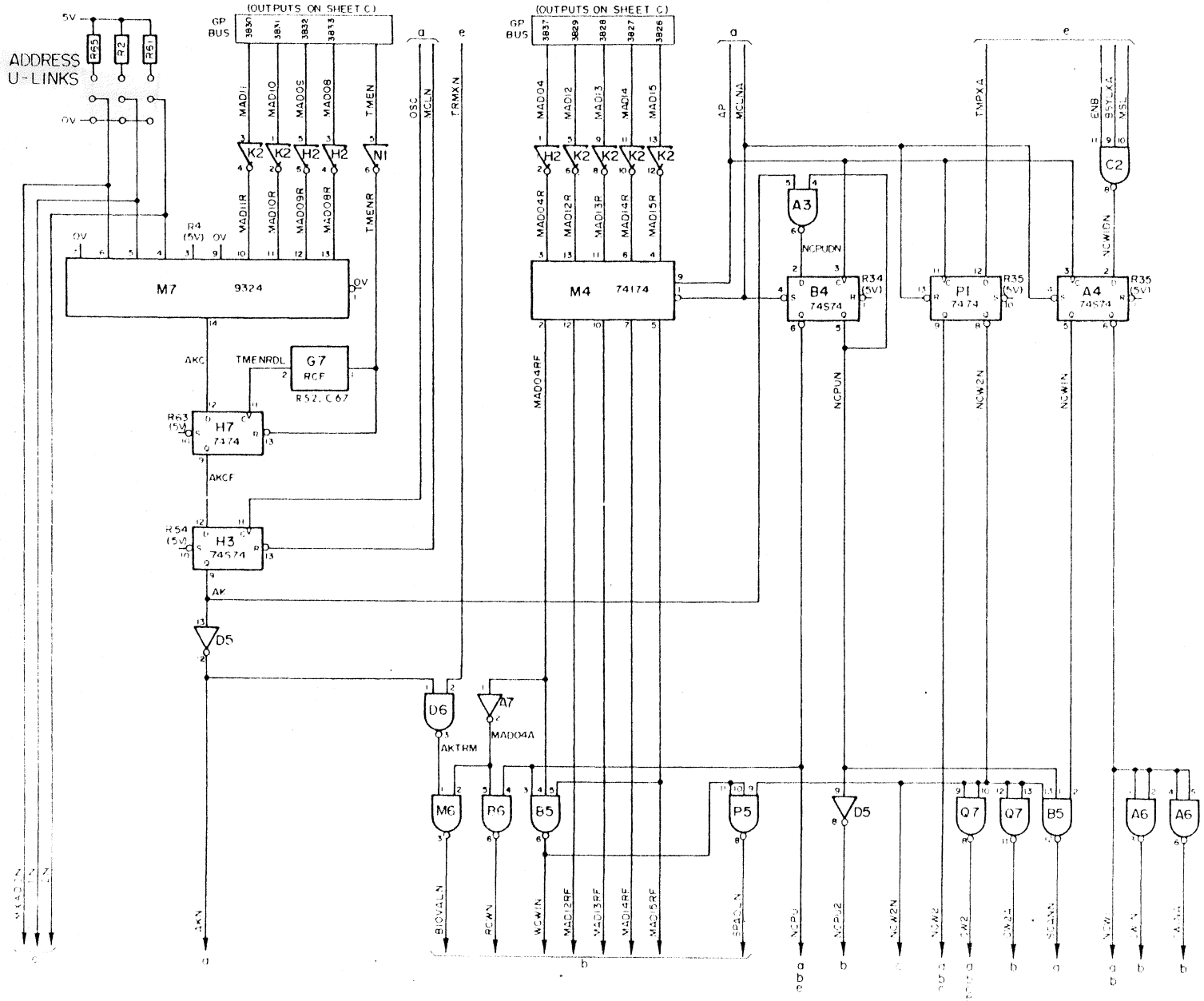


Figure B-9c Buffer, Address Generation (IOP)



igure B-9d Address Recognition, Execution Cyc OP)

REV 1

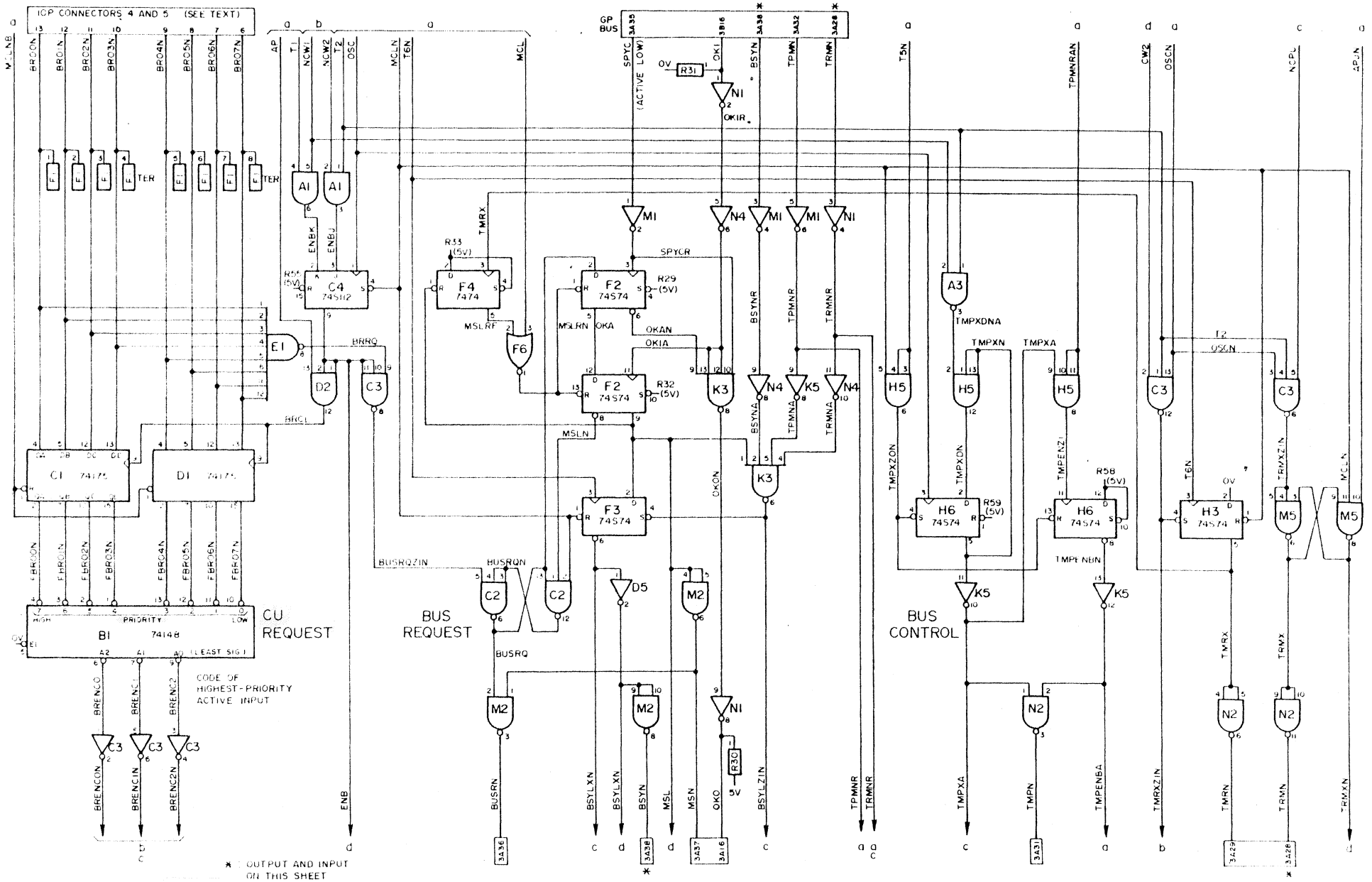


Figure B-9e Input/Output Control (IOP)

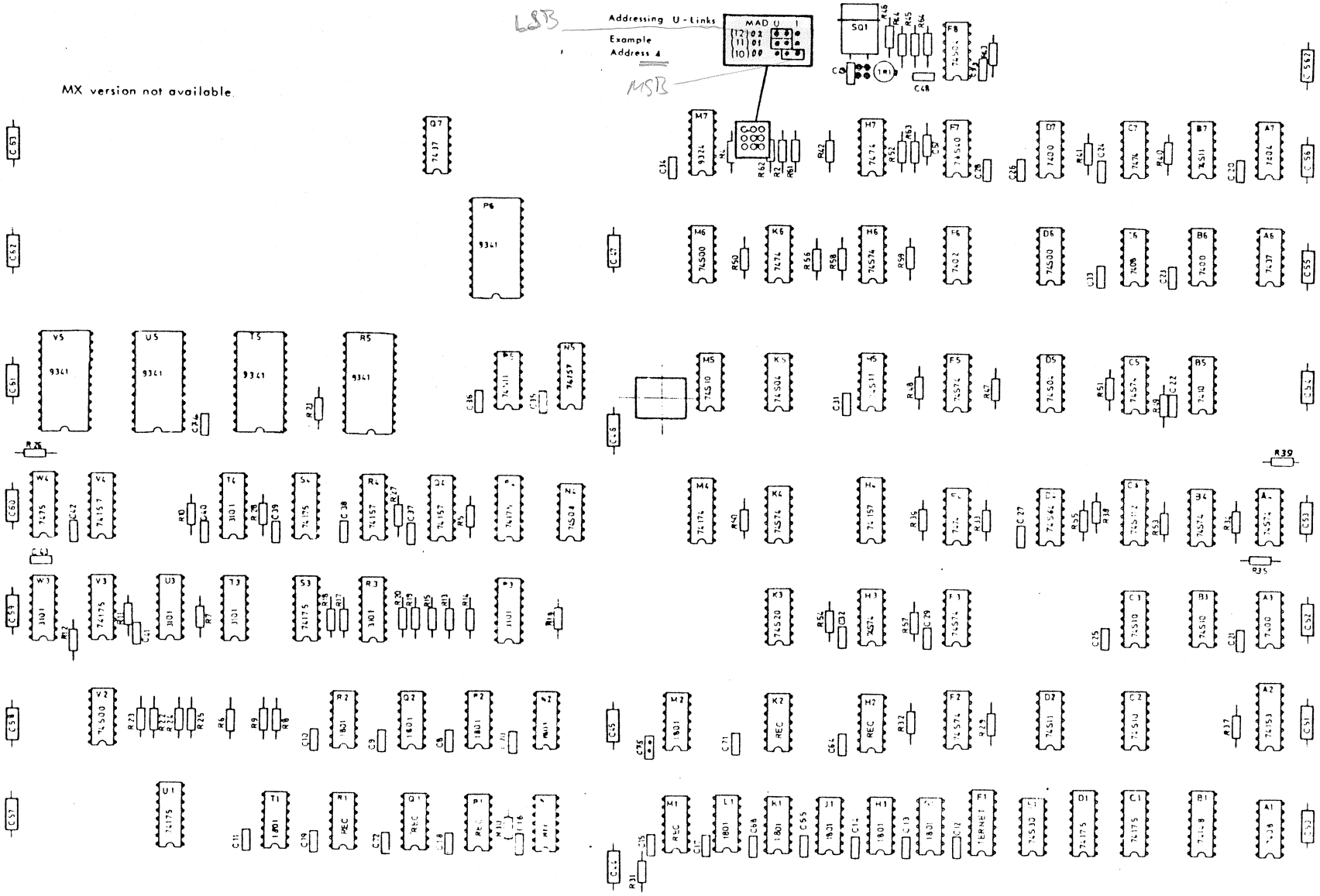


Figure 3-10 I/O Processor Layout (IOP)

Table B-1a Multiplex Card Parts List

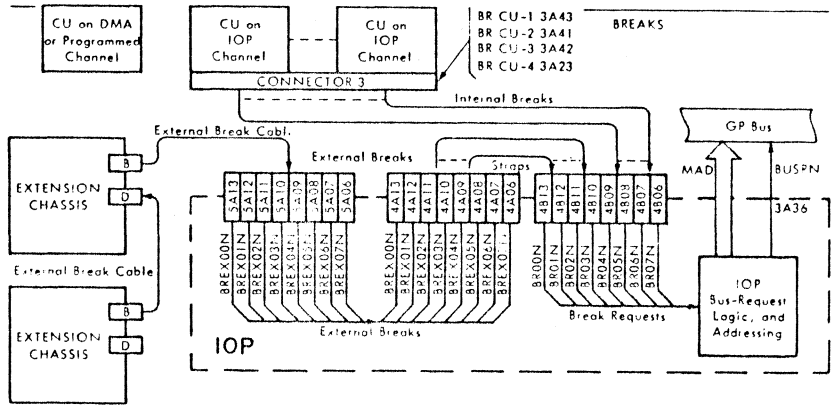
Reference	Description	12NC Code
	Printed circuit	5111 100 05473
[illegible],S2,S3,S5.	Integrated circuit 3101A	
[illegible]	Integrated circuit 7400	
C6.	Integrated circuit 7402	
[illegible]	Integrated circuit 7404	
[illegible]	Integrated circuit 7408	
[illegible]	Integrated circuit 7410	
D7,P7.	Integrated circuit 743[illegible]	
C5,P7,S7,T1.	Integrated circuit 7474	
P6.	Integrated circuit 7475	
B2	Integrated circuit 74148	
A7.	Integrated circuit 74153	
D3,F3,G3,K5,S6.	Integrated circuit 74157	
D2	Integrated circuit 74174	
A2,C2,[illegible],N3,P2,R3,T6.	Integrated circuit 74175	
B3	Integrated circuit 9324	
[illegible],N5,T2,T3,T5.	Integrated circuit 74181	
C[illegible],E[illegible],F1,G1,G2,H1,K2,L1,M1,N1.	Integrated circuit 1801	
B2,F2,H2,[illegible],L2,M2,N2.	Integrated circuit REC 0613	
	Integrated circuit 74H30	
B7.	Integrated circuit 74H53	
B4,P6.	Integrated circuit 74S00	
A5,C3,G5,P1.	Integrated circuit 74S04	
C4,C7,F6,N6.	Integrated circuit 74S10	
B7,D4,L6.	Integrated circuit 74S11	
B5.	Integrated circuit 74S20	
D5.	Integrated circuit 74S40	
A4,[illegible]5,B4,B6,D6,E5,E6,F5,G6.	Integrated circuit 74S74	
B3.	Integrated circuit 74S112	
B[illegible].	Ternet	
R43.	Resistor 215Ω, 1/8W, ±1%.	
R44.	Resistor 316Ω, 1/8W, ±1%.	
R45.	Resistor 2.15KΩ, 1/8W, ±1%.	
R46.	Resistor 3.16KΩ, 1/8W, ±1%.	
R3.	Resistor 330Ω, 1/4W, ±5%.	
R40.	Resistor 470Ω, 1/4W, ±5%.	
R4.	Resistor 510Ω, 1/4W, ±5%.	
R5-16,20-23,51,52.	Resistor 560Ω, 1/4W, ±5%.	
R17,24,31-39,47-50,53-58.	Resistor 1KΩ, 1/4W, ±5%.	
R2,19,28,29,30,42,61,62.	Resistor 3.3KΩ, 1/4W, ±5%.	
R1,18,25,26,27,41,59,60.	Resistor 5.6KΩ, 1/4W, ±5%.	
R63.	Resistor 100Ω, 1/8W, ±1%.	

Table B-1a contd.

Reference	Description	12NC Code
C48.	Capacitor 68pF, 63V, 2%, ceramic.	
C2,11,19,20,22,23,25,27-29,31,34,35,37,39,40,43,45-49,51-56,58,61-66,68-71,74-80.	Capacitor 10nF, ceramic.	
C10,38,67.	Capacitor 68µF, 16V, CTS13.	
C1,3-9,12-18,21,24,26,30,32,33,41,42,50,57,59,60,72,73,81.	Capacitor 3.3µF, 16V, CTS13.	
C82.	Capacitor 560pF, 10%.	
L1,L2.	Inductance.	
10.	U Link DCW06.	

Table B-1b IOP Parts List

Reference	Description	12NC Code
	Printed circuit	5111 100 06052
A3,B6,D7.	Integrated circuit 7400	
F5.	Integrated circuit 7402	
A7.	Integrated circuit 7404	
A1,C6.	Integrated circuit 7408	
B5.	Integrated circuit 7410	
A6,Q7.	Integrated circuit 7437	
C7,F4,H7,K6.	Integrated circuit 7474	
W4.	Integrated circuit 7475	
B1.	Integrated circuit 74148	
A2.	Integrated circuit 74153	
H4,N5,Q4,R4,V4.	Integrated circuit 74157	
M4.	Integrated circuit 74174	
C1,D1,P4,S3,S4,U1,V3.	Integrated circuit 74175	
P6,R5,T5,U5,V5.	Integrated circuit 74181 (9341)	
M7.	Integrated circuit 9324	
P3,R3,T3,T4,U3,W3.	Integrated circuit 3101A	
G1,H1,J1,K1,L1,M2,N2,P2,Q2,R2,T1.	Integrated circuit 1801	
H2,K2,M1,N1,P1,Q1,R1.	Integrated circuit REC 0613	
D6,M6,V2.	Integrated circuit 74S00	
D5,F8,K5,N4.	Integrated circuit 74S04	
B3,C2,C3,M5.	Integrated circuit 74S10	
B7,D2,H5,P5.	Integrated circuit 74S11	
K3.	Integrated circuit 74S20	
E1.	Integrated circuit 74S30	
F7.	Integrated circuit 74S40	
D4.	Integrated circuit 74S64	
A4,B4,C5,F2,F3,F5,H3,H6,K4.	Integrated circuit 74S74	
C4.	Integrated circuit 74S112	
R43.	Resistor 464n, 1/8W, 1%.	
R64.	Resistor 681n, 1/8W, 1%.	
R44.	Resistor 1.47Kn, 1/8W, 1%.	
R45.	Resistor 2.15Kn, 1/8W, 1%.	
R46.	Resistor 3.16Kn, 1/8W, 1%.	
R52.	Resistor 100n, 1/8W, 1%.	
R30.	Resistor 330n, 1/4W, 5%.	
R31.	Resistor 510n, 1/4W, 5%.	
R6-9,11-20,22-25,27,28.	Resistor 560n, 1/4W, 5%.	
R2,4,5,10,21,26,29,32-42,47-51,53-63.	Resistor 1Kn, 1/4W, 5%.	
C44-47.	Capacitor 47μF, 10V, electro.	
C50-63,562.	Capacitor 10μF, 25V, electro.	
C67.	Capacitor 560pF, 12V, 1%, micropacco	
C49.	Capacitor 470pF, ceramic.	
C48.	Capacitor 33pF, ceramic.	
C8-29,31-43,64,65,68,70-75.	Capacitor 10nF, ceramic.	
F1.	Fernet Resistor	
TR1.	Transistor BSX20	
Y1.	Quartz 20MHz QA60A Option BCW05	



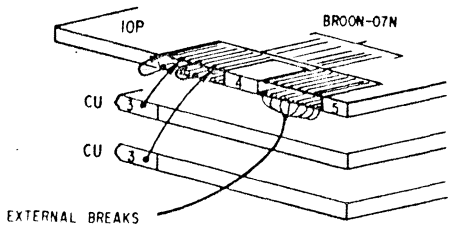


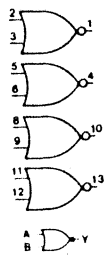
Figure B-11 Break-Request Signal Connections (IOP)

1801

see 7400)

7402

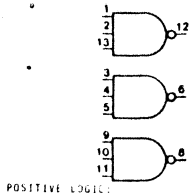
QUADRUPLE 2-INPUT
POSITIVE-NOR GATE



Vcc 14
GND 7

7410

7410



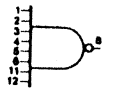
POSITIVE LOGIC:
Y=ABC

Vcc 14
GND 7

7430

7430

8-INPUT NAND GATE

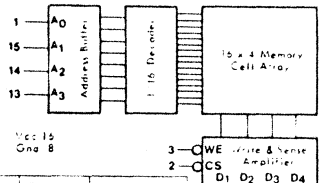


Vcc 14
GND 7

N.C.: 9,10,12

3101

3101 HIGH SPEED FULLY DECODED 64 BIT MEMORY

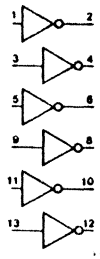


Vcc 16
Gnd 8

CS	WE	Operation	Output
L	L	Write	H
L	H	Read	Complement of written Data
H	L		H
H	H		H

7404

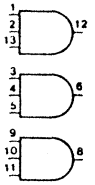
7404, S04, H04
7406
7414
7416



Vcc 14
GND 7

7411

7411



POSITIVE LOGIC:
Y=ABC

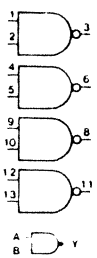
7437

(see 7400)

7400

7400
S00
H00
03
37
38
1801

1 open collector
2 buffer



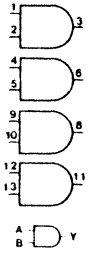
Y=AB

Vcc 14
GND 7

7408

7408
091

1 open collector

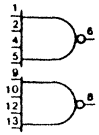


Y=AB

7420

7420 7440

BUFFER



POSITIVE LOGIC:
Y=ABCD

3,11 N.C.

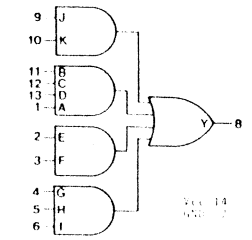
Vcc 14
GND 7

7440

(see 7420)

Figure B-12a IOP IC Guide

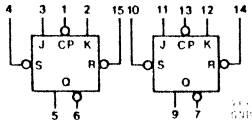
7464



74112

74S112

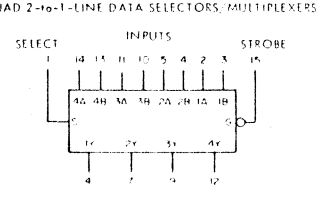
J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS



FUNCTION TABLE					
INPUTS				OUTPUTS	
S	R	CP	J	K	Q
L	H	X	X	X	H
H	L	X	X	X	L
L	L	↓	L	L	Q_0
H	H	↓	L	H	L
H	H	↓	H	L	H
H	H	↓	H	H	TOGGLE
H	H	H	X	X	Q_0

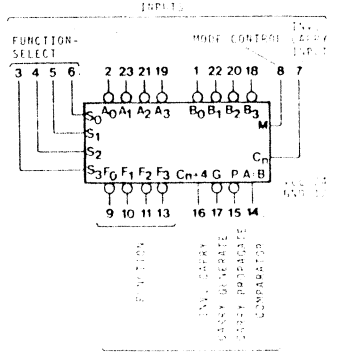
74157

QUAD 2-to-1-LINE DATA SELECTORS/MULTIPLEXERS



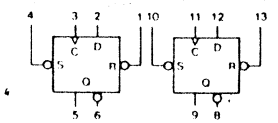
74181

ARITHMETIC LOGIC UNIT



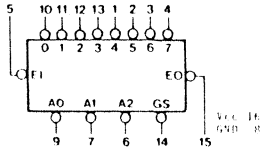
7474

7474, H74, S74



74148

8-LINE-TO-3-LINE PRIORITY ENCODER



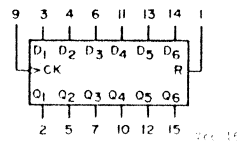
FUNCTION TABLE

INPUTS								OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	L	H
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

74174

74174

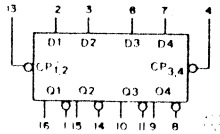
HEX D-TYPE FLIP-FLOPS WITH COMMON CLOCK AND RESET



FUNCTION TABLE			
INPUTS			OUTPUTS
R	CK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

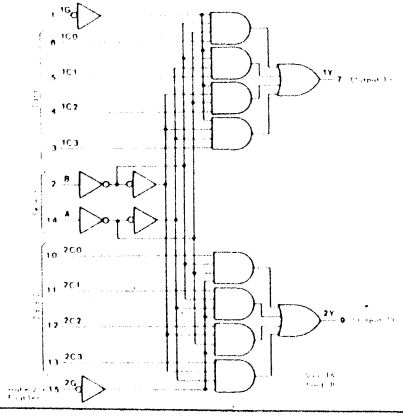
7475

7475



74153

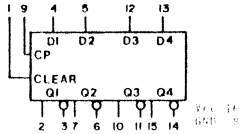
DUAL 4-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER



74175

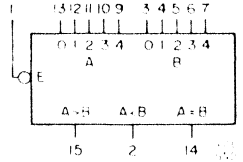
74175

QUAD D-TYPE FLIP-FLOPS



FUNCTION TABLE				
INPUTS			OUTPUTS	
R	C	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

9324



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