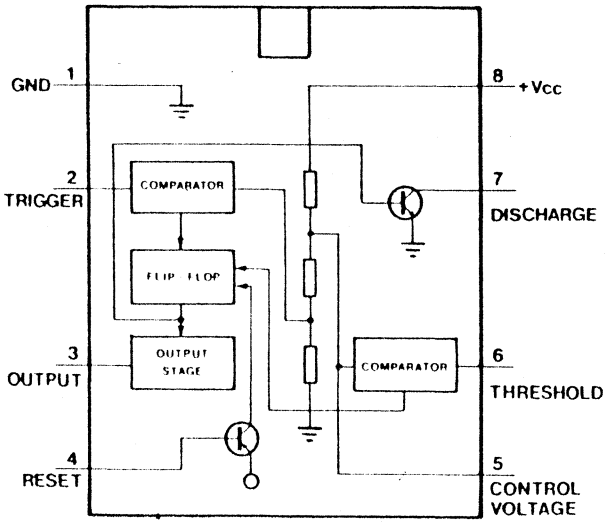
NE555V

TIMER

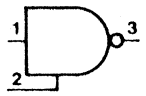


1489

(75 rec 189/75100 transmit)

1489A

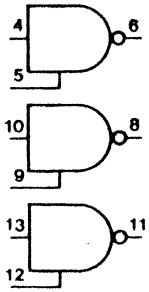
LINE RECEIVER



Response control gives:

a) Logic threshold shifting

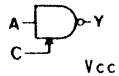
b) Input noise filtering



POSITIVE LOGIC:

$Y = \overline{A}$

C = response comtrol

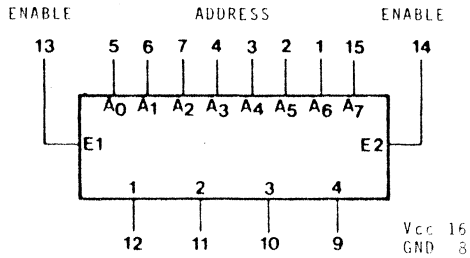


Vcc 14
GND 7

configure dip type 10% 9600 Baud ≈ 30 m.

6200

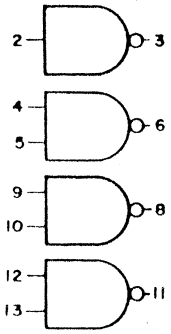
1024-BIT ROM (256x4) O.C.



1488

1488

QUAD MDTL LINE DRIVER



7 - 0V

14 - V+ - +15V max

1 - V- - -15V max

1801

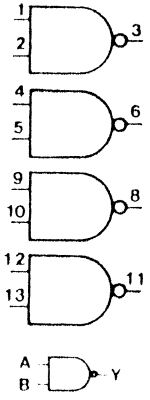
(see 7400)

7400

7400
S00
H00
03[1]
37[2]
38
1801[1]

1 open collector

2 buffer

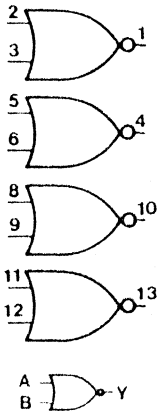


$Y = \overline{AB}$

Vcc 14
GND 7

7402

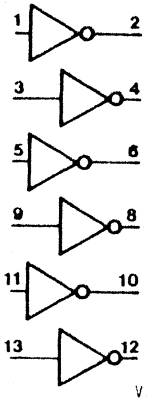
QUADRUPLE 2-INPUT
POSITIVE-NOR GATE



Vcc 14
GND 7

7404

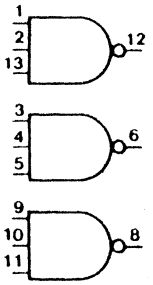
7404, S04, H04
7406 o.c. 30V
7414 sh Tris
7416 o.c. 15V



Vcc 14
GND 7

7410

7410



POSITIVE LOGIC:
$Y=\overline{ABC}$

Vcc 14
GND 7

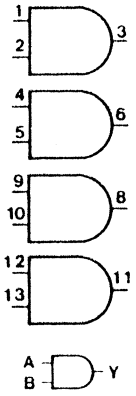
7403

(see 7400)

7408

7408
$0 9^{1}$

1 open collector

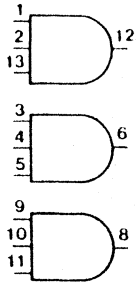


$Y=AB$

Vcc 14
GND 7

7411

7411



POSITIVE LOGIC:
$Y=ABC$

Vcc 14
GND 7

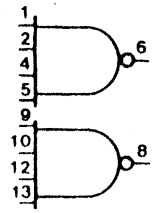
7416

(see 7404)

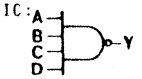
7420

7420 7440

BUFFER



POSITIVE LOGIC:
$Y=\overline{ABCD}$

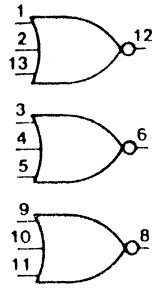


3,11 N.C

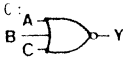
Vcc 14
GND 7

7427

7427

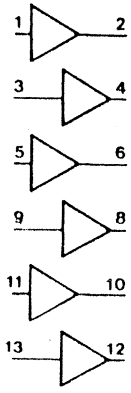


POSITIVE LOGIC:
$Y=\overline{A+B+C}$



Vcc 14
GND 7

7417

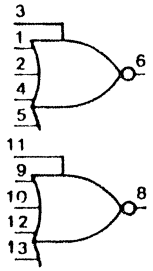


Vcc 14
GND 7

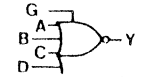
7425

7425

4-INPUT NOR
WITH STROBE



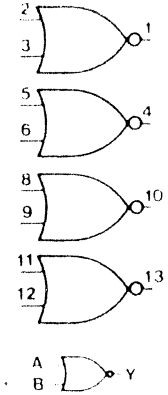
POSITIVE LOGIC:
$Y=\overline{G(A+B+C+D)}$



Vcc 14
GND 7

7428

2-Input Positive-NOR-Buffer



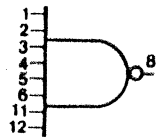
Vcc 14
GND

Positive Logic: $Y = \overline{A+B}$

7430

7430

8-INPUT NAND GATE



Vcc 14
GND 7

N.C. 9,10,13

7437

7438

(see 7400)

7453

7453 (EXPANDABLE)

7454

4-WIDE
AND-OR-INVERT

POSITIVE LOGIC:

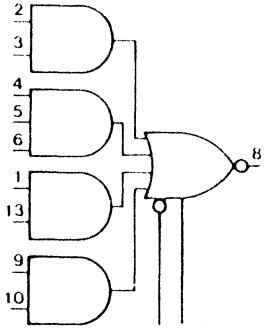
'53
$Y=\overline{AB+CD+FG+HI+X}$

'H53
$Y=\overline{AB+CDE+FG+HI+X}$

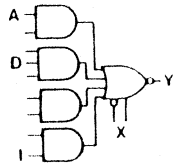
'54
$Y=\overline{AB+CD+FG+HI}$

'H54
$Y=\overline{AB+CDE+FG+HI}$

H53,H54 only



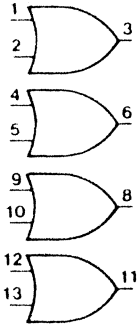
(12 11)/454 only



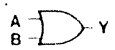
Vcc 14
GND 7

7432

7432



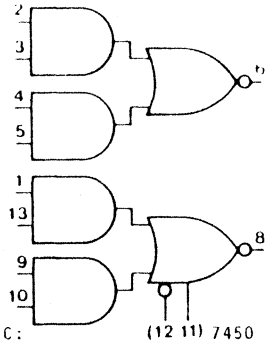
POSITIVE LOGIC:
$Y=A+B$



Vcc 14
GND 7

7450

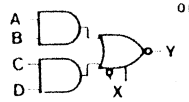
2-WIDE
2-INPUT
AND-OR-INVERT



(12 11) 7450 only

POSITIVE LOGIC:
$Y=\overline{AB+CD+X}$

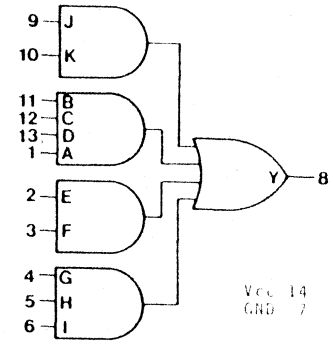
X=OUTPUT OF
7460,7462



Vcc 14
GND 7

7464

4-2-3-2-INPUT AND-OR-INVERT GATES



Vcc 14
GND 7

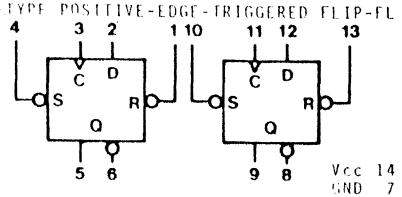
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	L	X	X	Q_0	$\overline{Q}_0$

Positive Logic: $Y=ABCD+EF+GHI+\overline{JK}$

7474

7474, H74, S74

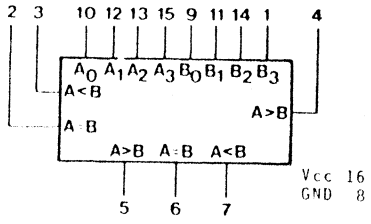
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FL

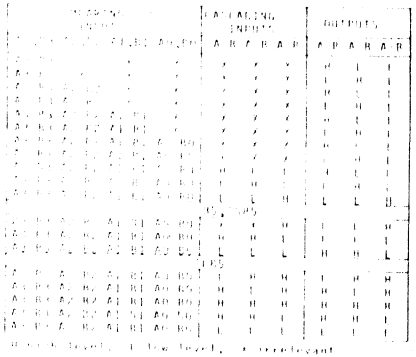


FUNCTION TABLE					
INPUTS				OUTPUTS	
S	R	C	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

7485

4-BIT MAGNITUDE COMPARATOR

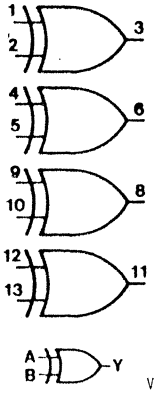




7486

7486

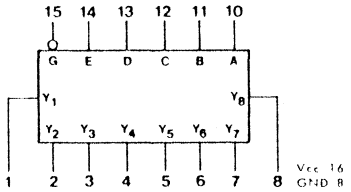
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES



Positive Logic: $Y = A \oplus B = \bar{A}B + A\bar{B}$

7488

256 BIT READ-ONLY MEMORY

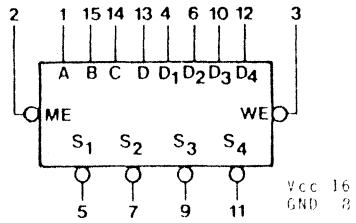


WORD-SELECT TABLE

WORD	INPUTS E	D	C	B	A	WORD	INPUTS E	D	C	B	A
0	L	L	L	L	L	16	H	L	L	L	L
1	L	L	L	L	H	17	H	L	L	L	H
2	L	L	L	H	L	18	H	L	L	H	L
3	L	L	L	H	H	19	H	L	L	H	H
4	L	L	H	L	L	20	H	L	H	L	L
5	L	L	H	L	H	21	H	L	H	L	H
6	L	L	H	H	L	22	H	L	H	H	L
7	L	L	H	H	H	23	H	L	H	H	H
8	L	H	L	L	L	24	H	H	L	L	L
9	L	H	L	L	H	25	H	H	L	L	H
10	L	H	L	H	L	26	H	H	L	H	L
11	L	H	L	H	H	27	H	H	L	H	H
12	L	H	H	L	L	28	H	H	H	L	L
13	L	H	H	L	H	29	H	H	H	L	H
14	L	H	H	H	L	30	H	H	H	H	L
15	L	H	H	H	H	31	H	H	H	H	H

7489

64-BIT READ/WRITE MEMORY

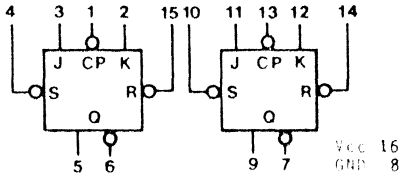


ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	↓	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High

74112

74S112

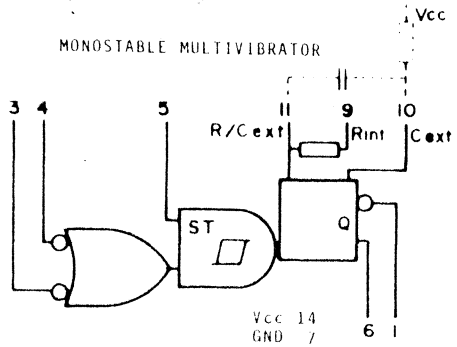
J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS



FUNCTION TABLE						
INPUTS					OUTPUTS	
S	R	C	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	H	H
L	L	X	X	X	H	H
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

74121

MONOSTABLE MULTIVIBRATOR



To use the internal timing resistor connect Rint to Vcc.

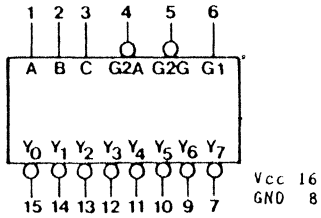
An external timing capacitor may be connected between Cext and Rext/Cext.

For accurate repeatable pulse widths, connect an external resistor between Rext/Cext and Vcc with Rint open-circuited.

To obtain variable pulse widths, connect external variable resistance between Rint or Rext/Cext and Vcc.

74138

DECODER



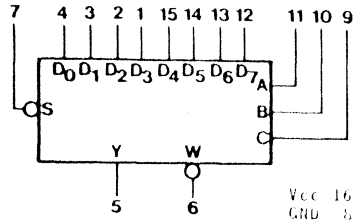
FUNCTION TABLE

INPUTS				OUTPUTS							
ENABLE G1	'G2	SELECT C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

'G2 = G2A+G2B

74151

DATA SELECTOR/MULTIPLEXER



FUNCTION TABLE

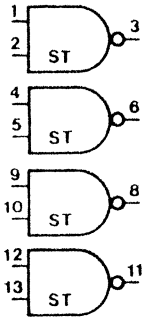
INPUTS					OUTPUTS	
SELECT C	B	A	STROBE		Y	W
X	X	X	H		L	H
L	L	L	L		D0	D0
L	L	H	L		D1	D1
L	H	L	L		D2	D2
L	H	H	L		D3	D3
H	L	L	L		D4	D4
H	L	H	L		D5	D5
H	H	L	L		D6	D6
H	H	H	L		D7	D7

D0,D1...D7 = the level of the D respective input

74132

74132

POSITIVE NAND SCHMITT TRIGGER



POSITIVE LOGIC:

Y=AB

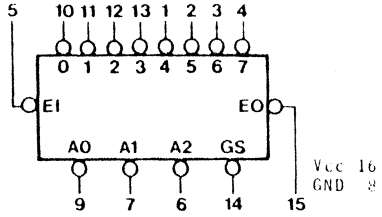
Vcc 14
GND 7

Positive going threshold V=1.7

Negative going threshold V=0.9

74148

8-LINE-TO-3-LINE PRIORITY ENCODER

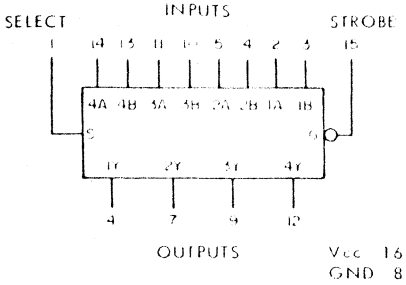


FUNCTION TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

74157

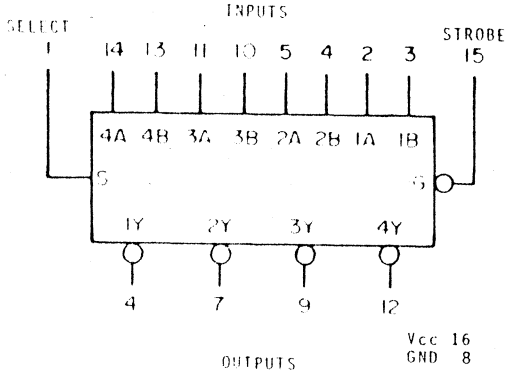
QUAD 2-to-1-LINE DATA SELECTORS/MULTIPLEXERS



74158

74158

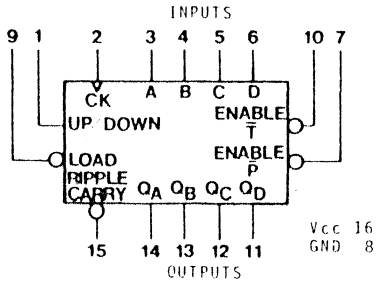
QUAD 2-to-1-LINE DATA SELECTORS/MULTIPLEXERS



74169

74169

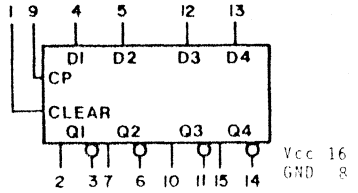
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS



74175

74175

QUAD D-TYPE FLIP-FLOPS



FUNCTION TABLE				
INPUTS			OUTPUTS	
R	C	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

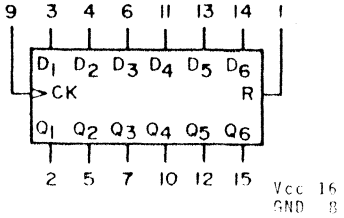
74161

(see 9310)

74174

74174

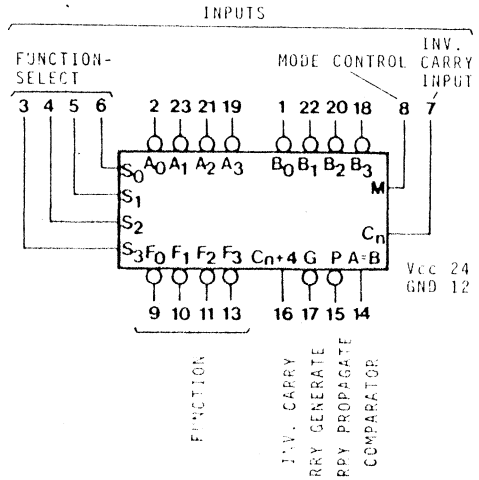
HEX D-TYPE FLIP-FLOPS WITH COMMON CLOCK AND RESET

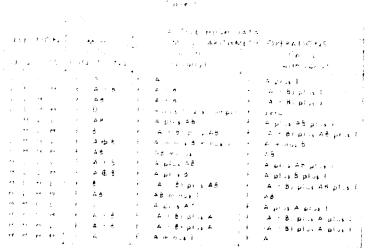


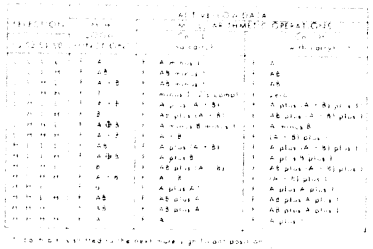
FUNCTION TABLE				
INPUTS			OUTPUTS	
R	C	D	Q	$\bar{Q}$t
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

X

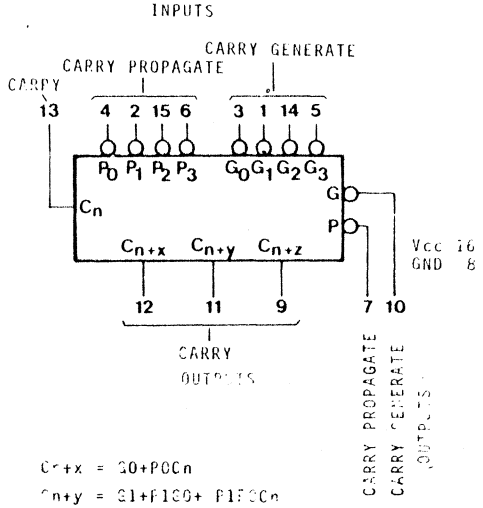
74181 ARITHMETIC LOGIC UNIT







74182 LOOK-AHEAD CARRY GENERATOR



$C_{n+x} = G_0+P_0C_n$

$C_{n+y} = G_1+P_1G_0+P_1P_0C_n$

$C_{n+z} = G_2+P_2G_1+P_2P_1G_0+P_2P_1P_0C_n$

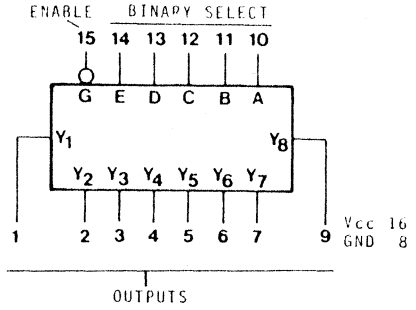
$G = G_3(P_3+G_2)\ (P_3+P_2+G_1)\ (P_3+P_2+P_1+G_0)$

$P = P_3P_2P_1P_0$

74188

74188A

256-BIT PROGRAMMABLE READ-ONLY MEMORY

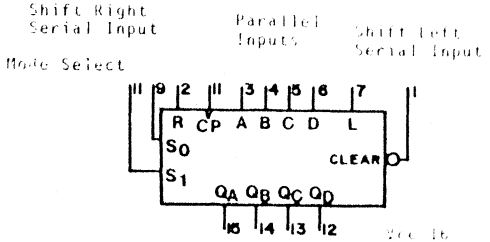


Organized as 32 Words of 8 Bits Each

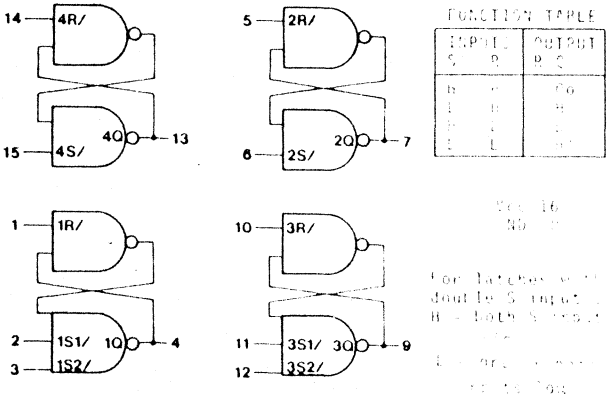
74194

74194

4-BIT SHIFT REGISTER



74279 QUADRUPLE S-R LATCHES



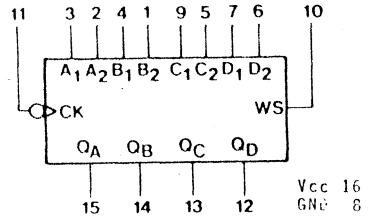
For latches with double S inputs:
H = both S inputs high
L = one or both S inputs low
X = either H or L

Q_0 = the level of Q before the indicated input conditions were established.

* This output level is pseudo stable; that is, it may not persist when the S and R inputs return to their inactive (high) level.

74298

QUADRUPLE 2-INPUT MULTIPLEXER WITH STORAGE



FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	QA	QB	QC	QD
↓	↑	a1	b1	c1	d1
↓	↑	a2	b2	c2	d2
↑	↑	QA0	QB0	QC0	QD0

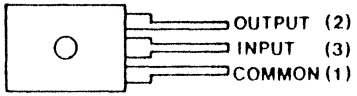
a1,a2,etc. = the level of steady-state input at A1,A2,etc.

QA0,QB0,etc. = the level of QA,QB,etc. entered on the most-recent ↑ transition of the clock input.

7905

7905 (-5V)

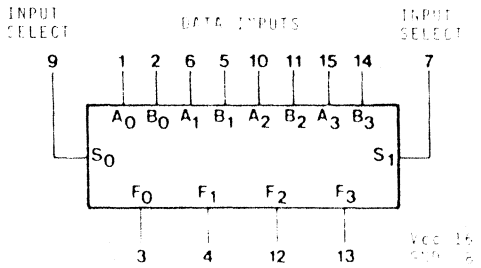
NEGATIVE VOLTAGE REGULATOR



8234

8234

QUAD 2-INPUT MULTIPLEXER



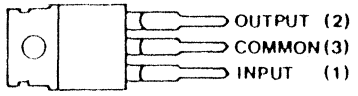
S0	S1	Selects
0	0	A
0	1	B
1	0	C
1	1	High Out

7812
7815
7912

7812C (+12V)

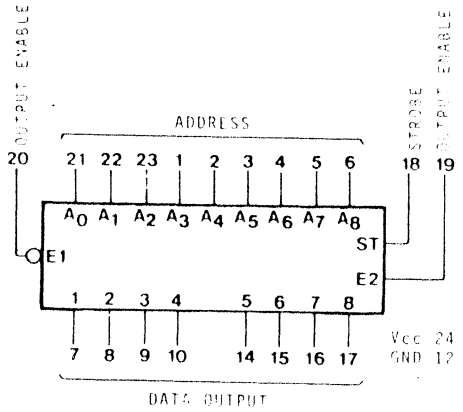
7815C (+15V)

POSITIVE VOLTAGE REGULATOR



8205

512x8 PROM WITH 3 STATE OUTPUTS



Strobe High: E1/E2 gate the output

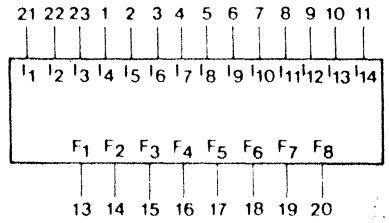
Strobe Low: Last addressed word is stopped at the output

8576

8576

PLA DATA SHEET

DATA INPUTS



OTHER OUTPUTS

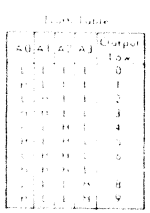
PLA - Programmable Logic Array

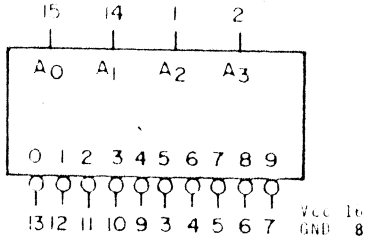
96 Input combinations are coded
(Refer to code table for specific part

9301

9301

ONE-OF-TEN DECODER

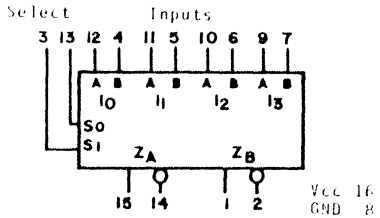




Multipurpose Decoder will accept four inputs and provide 10 mutually exclusive outputs.

9309

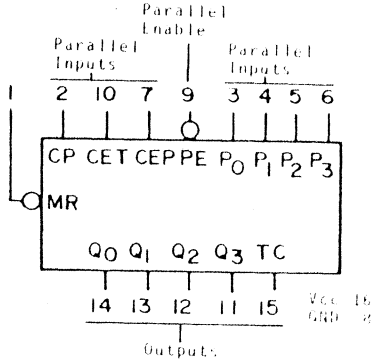
DUAL, 4-INPUT MULTIPLEXER



9316

9316

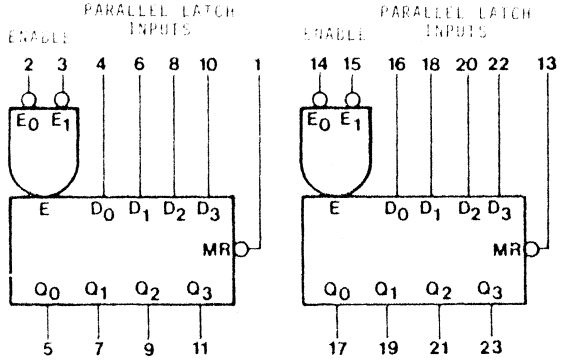
4-BIT BINARY COUNTER



TC = $Q_0 Q_1 Q_2 Q_3$ CEP

9308

8-BIT FOUR-BIT LATCH



FUNCTION TABLE

MR	E0	E1	D	Qn	OPERATION
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	Qn-1	Hold
H	H	L	X	Qn-1	Hold
H	H	H	X	Qn-1	Hold
L	X	X	X	L	Reset

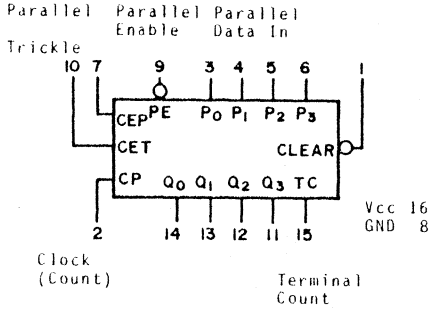
Vcc 24
GND 12

Qn-1 = Previous Output State
Qn = Present Output State

9310

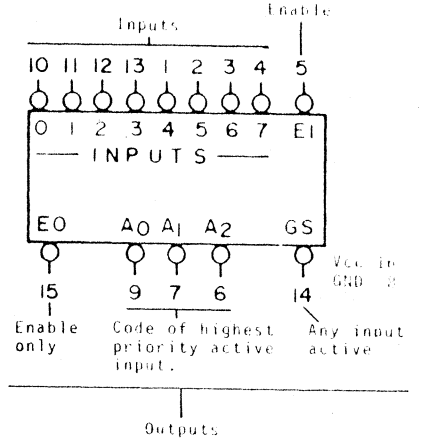
9310, 74161

BCD COUNTER
BINARY COUNTER



9318

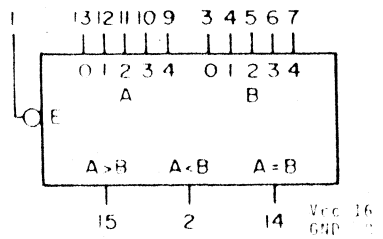
EIGHT-INPUT PRIORITY ENCODER



9318 is a Multipurpose Encoder designed to accept eight inputs and produce a binary weighted code of the highest order input.

9324

4-BIT COMPARATOR



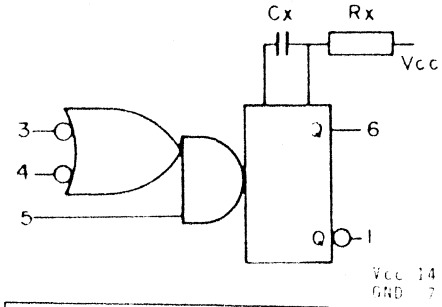
A fast, expandable Comparator that performs comparison between two 5-bit words and gives three outputs, "less than", "greater than" and "equal to". A HIGH level on the active LOW enable input forces all three outputs LOW.

93403

(see 7489)

9603

SINGLE SHOT WITH SCHMITT TRIGGER INPUT



FUNCTION TABLE						
t_n	INPUT	t_{n+1}	INPUT			OUTPUT
L	X		L	X	H	Trigger
X	L		X	L	H	Trigger
H	H		X	L	H	Trigger
H	H	H	L	X	H	Trigger

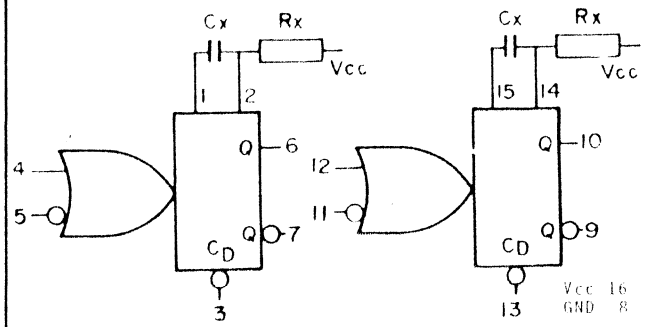
→ = Triggering Transition

9341

(see 74181)

9602

SINGLE SHOT



TRIGGERING FUNCTION TABLE			
PIN NO'S 5(11)	4(12)	3(13)	Operation
H-L	L	H	Trigger
H	L-H	H	Trigger
X	X	L	Reset

Dual Retriggerable, Resettable Monostable Multivibrator provides an output pulse whose duration and accuracy is a function of external timing components Ex and Rx.

ADL2011
CR202A

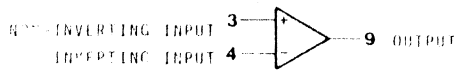
(see 74188)

REC 0613

(see 7404)

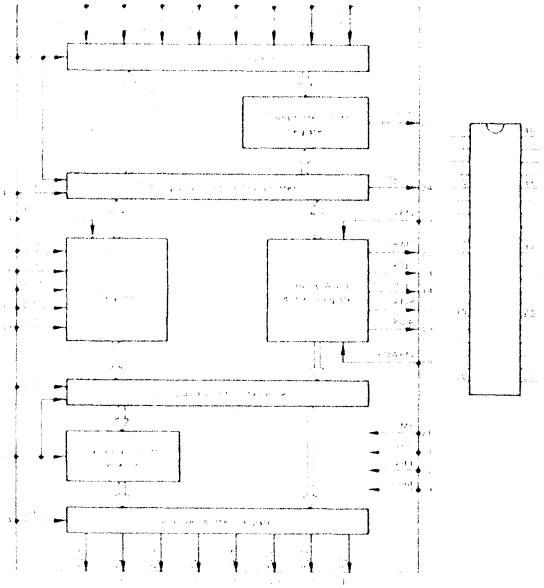
µA710DC

HIGH SPEED DIFFERENTIAL COMPARATOR



GND 2
+V 11
-V 6

UART



µA 723

µA723

PRECISION VOLTAGE REGULATOR