APPENDICES

In this manual, for descriptive purposes only, Type 1 control units have been defined as those control units connected directly to the GP bus and Type 2 control units as those units connected to the I/O bus.

When using Type 2 control units in an Equipment shelf E1 (described in Section 1 Part 2) a Bus Translator board is provided with the shelf to translate signals on the I/O bus into GP bus signals. The translator board contains signal and timing facilities, interrupt encoding circuits, and break request line terminations which enable up to eight Type 2 control units to be added to the system. The additional control units can be connected to the I/O processor channel or to the programmed channel but they cannot act as bus master. System protection against power failure is also provided on the board.

If the total GP bus length is greater than 1 metre, then the bus must be terminated at both ends and if less than 1 metre in length then it is only required to terminate at the basic mounting box end. To allow for the two possibilities the Equipment Shelf E1 is provided in two forms; in one form it contains a Bus Translator board on which bus termination facilities are provided (P843-008) and in a second form the bus line terminations are omitted (P843-007)

SYSTEM EXTENSION

A possible system arrangement showing the interconnections when using 3 Equipment Shelves E1 is shown in Figure A1.1. Note that the Bus Translator also provides the facility for extending the GP bus between Equipment Shelves. If all the eight break request lines connected to a Bus Translator are not required in an Equipment Shelf then the lines can be daisy-chained to the next Equipment Shelf as described later in this Chapter.

INTERFACE SIGNALS - GP BUS

The diagram in Figure A1.2 shows the GP Bus and I/O signals which are interfaced when using the Bus Translator boards.

Only the GP Bus interface signals used for control unit transactions are needed and these signals are described in Section 1, Part 1, Chapter 2 of this manual. The interface timing for a master to control unit exchange using programmed channel is given in Section 1, Part 1, Chapter 3 and the timing for a memory to control unit exchange using the I/O processor channel is described in Section 1, Part 1, Chapter 4. Details of the component characteristics used for transmitting or receiving the signals are given in Section 1, Part 2, Chapter 2.

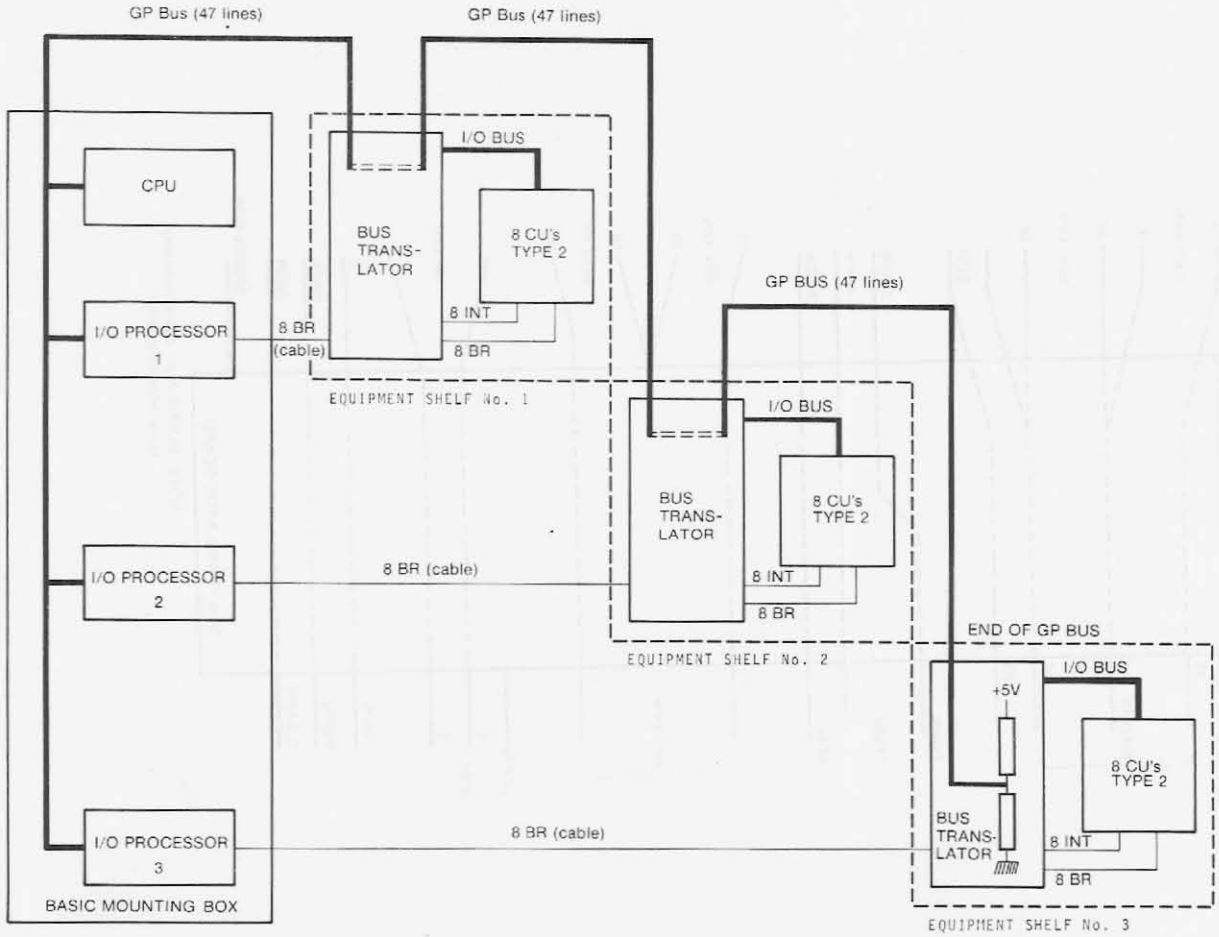


Figure A1.1 System using bus translator boards

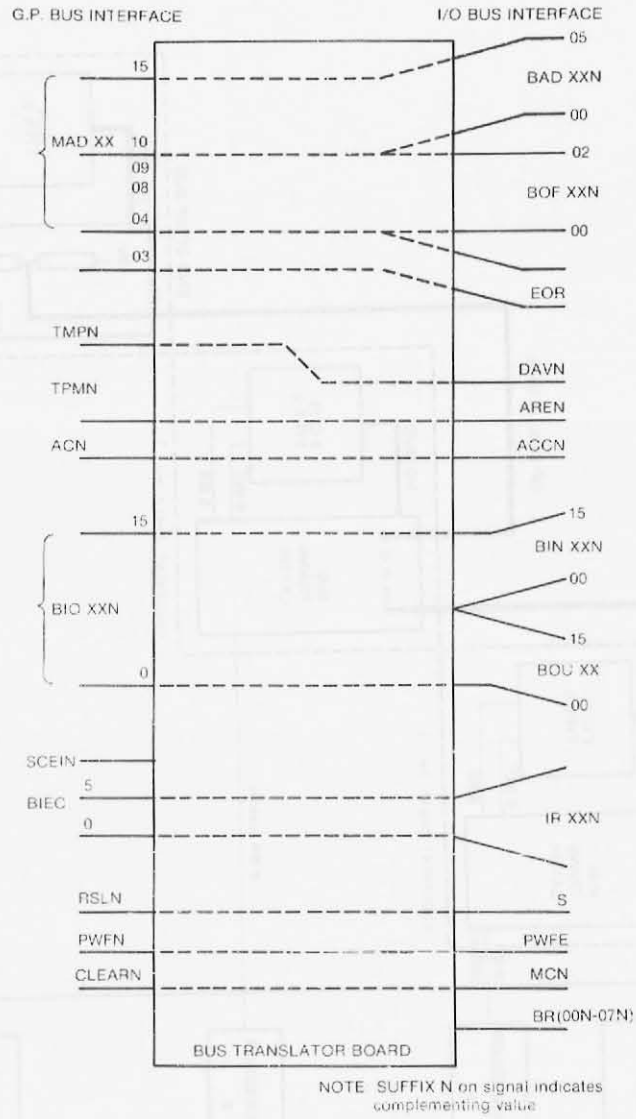


Figure A1.2Interface signals

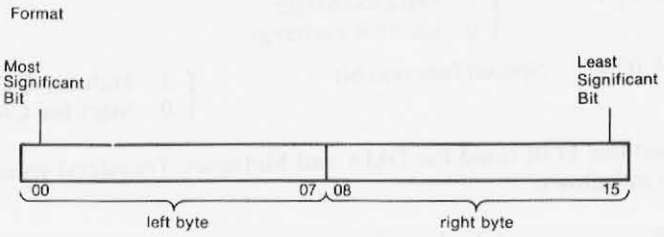
INTERFACE SIGNALS - I/O BUS

The I/O Bus interface signals shown in Figure A1.2 are described below:

Data Lines

Data Input Lines BIN 00N to 15N.

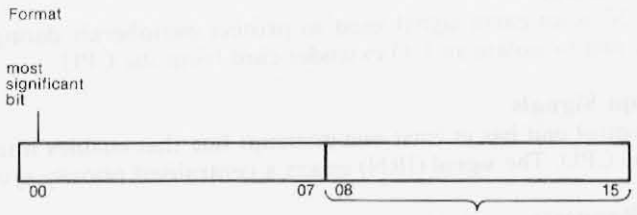
These are 16 unidirectional lines carrying data from a control unit connected on the bus.



When a control unit exchanges less than 16 bits it uses the rightmost bits of the BIN lines. If the control unit transfers per character (byte) in multiplex mode it should use the right character.

Output Lines BOU 00 to 15

These are 16 unidirectional lines carrying data to a control unit connected on the bus (the value transferred is the true value).

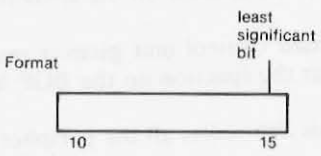


When a control unit exchanges less than 16 bits per word it uses the rightmost bits. If the control unit receives characters in multiplex mode it should use the right character.

Address Lines

Address Lines BAD 00N to 05N

These lines carry the 6-bit number defining the device address.



Function Lines

Function lines BOF 00N to 02N

These 3 lines carry a code which specifies the function to be performed. The code on each line is as follows:

BOF 00N
- 1 Exchange to control unit
- 0 Exchange from control unit

BOF 01N
- 1 Data exchange
- 0 Control exchange

BOF 02N Special function bit
- 1 Halt for CIO
- 0 Start for CIO

Signal line EOR (used for DMA and Multiplex Transfers) specifies the function also as follows:

EOR
- 1 Last data exchange
- 0 Not the last data exchange.

Timing Signal

Timing signal DAVN

This signal provides Device Address Validation and is used for address validation and exchange synchronisation within the control unit.

Power Control

Signal "S" is an earth signal used to protect peripherals during a decrease of voltage and to isolate an I/O extender card from the CPU.

Interrupt Signals

Each control unit has at least one interrupt line that enables it to obtain service from the CPU. The signal (IRN) enters a centralised priority system.

Break Requests

One break request signal BRN is sent from each control unit directly to the multiplex that handles its transfers.

Miscellaneous Signals

The following signals are also used during an exchange:

AREN: The addressed control unit gives a response on this signal line to indicate that the address on the BAD lines has been recognised.

ACCN: The addressed control unit gives a response on this signal line to indicate that the function on the BOF lines has been accepted.

MCN: A "0" on this line resets all the peripheral control units.

INTERFACE TIMING I/O BUS

The interface timing for a data transfer to a control unit (OTR/CIO instruction) is shown in Figure A1.3

During this exchange the control unit that decodes its address asserts AREN and ACCN, if it accepts the function. The unit samples the data on the DAVN rising edge, which occurs at a fixed time whatever the control unit answer is.

The interface timing for a data transfer to a control unit (INR/SST/TST instruction) is shown in Figure A1.4

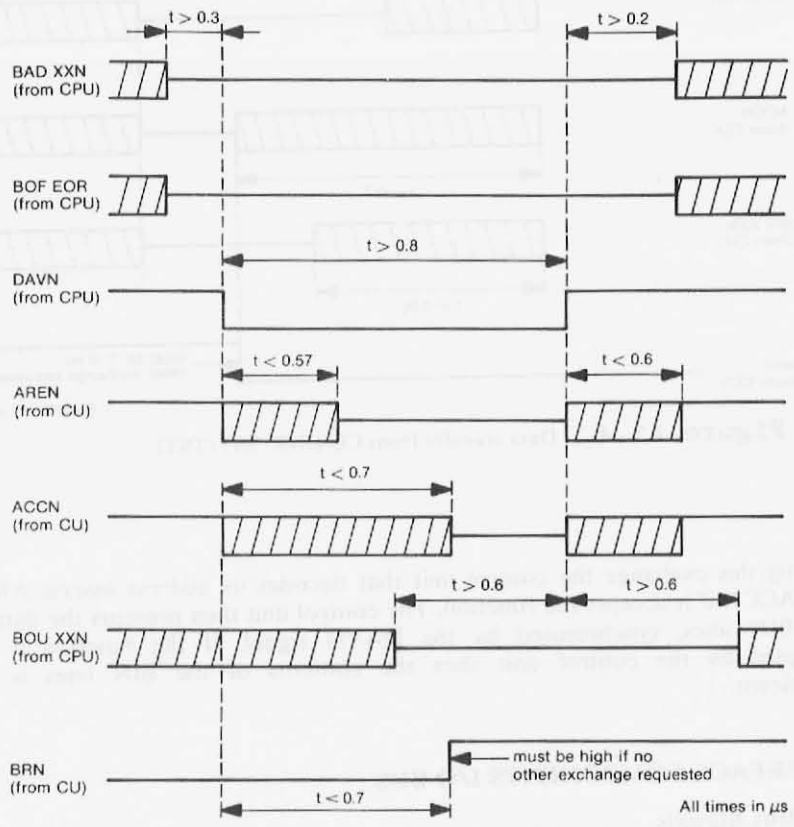


Figure A1.3 Data transfer to CU (OTR/CIO)

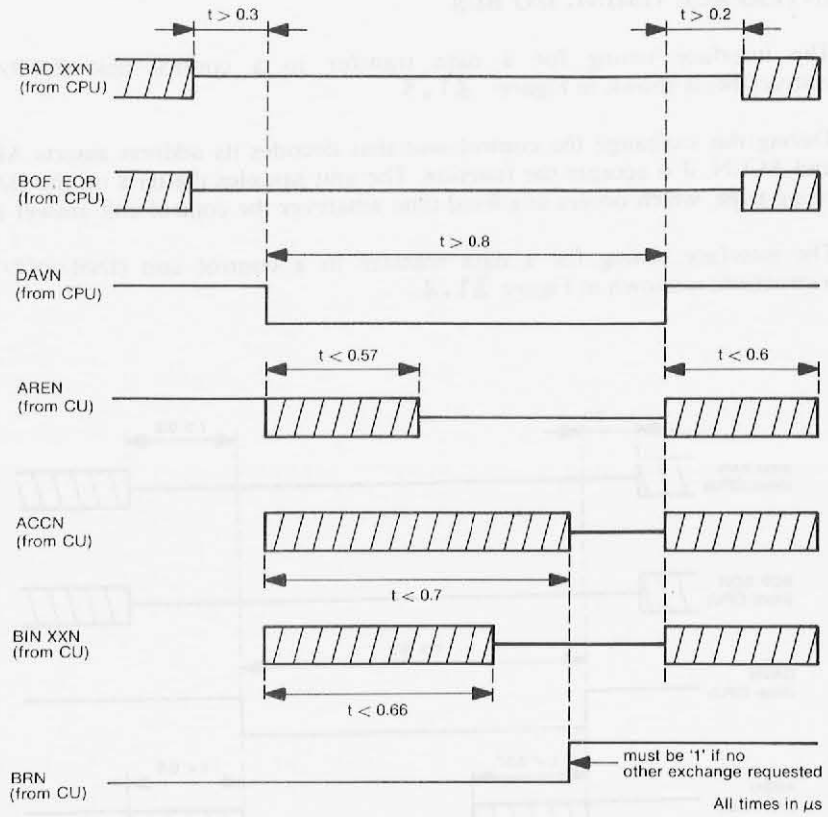


Figure A1.4. Data transfer from CU (INR/SST/TST)

During this exchange the control unit that decodes its address asserts AREN and ACCN if it accepts the function. The control unit then presents the data on the BIN lines, synchronised by the DAVN signal. If the function is not accepted by the control unit then the contents of the BIN lines is not significant.

INTERFACE COMPONENTS I/O BUS

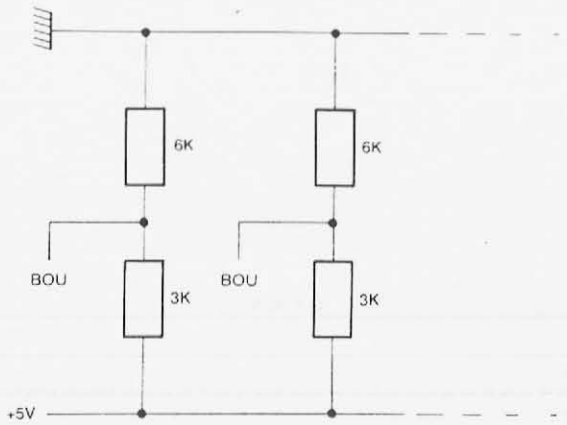
I/O Bus Signals

The I/O bus is designed to interface with standard TTL components operating at the following levels:

d.c. Supply	+5V ± 5%
Logic High Level	not less than +2.4V; typically above +3V
Logic Low Level	not greater than +0.4V; typically below +0.2V
One TTL Level	1.6 mA at +0.4V.

The control unit input for each of the BOU, BAD/, BOF/, DAV/, EOR/ and MC/ lines must present a fan in of one TTL load.

If only some of the BOU lines are used on a control unit board then the remaining ones must each be terminated on the board by either an inverter or by a 3K resistor connected to +5V and a 6K resistor connected to ground as shown:



Control unit outputs BIN/, ARE/ and ACC/ must each emanate from an open collector NAND gate.

Interrupt and Break Requests
PIL/ and BRL/ signals should be transmitted via one of the following circuits able to drive a matched long line up to 15 metres in length:

- An open collector NAND buffer (SN 7438) without resistor, if the signals are coupled by a wired OR to produce only a PIL/ interrupt for the programmed channel.
- A NAND buffer (SN 7437 or SN 7440).
- An inverter driver (SN 7416)
- A driver (SN 7417).

POWER CONTROL SYSTEM EXTENSION USING BUS TRANSLATOR BOARDS

The operation of the PWFN and RSLN signals for safeguarding the control units connected to the GP bus are described in Section 1, Part 2, Chapter 5. When using Type 2 control units connected via the Bus Translator boards power control signals are connected to extend the power protection system. The arrangement is shown in Figure A1.5.

In this arrangement signals PWFN and RSLN are connected to each bus translator board via the GP bus and signal PWFE1 (or PWFE2) from the Equipment shelf power supply is also connected in an "OR" function on the bus Translator board. The timing of the signals is shown in Figure A1.6

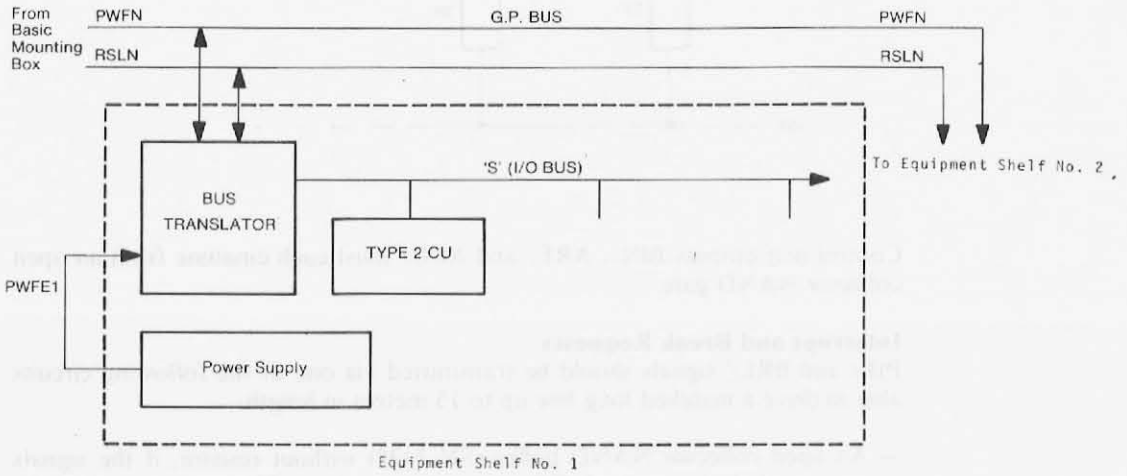


Figure A1.5 Power control system using bus translator boards

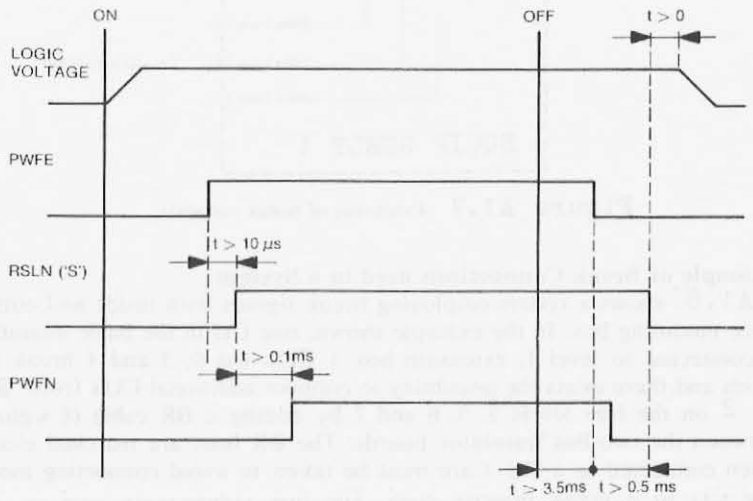


Figure A1.6 P852M/P856M/P857M power control timing

The timing of the signals is in accordance with I/O timing for switching off (due to the low energy reserve of the power supply) and with GP Bus timing for switching on (to obtain a correct master clear function in the P852M/P856M/P857M system).

Fan in:	PWFE	2TTL loads	
	PWFN	Receiver 1 REC0612	(see GP bus configuration rules)
Fan out:	PWFN	Emitter 1 1801	(see GP bus configuration rules)

Remark: RSLN(5): I sink 250 mA 15T2L
Loads max. for each Equipment shelf (7 Equipment shelves, in max. configuration).

BREAK CONNECTIONS ON BUS TRANSLATOR BOARD

A bus translator board receives one BR cable containing 8 signal lines to convey 8 break requests to the multiplex blocks in one I/O processor mounted in the basic mounting box. Figure A1.7 illustrates how the BR lines can either be connected to CU's in the shelf in which the Bus Translator board is situated (in this case the lines are electrically matched) or can be daisy-chained to the next shelf for extra CU connection or to be terminated if they are not to be used in the system. The matching resistors are provided on the Bus Translator boards and at the basic mounting box on the I/O processor board.

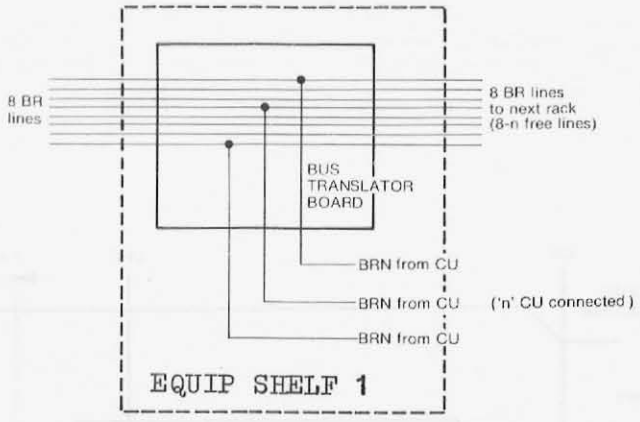


Figure A1.7 Extension of break requests

Example of Break Connections used in a System

Figure A1.8 shows a system employing break signals both inside and outside the basic mounting box. In the example shown, one CU in the basic mounting box is connected to level 1, extension box 1 CU's use 0, 3 and 4 break priority levels and there exists the possibility to connect additional CU's from 'Equipment shelf 2' on the free levels 2, 5, 6 and 7 by adding a BR cable (8 signal lines) between the two Bus Translator boards. The BR lines are matched electrically when connected to a CU. Care must be taken to avoid connecting more than one CU to a break priority level. The link connections used on the Bus Translator boards are illustrated in Figure A1.9.

SPARE LINES

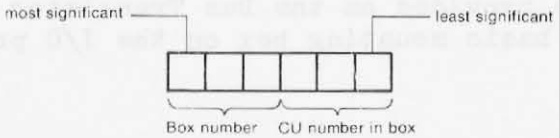
4 spare lines are provided on the GP bus and are accessible, via the Bus Translator board, on the I/O bus. The lines can be matched electrically on any Bus translator board and in this case they are not further daisy chained.

INTERRUPT SIGNAL ENCODING USING BUS TRANSLATOR BOARDS

The block diagram in Figure A1.10 shows a typical system arrangement using Type 2 control units. Extension boxes 1 to 7 are each given a 3-bit binary number from 001 to 111 which is coded by straps on the bus translator board interrupt encoding circuit and each of the 8 control units allocated to each rack is also identified by a 3-bit number which is coded by the interrupt encoder. The basic mounting box internal interrupts are coded in a similar manner; the interrupt encoder straps give the box number as 000.

Note: If all interrupt levels in one box are not employed then the numbering can be continued in the next box in the chain. In this manner two boxes may be identified with the same 3-bit binary number.

The box number and control unit number are combined so that each of the interrupts from 0 to 63 is identified by a single composite 6-bit number which has the following format:



The interrupt encoder logic ensures that both the box number and the control unit number are sampled in logical order of priority, the lowest number in each case having highest priority. When several signals are active therefore only the encoded signal for the interrupt with the highest priority appears on the 6 lines into the comparator.

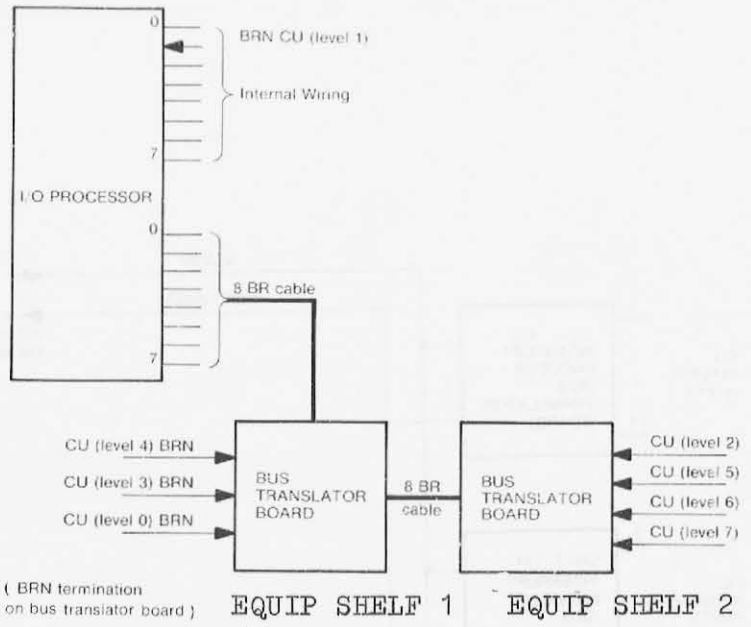
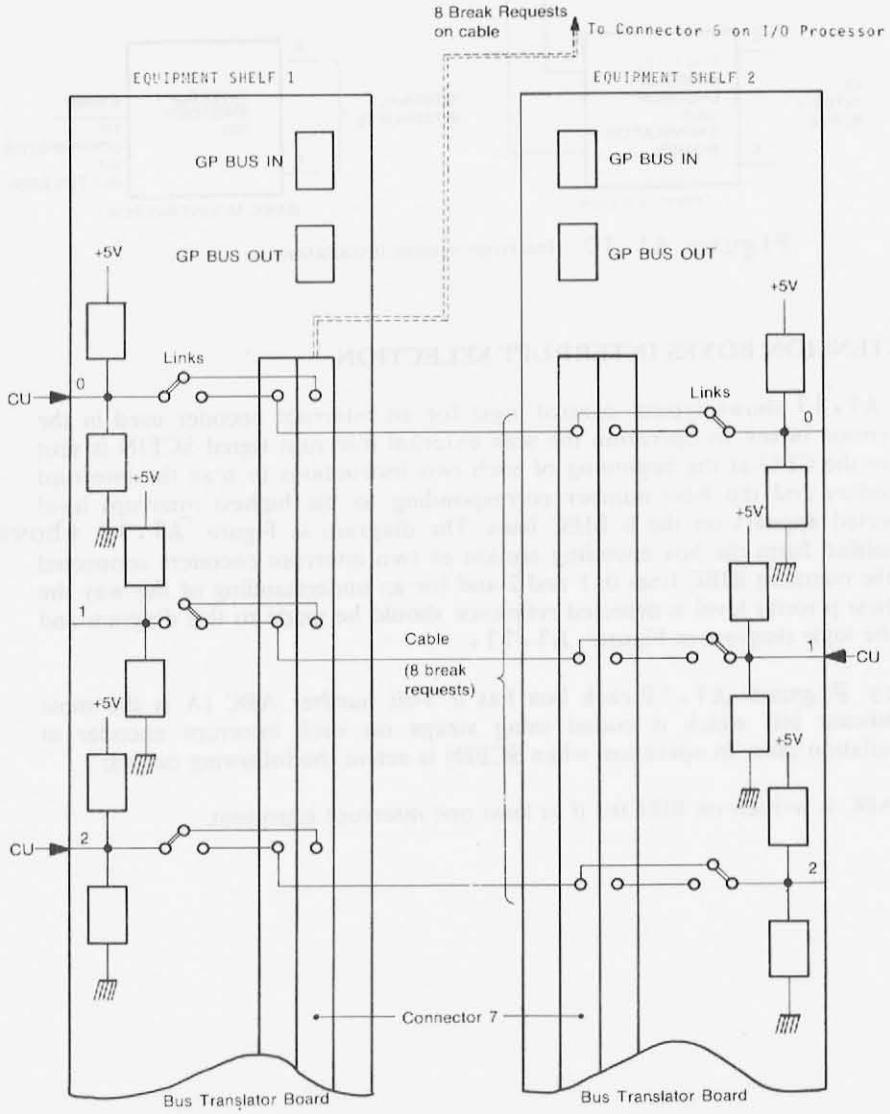


Figure A1.8 Break requests used in a system



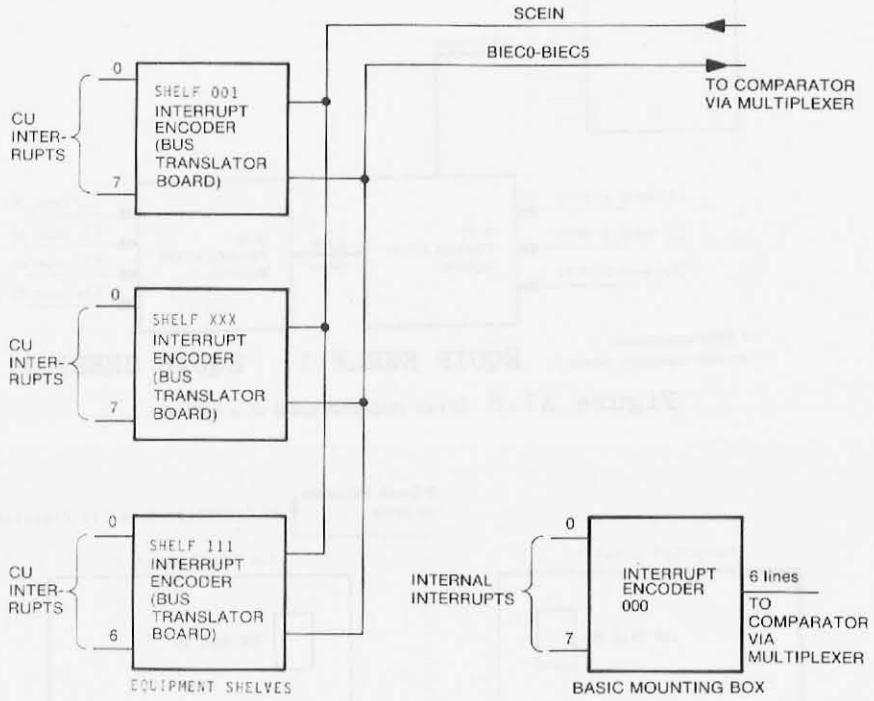


Figure A1.10 Interrupt system installation

EXTENSION BOXES INTERRUPT SELECTION

Figure A1.11 shows typical control logic for an interrupt encoder used in the extension boxes. In operation the scan external interrupt signal SCEIN is sent from the CPU at the beginning of each two instructions to scan the interrupt encoders and the 6-bit number corresponding to the highest interrupt level detected appears on the 6 BIEC lines. The diagram in Figure A1.12 shows in simplified form the box encoding section of two interrupt encoders connected to the common BIEC lines 0, 1 and 2 and for an understanding of the way the highest priority level is detected reference should be made to this diagram and to the logic diagram in Figure A1.11.

Referring to Figure A1.12 each box has a 3-bit number ABC (A is the most significant bit) which is coded using straps on each interrupt encoder at installation time. In operation when SCEIN is active the following occurs:

1. ABC is written on BIEC0-2 if at least one interrupt is present.

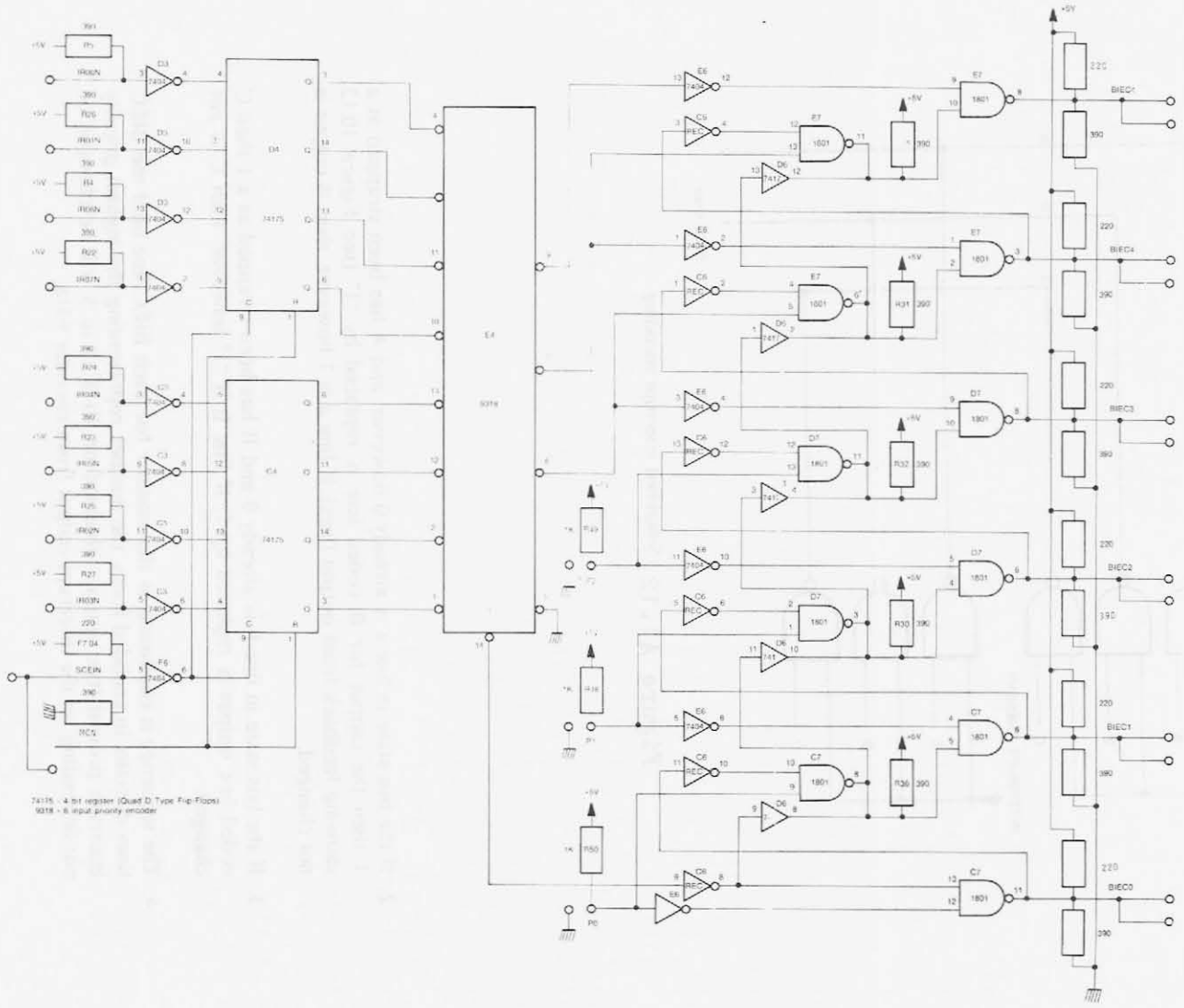


Figure A1.11 Interrupt encoding logic- bus translator

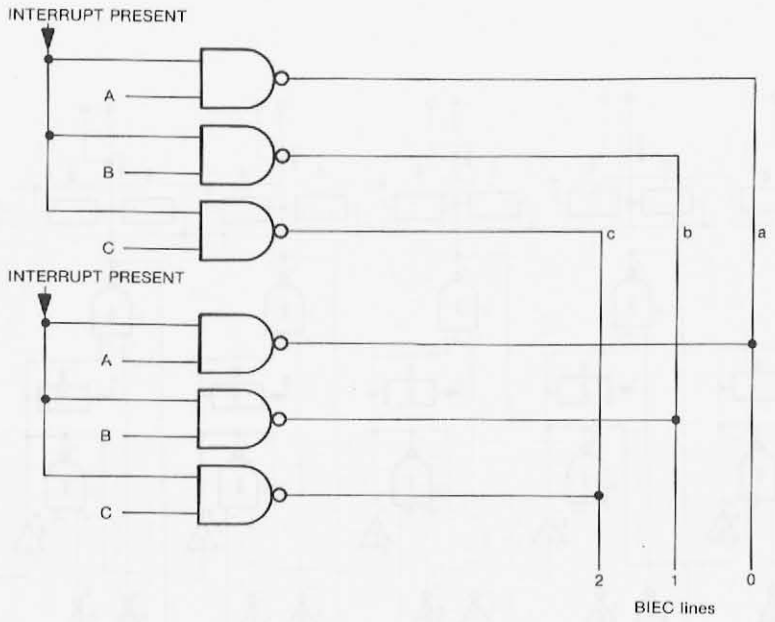


Figure A1.12 Simplified interrupt encoding

2. If the bus state in line a is already 0 however, and A has been strapped as a 1 then the output for B coded line is replaced by "1" (see Figure 10.12 showing feedback from output lines). If line a is 1 however, then B output is not changed.

3. If the bus state in line b is already 0 and B has been strapped as a 1 then C coded line output is replaced by 1. If line b is "1" however, then C is not changed.

4. The sequence is continued in this manner for each BIEC line until the BIEC lines contain, in encoded form, the number representing the highest priority interrupt present (the outputs obtained on BIEC 3 to 5 will be changed or not depending on the interrupt output from encoder 9318.

TIMING OF SCEIN SIGNAL

The diagram in Figure A1.13 shows the BIEC line signals in relationship to SCEIN. The BIEC lines are required to be stabilized within 1800 ns after SCEIN.

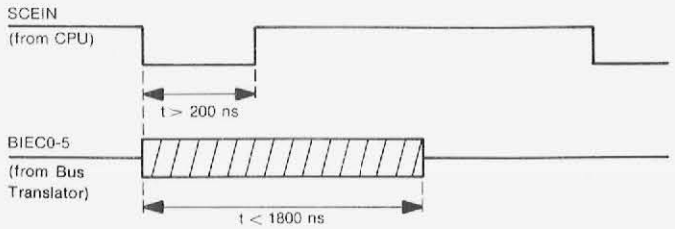


Figure A1.13 Signal SCEIN timing

When using a DIOS system which is constructed on small format boards(Type2) it is necessary to use equipment shelf P843-002 or P843-003 which incorporates a bus translator board P843-007 or 008 respectively to translate signals from the I/O bus to the GP bus. The following small format boards are available.

Control Boards

P839-050 (DIOC)	Digital input output control unit for 2 gated 16-bit input words and 2 buffered output words for programmed channel connection.
P839-150 (DIC)	Digital input control unit for 4 gated 16-bit input words for programmed channel connection.
P839-250 (DOC)	Digital output control unit for 4 buffered 16-bit output words for programmed channel connection.

Input Option Boards for DIOC,DOC,and DIC.

Note: These boards includd cable and connectors for connection to the control board.

P839-001	Input buffer board for 2 words,16-bits each.
P839-002	Input adaptor board for 2 words,16-bits each. Low threshold 1.5V. Input voltage level adaption. Max. voltage rating ± 48V.
P839-003	Input adaptor board for 2 words,16-bits each. High threshold 5.9V.Input voltage level adaption. Max voltage rating ± 48V.
P839-004 (IIS)	Input isolator board for 2 words,16-bits each. Can be used with input buffer and input change of state detector options.
P839-005	Input buffer and change of state detector board for 2 words,16-bits each.

P839-006 Input buffer and adaptor board for 2 words 16-bits each, Low threshold 1.5V.

P839-007 Input buffer and adaptor board for 2 words 16-bits each. High threshold 5.9V.

P839-008 Input buffer,change of state detector and adaptor board for 2 words,16-bits each. Low threshold 1.5V.

P839-009 Input buffer,change of state detector and adaptor board for 2 words,16-bits each. High threshold 5.9V.

Output Option Boards for DIOC,DOC,and DIC.

P839-010 Output level adaption board for 2 words 16-bits each. No isolation. Low threshold 1.5V.

P839-011 (OIS) Output isolator and level adjustment board for 2 words,16-bits each

P839-012 Output level adaption board for 2 words 16-bits each. No isolation. High threshold 5.9V.

Physical Construction

The small format boards have the dimensions as shown in Figure A2.1. Note also that the Bus Translator is constructed on a similar board.

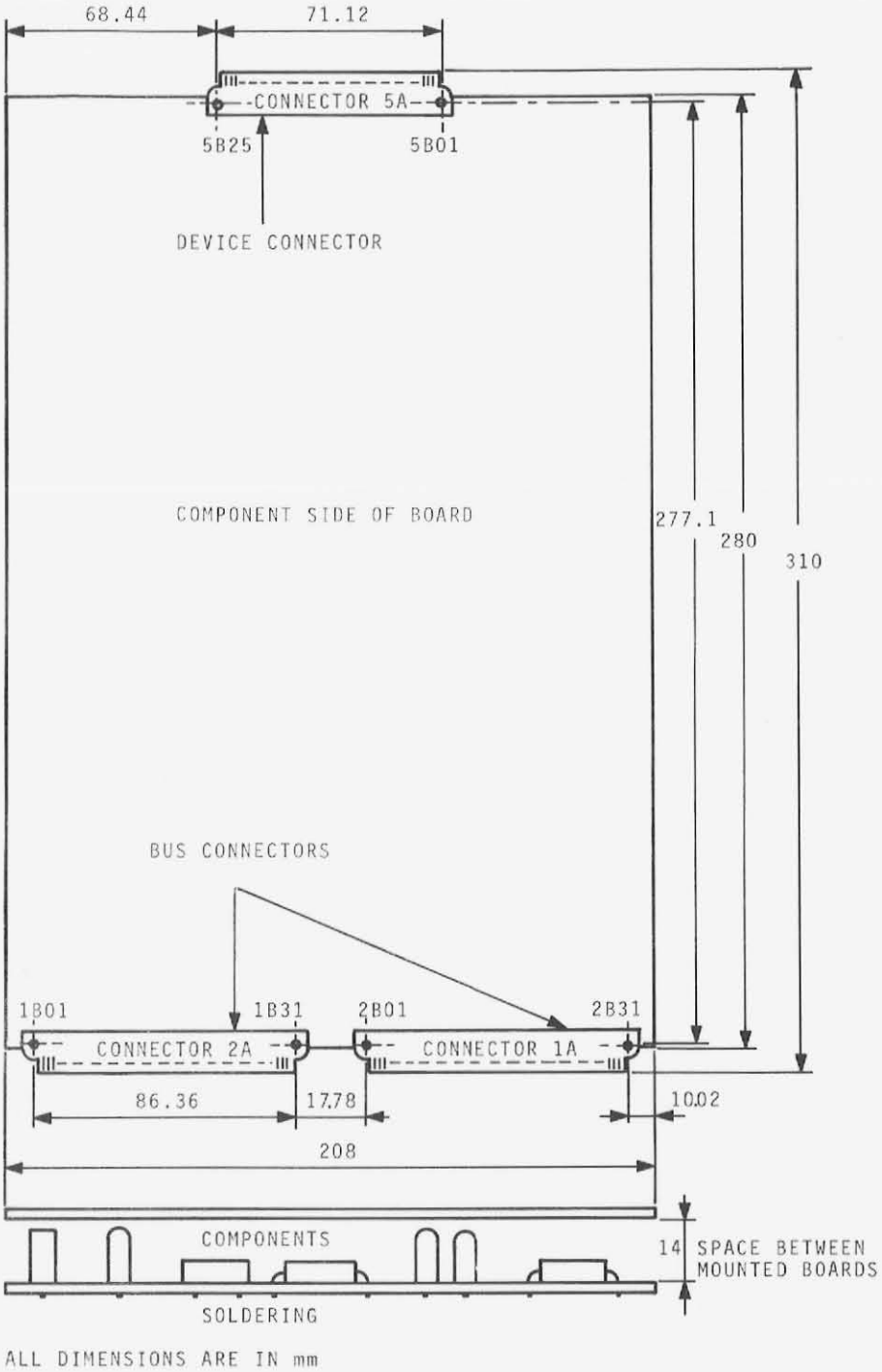


Figure A2.1. Dimensions of Small Format Board.

Appendix 3 Example Control Unit

On the following page is the logic diagram of the standard control unit (mounted on MCU'3 board) for a V24 Serial controller. The diagram shows how the decoding, sequencing and control flip-flops circuits dicussed in Section 1, Part 2, Chapter 3 have been incorporated.

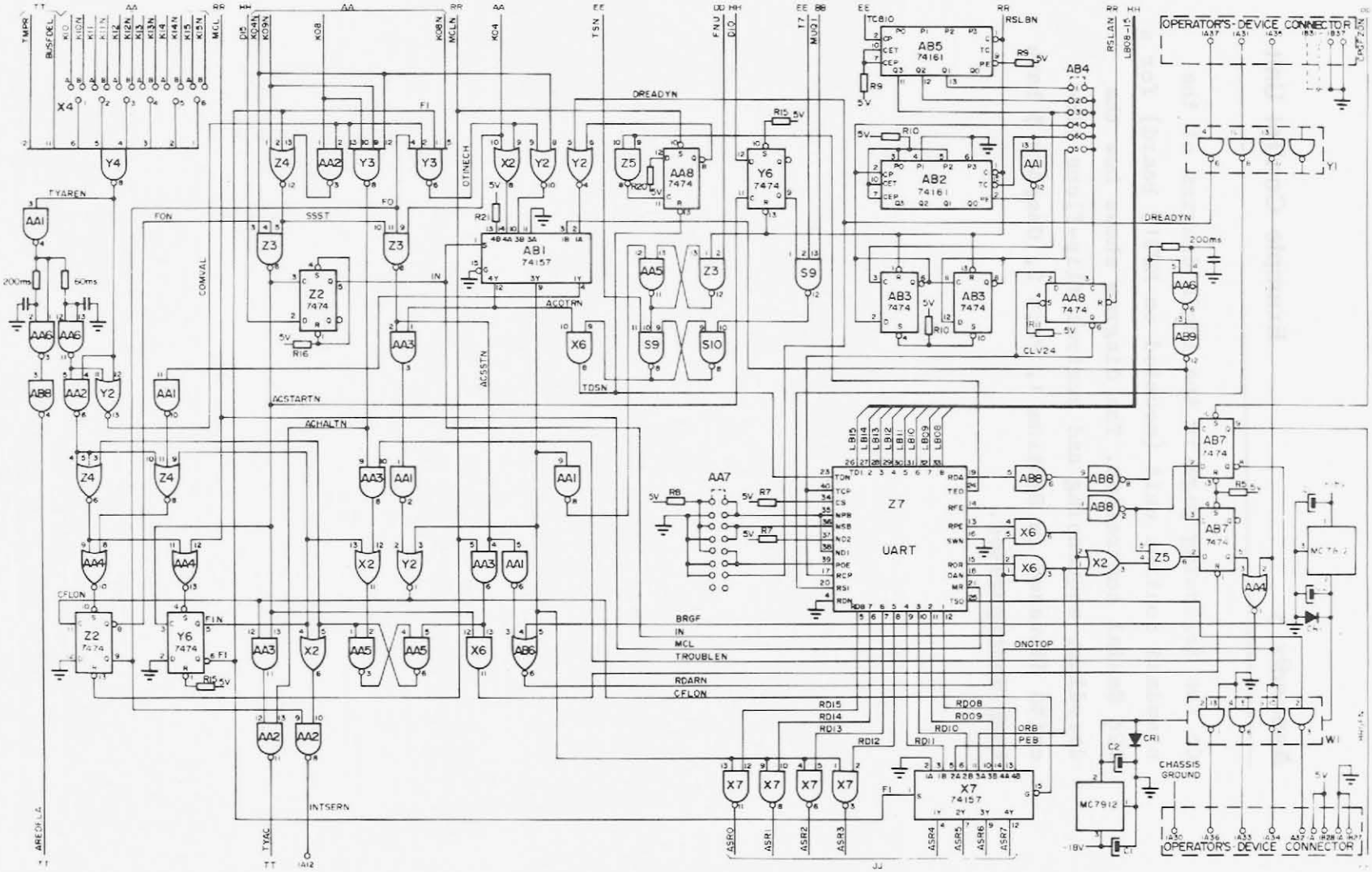


Figure A3.1 V24 serial controller-logic

Appendix 4 Printed Wiring Board (Motherboard)

On the following page is given an outline drawing for the printed wiring board (motherboard) into which the circuit boards mounted in the basic mounting box are plugged. The drawing shown is for the motherboard used in a Type M2 basic mounting box.

The backpanel P852M-801 is a sub assembly which includes:
- a frame with mechanical holders
- a printed circuit with the connection facility to carry the GP bus to external racks and the connection for:
  1. Six HE 901 connectors 2 x 43 pins (pitch 0.55 inch)
  2. Two connectors HE 901 2 x 37 pins, one each side of the CPU board connector 3. One connector (connector 5) is for the control panel signals and the other (connector 1) is for the ASR33 and the interrupt signals.
  3. On each side of the four lower connectors is a cutting to receive four HE 901 2 x 37 pins connectors or eight 2 x 13 pins connectors with an adaptor.

Pin connection details are given on the drawing for the control panel signals and for the ASR33 and interrupt signals to the CPU board. Further pin connection details not shown on the drawing will be found in Section 1, Part 2, Chapter 2 of this manual.

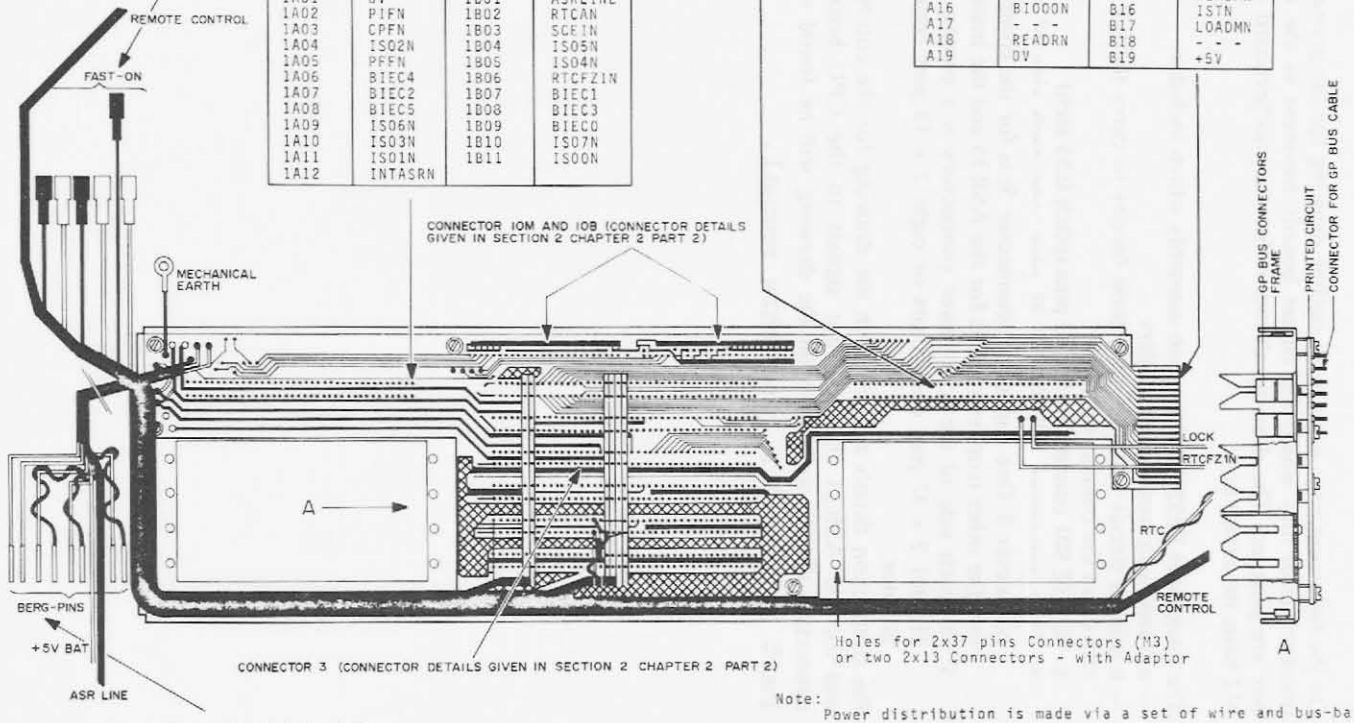
Fast-on Connector Colour Code

Colour	Signal Carried	Pin Connected to	
Green	+5V	3A19	3B19
		3A20	3B20
Yellow	+16V	3A06	3B06
			3B25
Blue	-5V		3B18
Red	+Bat		3B23
Black	0V	3A21	3B21
		3A22	3B22
		3A07	3B07
			3B24

Pin No	Signal	Pin No	Signal
5A29	BIOEKEY	5B29	CPMCN
5A30	UNLOCKN	5B30	IPL
5A31	RUNN	5B31	START
5A32	RCPOON	5B32	CPINT
5A33	LOADRN	5B33	RUNFA
5A34	READSTN	5B34	RCPO1N
5A35	RCPO3N	5B35	RCPO2N
5A36	LOADMN	5B36	READMN
5A37	READRN	5B37	INSTN

Pin No	Signal	Pin No	Signal
A01	BIO15N	B01	CPMCN
A02	BIO14N	B02	BIOEKEY
A03	BIO13N	B03	IPL
A04	BIO12N	B04	UNLOCKN
A05	BIO11N	B05	START
A06	BIO10N	B06	RUNN
A07	BIO09N	B07	CPINT
A08	BIO08N	B08	RCPOON
A09	BIO07N	B09	RUNFA
A10	BIO06N	B10	LOADRN
A11	BIO05N	B11	RCPO1N
A12	BIO04N	B12	READSTN
A13	BIO03N	B13	RCPO2N
A14	BIO02N	B14	RCPO3N
A15	BIO01N	B15	READMN
A16	BIOOON	B16	ISTN
A17	- - -	B17	LOADMN
A18	READRN	B18	- - -
A19	0V	B19	+5V

Pin No	Signal	Pin No	Signal
1A01	0V	1B01	ASRLINE
1A02	PIFN	1B02	RTCAN
1A03	CPFN	1B03	SCFIN
1A04	ISO2N	1B04	ISO5N
1A05	PFFN	1B05	ISO4N
1A06	BIEC4	1B06	RTCFZIN
1A07	BIEC2	1B07	BIEC1
1A08	BIEC5	1B08	BIEC3
1A09	ISO6N	1B09	BIECO
1A10	ISO3N	1B10	ISO7N
1A11	ISO1N	1B11	ISOON
1A12	INTASRN		



Berg-Pins Colour Code

Colour	Signal Carried	Pin Connected to
Yellow	PWFN	3A17
Blue	RSLN	3B17
Orange	RTC	
Red	-18V	3B01
Brown	+18V	3A01

Note:
Power distribution is made via a set of wire and bus-bars
+5V 20A for logic
-5V 1A and 16V 5A for Philips memories
+18V 2A and -18V 2A for Philips Control Unit

Figure A4.1 Printed wiring board (Motherboard)

Cetain I/O Cards might be delivered separately packed and therefore, to aid in identification, the following list is given containing the 12-digit part numbers with which they are marked; the last digit is shown as an 'X' because it varies with the card issue level. The cards of self-contained control units are not included.

Peripheral CU	Type Number	Part Number
Punched Tape Reader	P801-040	5111 199 7746X
Line Printer	P810-040	5111 199 7747X
Display (V24/V28 Interface)	P845-040	5111 199 7744X
DISC Units M.H. (X2)	P824-040	5111 199 7817X
Punched Tape Reader and Tape Punch	P840-001	5111 199 7745X
Punched Tape Reader, Tape Punch and V24 devices	P840-002	5111 199 7819X
Line Printer and Card Reader	P840-003	5111 199 7818X
Data Communication		
Multiple Line Control Unit SLCU2S	P847-060	5111 199 7611X
Multiple Line Control Unit SLCU 4	P847-070	5111 199 7610X
Multiple Line Control Unit ALCU 4	P846-070	5111 199 7609X
Multiple Line Control Unit ALCU 2	P846-060	5111 199 7514X
Medium Speed Line Multiplexer AMA8A	P845-060	5111 199 7531X
Medium Speed Line Multiplexer AMA8C	P845-070	5111 199 7609X
Low Speed Line Multiplexer AMA16	P844-060	5111 199 7508X
Control Module 64 lines V28CM	P844-110	5111 199 7507X
DIOS		
DIOD (1W)	P837-001	5111 199 7682X
DIOD (2W)	P837-002	5111 199 7740X

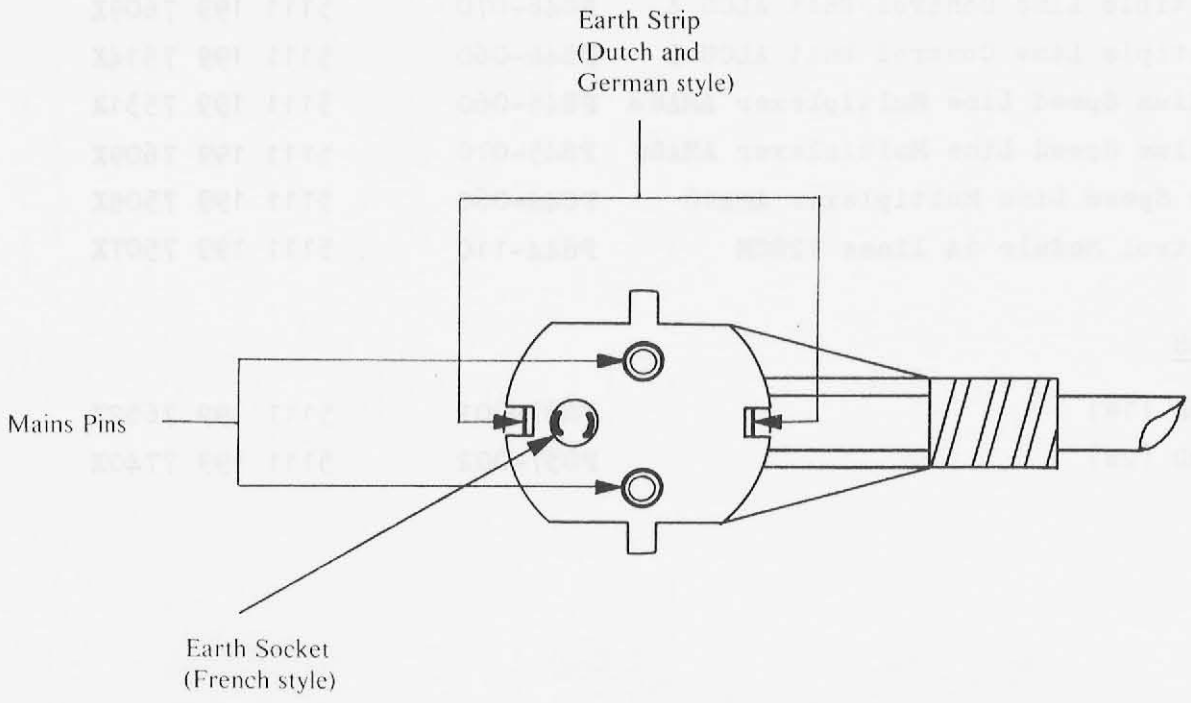
Shown below is a sketch of the versatile power plug with which the power cables are normally terminated; the plug fits most European types of single phase outlet socket.

Shielded Cables

Core size AWG 13-gauge - cross section 1.91 mm^2

Green/Yellow		Earth
Blue (neutral)	}	Mains
Black (line)	}	

General European Plug



The following pages provide an example of the Configuration Sheets which accompany the equipment when it is delivered.

The first page is merely an invoicing sheet.

Next are parts lists specifying the major items in the system, including I/O cards and logic options, together with the 12 digit part numbers.

The parts lists are followed by drawings showing the I/O and logic card locations, rack configuration and connections for the equipment.

The set concludes with sheets giving wiring interconnection and signal cable details.

CPD-OPM 11/75 FACTORY ORDER DATE 16/10/75 PAGE 1 OF 6 ORDER NUMBER: 03446-01

27 OCT 1975

TYPE: PA56M 6045

C. T. I.
12 NOV 1975

NER: ELKEM SPIGERVERKET A/S.
P.O. BOX 82.
3901 PORSGRUNN.
NORWAY.

FRY ADDRESS: APELDOORN

CE ADDRESS: APELDOORN

MER REFERENCE: 5132 DATED: 75/10/03

FRY DATES:	PHASE 1	REQUESTED 550	CONFIRMED 549	12NC OF PHASE: 5111 150 37210
	Phase II		612	

KS:

IBUTION:	MR. M. DELAVALLEE. RAMBOUILLET.		AUTHORIZED BY R. VAN DRIE	J. GAMBART 28/10/75 4

SUPERSEDES FO-NR: PHILIPS-ELECTROLOGICA APELDOORN DEPT: P.P.S.C.

SPECIMEN

A-32

QUANTITIES PER INSTALLATION PHASE					MOD QTY	LOT ORD QTY	COMMERCIAL TYPE NUMBER:	CORRESPONDING MASTER NUMBER DESCRIPTION :	12NC NUMBER:	REMARKS:
P80	P81	P82	P83	P84						
	1					1	P856 M403	P856 M400	5III I99 74950	
								Telescopic slides	5III I99 749I0	
								Identification label	5III I00 II602	
								Remote Cont. cable 3m	5III I99 77490	
								~~MEMORY MODULE 8K I,2us~~	~~43II 027 7306I~~	
								Configuration label	5III I00 23220	
								MEMORY MODULE I6K I,2u	5III I99 76240	
								~~MEMORY MODULE I6K 0,7u~~	~~5III I99 74900~~	
							P856 MI0_	P856 MI00	5III I99 74960	
								Telescopic slides	5III I99 79360	
								Identification label	5III I00 II602	
								Remote Cont. cable 3m	5III I99 77490	
								MEMORY MODULE 8K I,2us	43II 027 7306I	
								Configuration label	5III I00 23210	
								MEMORY MODULE I6K I,2u	5III I99 76240	
								MEMORY MODULE I6K 0,7u	5III I99 74900	
							P85_ M008	MEMORY MODULE 8K I,2us	43II 027 73060	
							P85_ MOI6	MEMORY MODULE I6K I,2u	5III I99 76240	
								or	4322 027 69690	
		1				1	P856 MOI6	MEMORY MODULE 16K 0,7u	5III I99 74900	
							P85_ M020	Multiplex card	5III I99 79330	
								Standard cable breaks3	5III I99 79630	
								Connector holder	5III I00 I954I	
								Connector 2xI3 pins	24II 029 II20I	
								Screw CM3xI0 4x	2522 002 4I099	
								Packing	5III I99 78220	
								Strap 8x	5III I99 884I0	

QUANTITIES PER INSTALLATION PHASE					MOD QTY	LST CRD QTY	COMMERCIAL TYPE NUMBER:	CORRESPONDING MASTER NUMBER DESCRIPTION :	12NC NUMBER:	ORDER NUMBER: P3446 01 REMARKS:	Mask NO:
PHO	PH1	PH2	PH3	PH4							
							P 849 010	RACK EXTENSION 4 CARTES EMBALLAGE KIT FIXATION CABLES	5111 199 82260 5111 199 82730 5111 199 79960		
							P 849 011	RACK EXTENSION 22 CARTES NON CABLE EMBALLAGE KIT FIXATION CABLES	5111 199 82690 5111 199 82720 5111 199 79940		
							P 849 013	RACK EXTENSION 22 CARTES EMBALLAGE KIT FIXATION CABLES	5111 199 84840 5111 199 82720 5111 199 79240		
							P 849 018	RACK EXTENSION 11 CARTES EMBALLAGE KIT FIXATION CABLES	5111 199 82780 5111 199 82720 5111 199 79950		
							P 849 019	RACK ALIMENTATION MODULAIRE EMBALLAGE	5111 199 84860 5111 199 82730		
							P 849 016	CABINET 36 U - 19 POUCES EMBALLAGE	5111 199 83040 5111 199 81240		
							P 849 116	CABINET EXTENSION 36 U - 19 POUCES EMBALLAGE	5111 199 83030 5111 199 81240		
	1					1	P 849 017 /	CABINET 36 U - 19 POUCES EQUITE EMBALLAGE KIT BASIC SPARE PARTS GLISSIERES TELESCOPIQUES	5111 199 81610 5111 199 81240 5111 199 81130 5111 199 82980		
							P 849 117	CABINET EXTENSION 36U - 19 POUCES EMBALLAGE KIT BASIC SPARE PARTS	5111 199 81620 5111 199 81240 5111 199 81130		
							P 849 040	ENSEMBLE 2 VENTILATEURS	5111 199 82850		
							P 849 041	ENSEMBLE 4 VENTILATEURS	5111 199 82860		
							P 849 042	POWER DISTRIBUTION PANEL 10A KIT BASIC SPARE PARTS	5111 199 83000 5111 199 81170		
							P 849 043	POWER DISTRIBUTION PANEL 25A KIT BASIC SPARE PARTS	5111 199 83010 5111 199 81170		
							P 849 044	GLISSIERES TELESCOPIQUES ADAPTATION	5111 199 82980		
							P 849 045	GLISSIERES TELESCOPIQUES POUR PHD	5111 199 82990		
	2					2	P 849 046 /	PANNEAU 1 U	5111 199 82870		
	1					1	P 849 047 /	PANNEAU 3 U	5111 199 85260		
	1					1	P 849 048 /	PANNEAU 5 U	5111 199 85250		
							P 849 049	PANNEAU 7 U	5111 199 85240		
							P 849 002	GENERAL PURPOSE CARD	5111 199 85800		
							P 849 005	CONNECTEUR MALE (PERIPHERIQUE)	2411 029 11032		
							P 849 006	CONNECTEUR FEMELLE EQUIPE	5111 199 81220		
							P 849 012	GENERAL PURPOSE CARD INTERFACE	5111 199 82080		
							P 849 035	CONNECTEUR MALE(COTE I/O BUS)	2411 029 11033		
							P 849 036	CONNECTEUR FEMELLE FCR IIS	2411 029 11024		
							P 849 015	I/O EXTENDER; INCLUS CABLES 5M	5111 199 82570		
							P 849 115	I/O EXTENDER AVEC CARTE INTER INCL CABLES DE 5M	5111 199 81210		
							P 849 215	CABLES ET BORNIERS POUR LESS SIGNAUX	5111 199 80130		
							P 849 315	I/O EXTENDER INCLUS CABLE 5M(P850)	5111 199 79450		
							P 849 031	I/O EXTENDER DMA INCL CABLES 5M	5111 199 81690		
							P 849 003	PROLONGATEUR DOUBLE	5111 199 82680		
							P 849 004	PROLONGATEUR SIMPLE	5111 199 80690		
							P 849 050 /	CONTROL PANEL PORTATIF POUR P850 M	5111 199 80030		
							P 849 055	CONTROL PANEL PORTATIF POUR P850M	5111 199 79390		

QUANTITIES PER INSTALLATION PHASE					MOD QTY	LST CRD QTY	COMMERCIAL TYPE NUMBER:	CORRESPONDING MASTER NUMBER DESCRIPTION :	12NC NUMBER:	ORDER NUMBER: 3446 01 REMARKS:	MAST NO:
	PH1	PH2	PH3	PH4							
							P 852M 016	Memory module 16K	8222 297 0793		
								Packing	5111 199 7822		
	1					1	P 843M 020	Multiplex card	5111 199 7933		
								Cable for break	5111 199 7963		
								Connector holder	5111 100 1954		
								Connector 2 x 13 pins	2411 029 1120		
								Screw CM 3 x 10	2522 002 41099		
								Packing	5111 199 7822	x if extension	
	1					1	P 843M 032	Integrated circuit 1821	5111 010 0182		
								Female plug F088	2422 024 88003		
							P 852M 030	Mini panel	5111 199 7577		
								Control panel	5111 199 8145		
							P 849 052	Portable control panel	5111 199 7757		
							P 843 025	General purpose card	5111 199 7938		
								Packing	5111 199 7822		
							P 843 026	C P Card with hole pattern	5111 199 8251		
								Packing	5111 199 7822		
							P 843 021	Female connector 74 pins	2411 029 11024		
								2 x Screw CM 3 x 10	2522 002 41099		
								2 x Washer Z3 U	2511 618 37003		
							P 843 022	Female connector 26 pins	2411 029 11204		
								Connector holder	5111 100 19541		
								4 x Screw CM 3 x 10	2522 002 41099		
								4 x Washer Z3U	2511 618 37003		
							P 843 027	10 x Circuit integré NEC 0612	5111 010 00612		
								10 x Circuit integré 1801	5111 010 01801		
							P 843 035	Extender board	5111 199 7802		
								Packing			
							P 843 135	Extender board	5111 199 7801		
								Card ADAP	5111 199 7793		
	1					1	P 824 040	Control unit	5111 199 7817		
								Strap	5111 199 8841		
								Packing	5111 199 7822	x if extension	
							P 824 001	Disc x 1215.001	5111 199 7748		
	1					1	P 824 002	Disc x 1215.002	5111 199 7991		
	1					1	P 824 100	Cartridge for X 1235	5122 021 0225		
	1										
	1					1	P 833 001	Cassette type EIA	5111 199 0043		

QUANTITIES PER INSTALLATION PHASE					ORD QTY	LST ORD QTY	COMMERCIAL TYPE NUMBER:	CORRESPONDING MASTER NUMBER DESCRIPTION :	12NC NUMBER:	ORDER NO: Ø 3446 01 REMARKS:	TASK NO:
PH0	PH1	PH2	PH3	PH4							
							P 840 003	Control unit LP. CR 2 Straps MCU 2 Packing	5111 199 7810 5111 199 8041 5111 199 7822	if extension	
							P 006 101	Card Reader M200	5111 199 8010		
	1					1	P 810 040 /	Control unit LP Strap Packing	5111 199 7747 5111 199 8041 5111 199 7822	if extension	
	1					1	P 809 002 /	Line printer x 1415	5111 199 7658		
							P 810 001	Line printer DP 2310	5111 199 8568		
							P 811 001	Line printer DP 2420	5111 199 8569		
							P 812 001	Line printer DP 2440	5111 199 8430		
							P 801 040	Control unit PTR Strap Packing	5111 199 7746 5111 199 8041 5111 199 7822	if extension	
	1					1	P 840 001 /	Control unit PTR PTP 2 Strap MCRP Packing	5111 199 7745 5111 199 8041 5111 199 7822	if extension	
							P 840 002	Control unit PTR PTP V24 3 Straps Packing MCU 3	5111 199 7819 5111 199 8041 5111 199 7822	if extension	
	1					1	P 801 001 /	PTR 333	5111 199 8434		
							P 802 001	PTR 600	5111 199 8435		
	1					1	P 803 001 /	PTP 75	5111 199 8432		
							P 804 001	PTP 150	5111 199 8431		
							P 818 040	Control unit V 24 Strap Packing	5111 199 7744 5111 199 8041 5111 199 7822	if extension	
							P 841 001	ASR 33.	5111 199 8330		
							P 841 002	ASR 35	5111 199 8329		
							P 841 003	KSR 33	5111 199 9827		
							P 841 004	KSR 35	5111 199 9826		
	1					1	P 842 001 /	Character printer (V 24)	5111 199 7947		
							P 842 002 /	Character printer (TTY)	5111 199 7795		
							P 837 001	DIOD 1W	5111 199 7682		
	1					1	P 837 002 /	DIOD 2W	5111 199 7740		
							P 843 010	Stabilizer RG 1 Rectifier RD 1 Packing for RD 1 Packing for RG 1	51111199 8716 5111 199 6511 5111 199 8129 5111 199 7822		

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