Signetics

8X330
Floppy Disk Formatter/ Controller

Product Specification

Microprocessor Products

DESCRIPTION

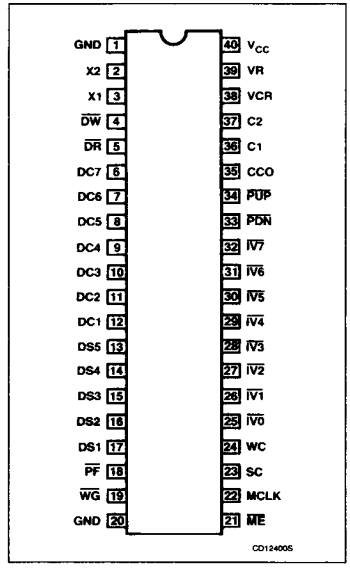
The Signetics 8X330 Floppy Disk Formatter/Controller is a monolithic peripheral device of the 8X300 Family. The chip uses Bipolar-Schottky/1^2L-Technology and some very unique features to provide 8X330 customers with a competitive edge in both simple and complicated disk-controller designs. The competitive advantage is measurable in terms of "systems parts count", "error correction capabilities", and "overall design concepts" that are applications oriented. Except for the following, the 8X330 contains all processing circuits and the required control logic to encode/decode double-density (MFM/M^2FM) and single-density (FM) codes: a crystal; a capacitor; an external transistor acting as a series-pass element for the on-chip voltage regulator; an active low-pass filter; and an optional off chip voltage controlled oscillator (refer to Features and Option). Data-separation and write-precompensation logic are located on the chip, while 16-bytes of scratch-pad RAM are provided for storage of various control/status parameters.

FEATURES

- **Single or double density encoding/decoding**
- **On-chip data separator**
- **Programmable:**
  - **FM, MFM, and M^2FM encoding/decoding**
  - **Preamble Polarity**
  - **Data transfer rate**
  - **Address mark encoding/decoding**
  - **Sector length**
  - **Output port (7-bits disk command)**
  - **Input port (5-bits disk status)**
- **Write Precompensation with on/off control**
- **On-chip phase lock loop**
- **CRC generator with software-controlled error correction capabilities**
- **40-pin package**
- **+5V operation**

OPTION: External Voltage Controlled Oscillator (VCO). For critical applications, window margins can be improved by as much as 6% with the use of an external VCO.

PIN CONFIGURATION



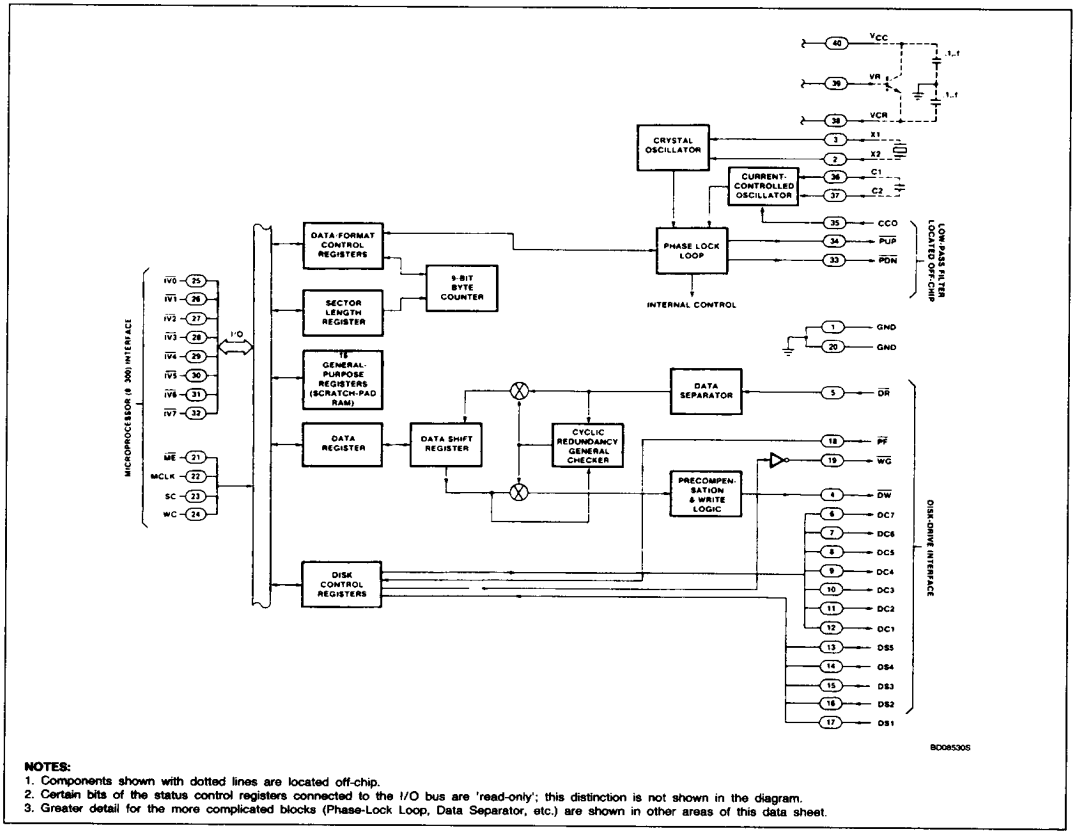
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
40-Pin plastic DIP	N8X330

PIN DESCRIPTION

PIN NO	MNEMONIC	DEFINITION	FUNCTION
1, 20	GND	Ground	Circuit ground
2, 3	X1, X2	Crystal inputs	Inputs from a crystal that determines frequency of an on-chip crystal oscillator.
4	$\overline{DW}$	Data write	A series of negative-going pulses transmitted to the disk drive. The data write signal produces pulses (with precompensation, if required) for data and clock in accordance with the applicable encoding rules (FM, MFM or M^{2}FM).
5	$\overline{DR}$	Data read	Negative-going pulses transmitted from the disk drive to a Schmitt-trigger input of the 8X330; these pulses represent encoded data and clock from the disk media.
6 – 12	DC1 – DC7	Disk commands	Seven outputs from the 8X330 that allow general-purpose control, of one or more disk drives.
13 – 17	DS1 – DS5	Disk status	Five general-purpose Schmitt-trigger inputs from the disk drive (or drives) that provide status information for the 8X300.
18	$\overline{PF}$	Power fail	Schmitt-trigger input from external logic that is active (low) when the "user-sensed" power supply voltage drops below a predetermined value.
19	$\overline{WG}$	Write gate	When active (low), this 40mA open-collector output enables writing to the disk media. When $\overline{PF}$ is low, the write gate is inhibited during periods of power supply uncertainty.
21	$\overline{ME}$	Master enable	When this input signal is active (low), the 8X330 can be accessed and enabled by the 8X300. (Refer to the $\overline{LB}$ and $\overline{RB}$ pinout discriptions of the 8X300 for further detail.)
22	MCLK	Master clock	When active high and with $\overline{ME}$ in the active-low state, this input signal provides a means whereby the I/O output from the 8X300 is interpreted as an enabling address (provided there is an address match) or as input data (if one of the 8X330 registers has already been selected).
23	SC	Select command	When this signal is active (high), the information output on pins $\overline{IV0} - \overline{IV7}$ of the 8X300 is interpreted as an address input by the 8X330.
24	WC	Write command	When this signal is active (high), the information output on pins $\overline{IV0} - \overline{IV7}$ of the 8X300 is interpreted as input data by the 8X330.
25 – 32	$\overline{IV0} - \overline{IV7}$	Input/output lines	Eight 3-State input/output lines that provide bidirectional data transfers between the 8X300 and the enabled I/O device; $\overline{IV7}$ is the *Least Significant Bit.*
33	$\overline{PDN}$	Pump down output	Open-collector output of on-chip phase detector which indicates (by a negative-going, quantized, pulse-width modulated signal) that internal CCO frequency is too high.
34	$\overline{PUP}$	Pump up output	Open-collector output of on-chip phase detector which indicates (by a negative-going, quantized, pulse-width modulated signal) that internal CCO frequency is too low.
35	CCO	Frequency Control Input for Current-Controlled Oscillator	Variable input current from external low-pass filter that controls the frequency of the oscillator.
36 – 37	C1, C2	Capacitor input terminals	Inputs for capacitor that determines center frequency of the current-controlled oscillator.
38	VCR	Regulated supply voltage	DC voltage input from emitter of external series-pass transistor; this voltage powers internal logic of chip.
39	VR	Reference voltage	Reference voltage output to base of series-pass transistor; this reference controls VCR.
40	V_{CC}	Supply voltage	+5V power.

BLOCK DIAGRAM



NOTES:
1. Components shown with dotted lines are located off-chip.
2. Certain bits of the status control registers connected to the I/O bus are 'read-only'; this distinction is not shown in the diagram.
3. Greater detail for the more complicated blocks (Phase-Lock Loop, Data Separator, etc.) are shown in other areas of this data sheet.

SYSTEM INTERFACE

A typical flophy disk controller using an 8X300 microcontroller and the 8X330 is shown in Figure 2. The non-shaded portion of this particular configuration can service the command, status, and input/output requirements of two double-sided disk drives and, under software supervision, the system can read/write single-density (FM) or double-density (MFM/M^{2}FM) codes. Interface requirements consist of the 8X300 microcontroller and the two disk drives. All 8X330 control and data registers directly linked to the microprocessor interface (Figure 1) are addressable and appear to the 8X300 as simple I/O ports; a 13-bit address bus and a 16-bit instruction bus provide communications between the 8X300 and up to 8K of microprogram storage.

The disk-drive interface consists of seven output control lines (DC1-DC7), five input status lines (DS1-DS5), a write gate ($\overline{WG}$), a data-write output ($\overline{DW}$), and a data-read input ($\overline{DR}$). The twelve command/status lines are not dedicated; thus, the user can assign system functions to best suit a given application. As shown in Figure 2, all control lines except $\overline{WG}$ are buffered to accommodate a reasonable distance between the controller and the disk media; the Write Gate, being a 40mA output, requires no buffering.

As shown by the shaded part of Figure 2, the control and status lines can be expanded with peripheral hardware — the 8T32 (in this example) being only one method of implementation. Using this particular technique, one I/O port is totally dedicated to output control, whereas, the other port is totally dedicated to input status. With additional hardware and supporting software, the disk-drive system can be expanded without limit; however, five or six drives is sufficient for most applications. By using the programmable features of the 8X330, the user can emphasize and prioritize those system parameters that are most important — economics, reliability and/or speed.

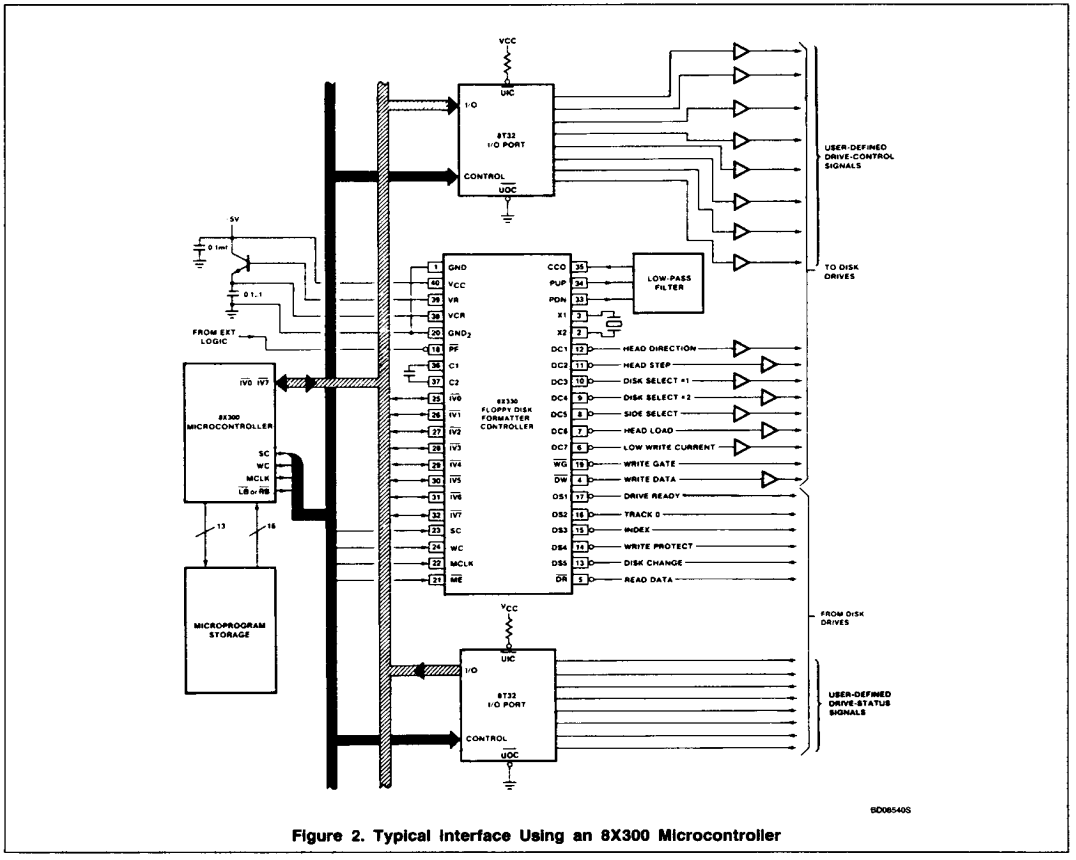


Figure 2. Typical Interface Using an 8X300 Microcontroller

FUNCTIONAL OPERATION

As shown in Figure 2, the interface between the 8X300 and 8X330 consists of twelve lines — $\overline{IV0}$-$\overline{IV7}$, SC, WC, MCLK, and $\overline{ME}$; the Master Enable ($\overline{ME}$) input (pin 21) is driven from either the $\overline{LB}$ (Left Bank) or $\overline{RB}$ (Right Bank) output of the 8X300. An expanded view of this interface is shown in Figure 3 and, as indicated, the 8X330 appears as a number of addressable registers (110_8-127_8 and 132_8-137_8) under input/output control of the 8X300. These registers are used for general-purpose storage, data-transfer operations, disk commands, disk status, and various control functions. Design-oriented information for these registers and other data-processing/logic functions of the 8X330 are described in the paragraphs that follow; in all of these registers, bit 0 is the Most Significant Bit (MSB).

NOTE:
When power is first applied to the 8X330, the Disk Command lines (DC1-DC7), the Write Gate ($\overline{WG}$) output, and contents of Command/Status Register #2 (CSR #2) are set to 1 (high). The wakeup state of all other bits is undefined.

General-Purpose Register File

This general-purpose (scratch pad) memory is directly accessible by the 8X300 and is used to store system variables such as track address, sector address and other necessary parameters. The sixteen 8-bit registers (110_8-127_8) provide sufficient on-chip memory to accommodate a minimum of two disk drives; the maximum number of drives that this non-dedicated memory file can support depends on several factors — system configuration, reliability requirements, economic constraints, and so on. Because of the on-chip file, all other system memory can be dedicated to the purpose of handling data to-and-from the disk media.

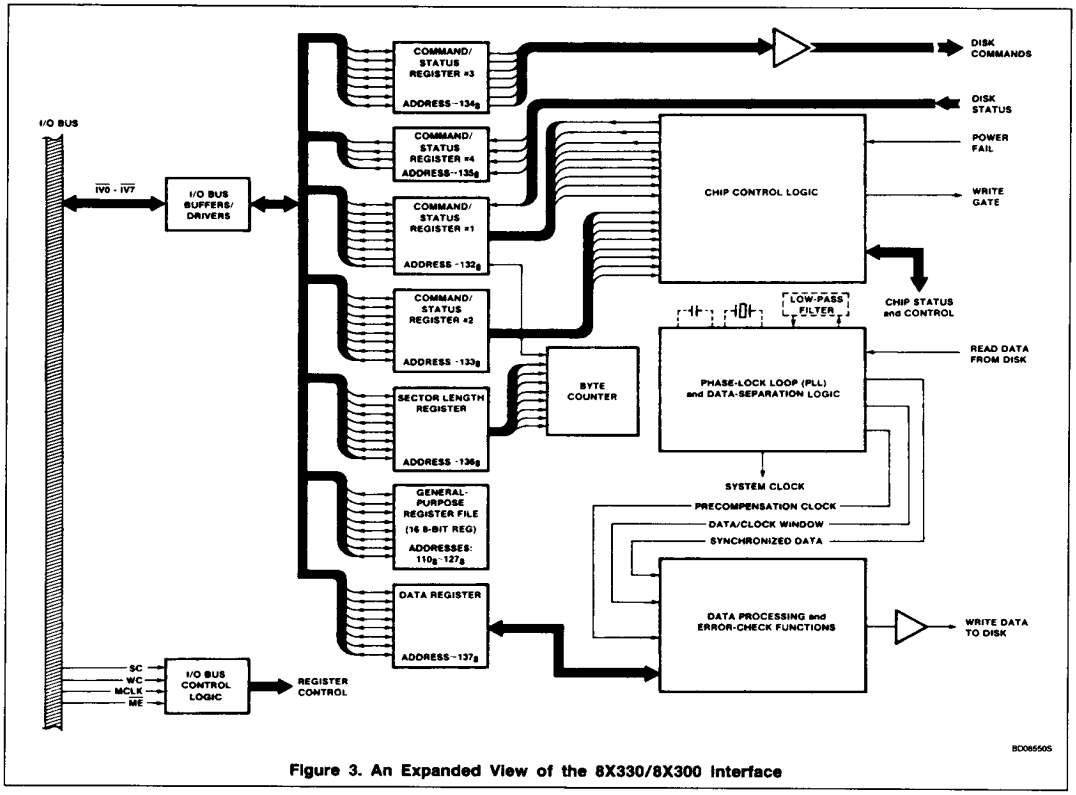


Figure 3. An Expanded View of the 8X330/8X300 Interface

Command/Status Register #1 (CSR 1/Address 132_8)

The disk status (read) or disk-command (write) contents of this register are interpreted as follows: unless otherwise indicated, all bits of CSR 1 are read/write from the I/O bus.

Bit 0 (Write Gate Enable)

Enables write gate output ($\overline{WG}$/pin 19) to disk drive(s) — the write gate ($\overline{WG}$) cannot be enabled unless the PF input pin (18) is high. When the WGE bit is set to 0, the $\overline{WG}$ output pin is low (enabled); when WGE is set to 1, the $\overline{WG}$ output is high (disabled). If the PF input goes low while the $\overline{WG}$ output is low, the $\overline{WG}$ output will go high and the Write Gate Enable bit is reset to 1.

Bit 1 (CRC Enable)

When set to 1, permits internal CRC register to compute remainders on the data stream in either read or write modes of operation. When set to 0, the CRC register becomes the source of data. A change in the CRC Enable bit does not become effective until the "next BYTRA flag appears" following the command bit change (refer to description of CSR 1/Bit 6).

Bit 2 (Data Register Control)

When set to 0, contents of data register consists of interleaved data-and-clock bits; starting from the MSB ($\overline{IV0}$) position, register contents are: Clock 1, Data 1, Clock 2, Data 2, Clock 3, Data 3, Clock 4, and Data 4. When writing an address mark, the appropriate data/clock pattern is loaded into the data register by the 8X300. Since each byte of data from the processor becomes an interleaved pattern (4-bits of data and 4-bits of clock) in the 8X330 data register, two bytes from the processor are required to write each full byte of address mark to the drive — eight bit cells with each cell containing a possible data and/or clock transition, or a total of 16-bit positions. When writing address marks, the normal on-chip clock insertion circuitry of the 8X330 is inhibited; thus, the user is free to define any clock/data pattern for the address mark.

When reading address marks, the data register is loaded with data and clock representing four bit cells from the disk media. The information in the data register can then be compared with the expected address mark by the 8X300 on a nibble-by-nibble basis. When the DRC bit is set to 1, the data register contains separated data (no clocks). A state change in this bit does not become effective until the 'next BYTRA flag appears" following the state-change command.

Bit 3 (Sync Enable)

The Sync Enable bit allows the on-chip data separator to obtain bit and byte synchronization; this bit also controls initialization of the CRC Register. With the 8X330 in Read mode and with Bit 3 set to 0, bit synchronization occurs. The Preamble field is assumed to be all "zeroes" or all "ones" as determined by the Preamble Select bit (SCR 2/Bit 4).

When the proper number of preamble bytes, as determined by the disk-control program, have been found, the Sync Enable bit should

be changed, under program direction, to a 1. This puts the 8X330 in the Address-Mark search mode. Accordingly, all bits of the CRC Register are preset to 1, the BYte TRAnsfer flag is inhibited, and the 8X330 examines the data stream for an Address Mark. The Address Mark is detected by observing the data and clock bits to find a change in the normal Preamble pattern. Byte synchronization is achieved by assuming that the change occurred in the bit cell determined by two Bit Select bits (CSR 2/Bits 2 and 3).

When the pattern change is found indicating the start of an Address Mark, the 8X330 starts CRC computation and synchronizes BYTRA to the byte boundaries. Note that the 8X330 presumes and Address Mark by finding a change in the preamble pattern; however, it is up to the 8X300 to read the Address Mark and to establish its validity or nonvalidity.

In write mode, setting the Sync Enable bit to 0 presets all bits of the CRC Register to 1. Setting the Sync Enable bit to 1 allows CRC computation to begin at the next byte boundary.

Bit 4 (Load Counter)

When set to 1, transfers 8-bits of data from Sector Length register and 1-bit (MSB) of data from Byte Counter (refer to next description) to 9-bit Byte Counter. Loading of the 9-bit Byte Counter is effective one bit-cell time after the Load Counter bit is set to 1. In both the read and write modes of operation, the Byte Counter is incremented by BYTRA. The Load Counter bit is self-clearing and always returns a 0 when read.

NOTE:
The Load Counter bit must be set one or more instruction cycles *after* setting the Byte Counter MSB, that is, bits 4 and 5 of CSR 1 cannot be set during the same instruction cycle.

Bit 5 (Byte Counter MSB)

This bit is used to set and monitor the state of the ninth (MSB) bit in the Byte Counter; reading this bit always returns the current state of MSB in the Byte Counter. The MSB of the Byte Counter is set to the value of CSR 1/Bit 5 when the Load Counter bit (CSR 1/Bit 4) is asserted — refer to preceding description.

NOTE:
The Byte Counter MSB must be set one or more instruction cycles *before* the Load Counter bits — bits 4 and 5 of CSR 1 cannot be set during the same instructions cycle.

Bit 6 (BYTRA)

During a disk read operation, the BYTRA flag is automatically set to 0 when 8-bits of information are transferred from the Data Shift Register to the Data Register — see Figure 1. During a disk write operation, BYTRA is automatically set to 0 when 8-bits are transferred from the Data Register to the Data Shift Register. BYTRA (a read-only bit) is reset to a 1 when the Data Register (address 137_8) is selected by the user's program. During read/write operations, the 1-to-0 transition of the BYTRA flag increments the Byte Counter to keep count of bytes read or bytes written. All read-only bits of the 8X330 are designed to remain stable during the monitor period; thus, to read a status change of BYTRA, Disk-Status bit, the Byte Counter MSB, or other read-only bit requires a two-instruction loop similar to:

```
TEST    SEL     CSR 1
        NZT     BYTRA,  TEST
```

Bit 7 (Disk Status 1)

Reflects state (0 or 1) of input DS1 (pin 17); this is a user-definable read-only bit.

NOTE:
A high input on any one of the Disk Status lines of the 8X330 is read by the 8X300 program as a logical 1 and a low input on the status lines is read as a logical 0.

PRECOMP TIME	DATA/CLOCK PATTERN (IN DATA SHIFT REG)			BIT BEING WRITTEN	BITS ALREADY WRITTEN TO DISK		
2T (Late)	0	1	0	1	0	0	0
2T (Late)	0	1	0	1	0	0	1
2T (Early)	1	0	0	1	0	1	0
2T (Early)	0	0	0	1	0	1	0

NOTE:

where, $T = \frac{1}{\text{crystal frequency}}$ if bit 7 of CSR 2($\frac{1}{2}$F) = 1

$T = \frac{2}{\text{crystal frequency}}$ if bit 7 of CSR 2($\frac{1}{2}$F) = 0

Command/Status Register #2 (CSR 2/Address 133_8)

The disk status (read) or disk-command (write) contents of this register are interpreted as follows:

Bit 0 (Precompensation Enable)

This command bit determines whether or not precompensation is applied to the data stream being written onto the disk. When set to 0, precompensation is inhibited. When set to 1 and with double-density encoding, write precompensation is applied to the data/clock bit patterns in the table to the left.

Bit 1 (Read Mode)

When set to 0, the 8X330 reads data from the disk and transfers it to the Data Register; when set to 1, data from the Data Register is transferred to the disk, provided the Write Gate Enable bit (CSR1/Bit 0) is set to 1. With WGE set to 0 and the Read Mode bit set to 1, the current-controlled oscillator is forced to lock onto the crystal oscillator; this technique is used during a data-read operation to ensure rapid acquisition of the disk data.

Bits 2, 3 (Bit Selects 1 and 0)

Together with the Sync Enable (CSR 1/Bit 3), these two bits allow the user to establish byte boundaries for the data stream; this is done in the following way. After bit synchronization is established, and the preamble pattern is verified, the 8X330 looks for a change in the normal preamble pattern. As shown in the following Truth Table, Bit Select 1 (Bit 2) and Bit Select 0 (Bit 3) identifies the bit cell within the first nibble of the first Address-Mark byte in which the first deviation from the normal preamble is expected. BYTRA is always referenced to bit cell 0.

BS 0	BS 1	BIT CELL
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4 (Preamble Select)

This bit is used only for bit synchronization — refer to CSR 1/Bit 3. With Bit 1 of CSR 2 set to 0 (Read Mode) and the Preamble Select bit set to 0, the preamble field is assumed to be all zeroes; with the Preamble Select it set to 1, the preamble field is assumed to be all ones. In either case, preamble validity is determined by the 8X300.

Bits 5,6 (E1 and E2)

Together, E1 and E2 select the encoding scheme used to write data on the disk — refer to truth table that follows.

E1	E2	ENCODING SCHEME
1	X	FM
0	0	MFM
0	1	M^2FM

x = don't care

Bit 7 (1/2F)

This bit allows the data transfer rate to be changed without modification of the frequency-selective components in the data-separation logic; thus, differences in data transfer rates between standard-and-mini floppies can be accommodated via software — no component or other hardware changes. Assuming an 8MHz crystal and with the 1/2F bit set to 1, the data transfer rate is 250K bits per second in the single-density (FM) mode and 500K bits per second in the double-density (MFM/M^2FM) mode. When set to 0, the transfer rates are halved — 125K bits and 250K bits, respectively. When using frequencies other than 8MHz, the data transfer rate is determined as follows:

BIT 7 (½F)	SINGLE-DENSITY (FM)	DOUBLE-DENSITY (MFM/M^2FM)
0	$\frac{\text{xtal freq}}{64}$	$\frac{\text{xtal freq}}{32}$
1	$\frac{\text{xtal freq}}{32}$	$\frac{\text{xtal freq}}{16}$

Command/Status Register #3 (CSR 3/Address 134_8)

This register contains seven bits (Bit 0 through Bit 6) which determines the state of the disk-command outputs; writing to Bit 7 has no effect and reading Bit 7 always returns a zero. When a logical "1" is specified by the 8X300 program for a given disk-command line, a high will appear at the output of the 8X330 for that particular command line. Each bit and the output pin it controls are summarized below.

BIT (CSR 3)	CONTROL FUNCTION	PKG PIN NO
0	DC1 Output	12
1	DC2 Output	11
2	DC3 Output	10
3	DC4 Output	9
4	DC5 Output	8
5	DC6 Output	7
6	DC7 Output	6

Command/Status Register #4 (CSR 4/Address 135_8)

This register contains four bits (Bit 0 through Bit 3) which reflect the state of the disk-status inputs to the 8X330; reading all other bits (4 through 7) always returns a zero. These read-only bits and the reflected status they represent are as follows; the information specified by notation for Bit 7/CSR 1 is applicable to these input lines.

BIT (CSR 4)	CONTROL FUNCTION	PKG PIN NO
0	DS2 Input	16
1	DS3 Input	15
2	DS4 Input	14
3	DS5 Input	13

Sector Length Register — Address 136_8

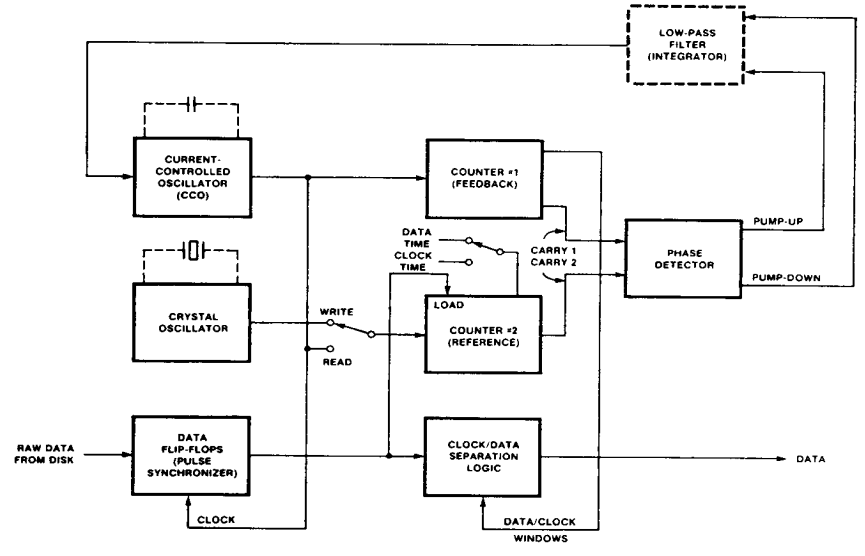
This register contains the load value for the lower eight (LSBs) bits of the Byte Counter. Data is transferred from the Sector Length Register to the Byte Counter under control of Load Counter Bit in CSR 1. When the contents of this register are transferred to another location via a read or write commands, the original holding of data is not lost; thus, if the same data is to be used more than once, a repetitive read or write can be implemented without reloading the register.

Data Register — Address 137_8

Together with the Data Shift Register, the Data Register is used for bidirectional transfer of data between the 8X330 and the I/O bus. All transfers to-and-from this register are made in conjunction with Bit 6 (BYTRA — Byte Transfer Flag) of CSR 1. When the Data Register Control bit (CSR 1/Bit 2) is set to 0, the content of this register is interleaved with four bits of data and four bits of clock. When data is transferred from the Data Register to the Data Shift Register, the original content of the Data Register is not lost.

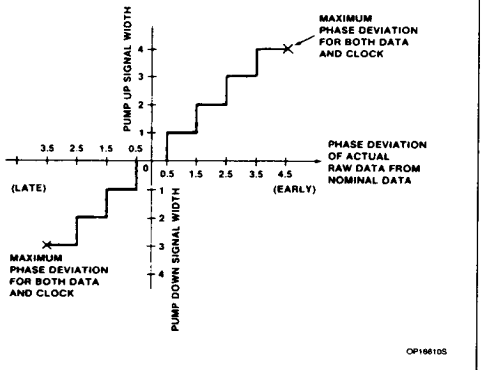
Phase Lock Loop (PLL) and Data Separation Logic

An expanded view of the phase-lock loop and the data-separation logic is shown in Figure 4. Basically, the PLL consists of two counters, a phase detector, and a feedback loop containing a low-pass filter (off-chip) that controls a phase-locked oscillator (CCO). In simplified form, the data-separation logic consists of data flip-flops (pulse synchronizer) and other circuits required to separate data and clock transitions. In the read mode, the output of the phase-locked oscillator (CCO) is applied to the clock inputs of counter #1, counter #2, and the pulse synchronization circuits. Essentially, the frequencies of the two counters are identical (phase relationships may or may not be identical); to maintain proper frequencies and to continuously correct any phase deviations, the following actions occur. Preset values which represent, respectively, nominal midpoints of the clock and data windows are present at counter #2 and, when an output appears at the pulse synchronizer, these preset values are entered. The count sequence for both counters is from "0 to F"; hence, the phase difference between Carry 1 (counter #1) and Carry 2 (counter #2) actually corresponds to any phase deviation between the CCO and the synchronized data from the disk. The phase detector measures the phase difference between the two carry inputs and produces a series of quantized pulses whose widths are proportional to the phase error at the end of each counting cycle. After integration by the low-pass filter, a current proportional to the phase error is applied to the current-controlled oscillator. Accordingly, the CCO is driven in a direction (pump-up or pump-down) to correct any phase difference between the synchronized disk data and the feedback-controlled clock. Phase detector characteristics for both single-and-double density formats are shown in Figures 5 and 6.



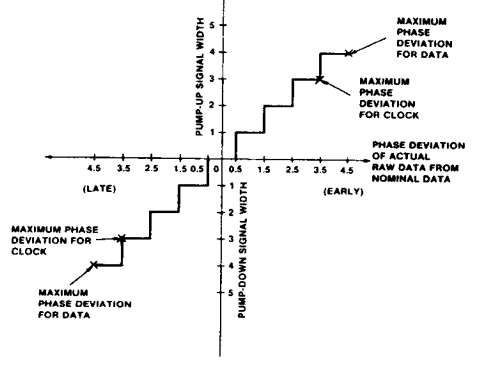
NOTE:
Components shown with dashed lines are located off-chip

Figure 4. Simplified Block of Phase-Lock Loop



NOTE:
All horizontal/vertical units are specified in CCO clock periods; for Standard Floppy FM Format, one CCO clock period equals 250 nanoseconds

Figure 5. Phase Detector Characteristic for Single-Density (FM) Format



NOTE:
All horizontal/vertical units are specified in CCO clock periods; for standard floppy double density (MFM/M^{2}FM), one CCO clock period equals 125 nanoseconds

Figure 6. Phase Detector Characteristic for Double-Density (MFM/M^{2}FM) Format

Data Processing and Error-Check Functions

The functions of the 8X330 are summarized in Figures 7 and 8. The read/write operations are software-controlled by previously-described bits of command/status registers CSR1 and CSR2. For the sake of simplicity, control lines and much of the control logic associated with the data processing and error-check functions are omitted in the read/write diagrams.

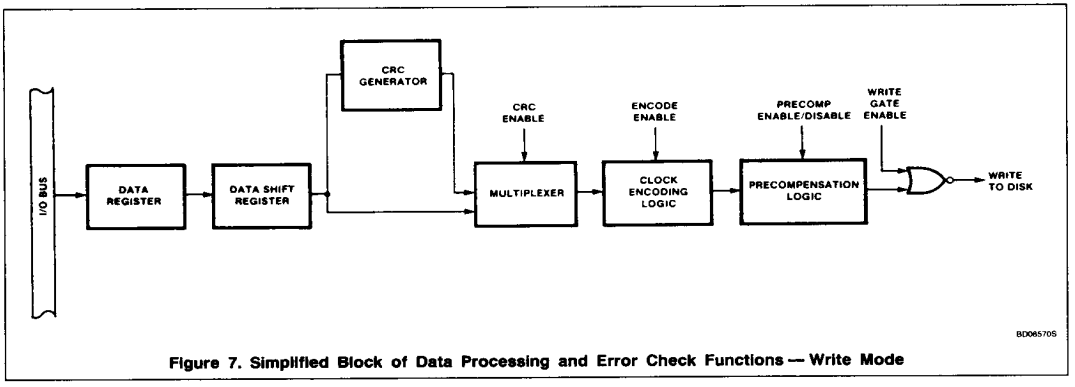


Figure 7. Simplified Block of Data Processing and Error Check Functions — Write Mode

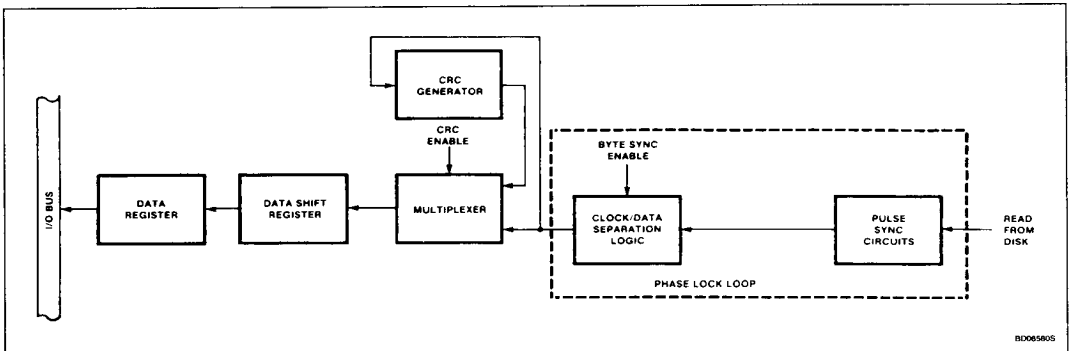


Figure 8. Simplified Block of Data Processing and Error Check Functions — Read Mode

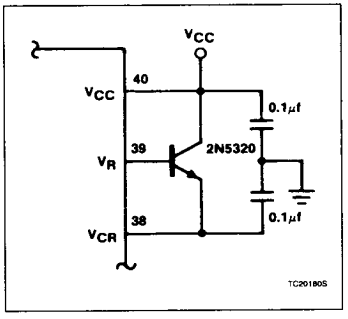
DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V (±5%), T_A = 0°C to 70°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS	COMMENTS
			Min	Typ	Max		
V_{IH}	High-level input voltage		2		V_{CC}	V	For all inputs except X1, X2, C1, C2, CCO, and V_{CR}
V_{IL}	Low-level input voltage		−1		0.8	V	
V_{CC}	Supply voltage		4.75	5	5.25	V	5V (±5%)
V_{CR}	Regulator voltage	V_{CC} = 5V		3.1		V	From series-pass transistor
V_{CL}	Input clamp voltage	V_{CC} = Min I_{IN} = −5mA	−1			V	Inputs X1, X2, C1, C2, and CCO do not have internal clamp diodes.
V_{OH}	High-level output voltage	V_{CC} = Min; I_{OH} = −0.4mA	2.7			V	DC1 through DC7 (Pins 6 – 12) & $\overline{DW}$ (Pin 4)
		V_{CC} = Min; I_{OH} = −3mA	2.4			V	$\overline{IV0}$ – $\overline{IV7}$ (Pins 25 – 32)
V_{OL}	Low-level output voltage	V_{CC} = Min; I_{OL} = 8mA			0.5	V	DC1 through DC7 (Pins 6 – 12); $\overline{PUP}$, $\overline{PDN}$ (Pins 33, 34); $\overline{DW}$ (Pin 4)
		V_{CC} = Min; I_{OL} = 16mA			0.55	V	$\overline{IV0}$ – $\overline{IV7}$ (Pins 25 – 32)
		V_{CC} = Min; I_{OL} = 40mA			0.55	V	$\overline{WG}$ (Pin 19)
I_{CEX}	Open-collector leakage current with output set to 1.	V_{CC} = Min; V_{OUT} = V_{CC}			100	μA	$\overline{WG}$ (Pin 19); $\overline{PUP}$ (Pin 34); $\overline{PDN}$ (Pin 33)
I_{IH}	High-level input current	V_{CC} = Max; V_{IN} = 2.7V			20	μA	DS1 – DS5 (Pins 13 – 17); $\overline{PF}$ (Pin 18); $\overline{DR}$ (Pin 5)
					40	μA	$\overline{ME}$ (Pin 21); MCLK (Pin 22); SC (Pin 23); WC (Pin 24)
		V_{CC} = Max; V_{IN} = 5.25V; CCO (Pin 35) input current = 0mA			4	mA	With C1 (Pin 36) under test, C2 (Pin 37) is open and, vice-versa.
		V_{CC} = Max; V_{IN} = 5.25V CCO (Pin 35) input current = 1mA			2	mA	
		V_{CC} = Max; V_{IN} = 0.6V			4	mA	With X2 (Pin 2) under test, X1 (Pin 3) is open and, vice-versa.
		V_{CC} = Max; V_{IN} = 4.5V			50	μA	$\overline{IV0}$ – $\overline{IV7}$ (pins 25 – 32)
V_{CCO}	Input voltage for current-controlled oscillator	V_{CC} = 5V; T_A = 25°C CCO input current (Pin 35) = 300μA		750		mV	
I_{IL}	Low-level input current	V_{CC} = Max; V_{IN} = 0.4V			−400	μA	DS1 – DS5 (Pins 13 – 17); $\overline{PF}$ (Pin 18); $\overline{DR}$ (Pin 5)
					−800	μA	$\overline{ME}$ (Pin 21); MCLK (Pin 22); SC (Pin 23); WC (Pin 24)
					−4	mA	X1 (Pin 2), X2 (Pin 3), with X1 under test, X2 is open and, vice-versa.
		V_{CC} = Max V_{IN} = 0.5V			−550	μA	$\overline{IV0}$ – $\overline{IV7}$ (Pins 25 – 32)

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS	COMMENTS
			Min	Typ	Max		
I_{OS}	Output short-circuit current	V_{CC} = Max; Output = "1"; V_{OUT} = "0".	−15		−100	mA	DC1 − DC7 (Pins 6 − 12) & $\overline{DW}$ (Pin 4)
		(NOTE: At any time, no more than one output should be connected to ground)	−30		−140	mA	$\overline{IV0}$ − $\overline{IV7}$ (Pins 25 − 32)
I_{CC}	(Pin 40)	V_{CC} = Max			200	mA	
I_{CR}		V_{CC} = Max			250	mA	
I_{REG}	(Pin 39)	V_{CC} = 5V; V_{CR} = 0V & V_R = 2V	−16		−27	mA	

NOTES:
1. Operating temperature ranges are guaranteed after thermal equilibrium has been reached.
2. All voltages measured with respect to ground terminal.
3. Unless otherwise specified, each test requires that V_{CR} be supplied through a series-pass transistor as shown in the accompanying drawing.

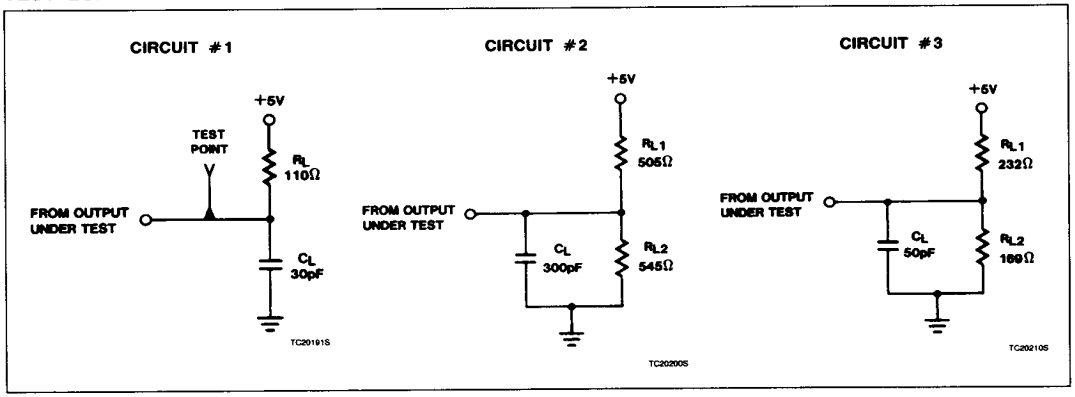


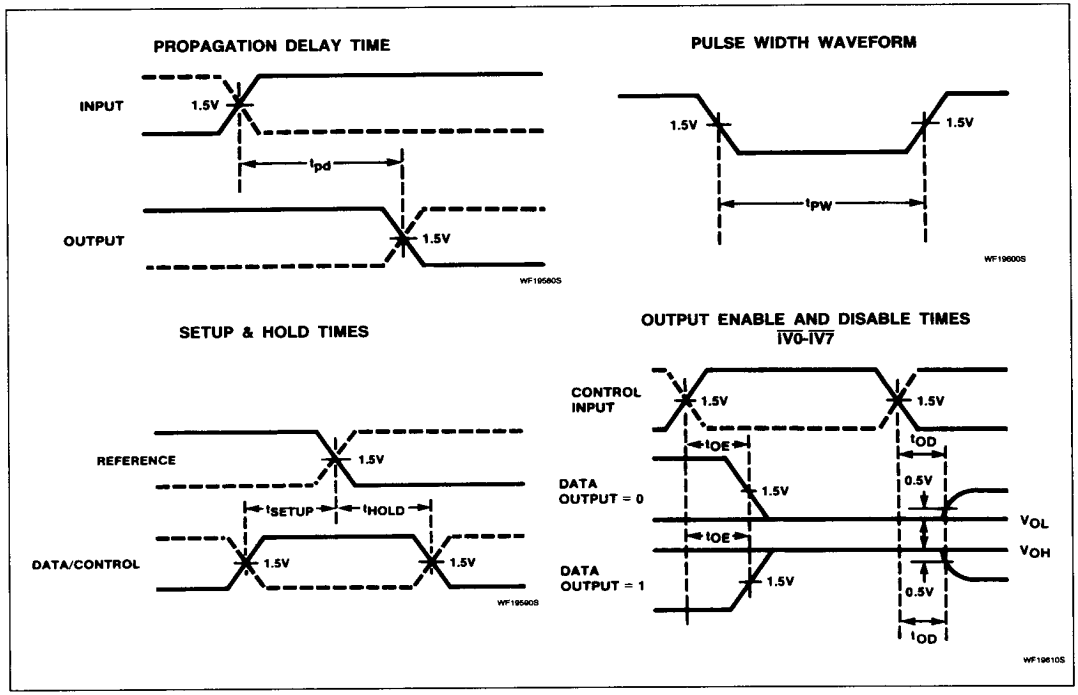
AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V(±5%), T_A = 0°C to 70°C

MNEMONIC	REFERENCE	INPUT	OUTPUT	TYPICAL MINIMUM	TYPICAL MAXIMUM	COMMENTS
t_{PD}		↓ $\overline{PF}$	$\overline{WG}$ ↑		60ns	Refer to Note 3 and Test Loading Circuit #1.
t_{PD}		↑ MCLK	$\overline{WG}$ ↑		100ns	
t_{PD}		↑ MCLK	$\overline{WG}$ ↓		100ns	
t_{PD}		↑ MCLK	DC1 – 7 ↑		70ns	Refer to Note 3 and Test Loading Circuit #2.
t_{PD}		↑ MCLK	DC1 – 7 ↓		70ns	
t_{PW}		↓ $\overline{PF}$ ↑		50ns		
t_{PW}		↓ $\overline{DR}$ ↑		50ns		
t_{PW}			↓ $\overline{DW}$ ↑			Note 1
t_{SETUP}	↓ SC	Input on DS1 – 5		55ns		Note 2
t_{SETUP}	↓ WC	Input on DS1 – 5		55ns		Note 2
t_{SETUP}	↓ $\overline{ME}$	Input on DS1 – 5		55ns		Note 2
t_{HOLD}	↓ SC	Input on DS1 – 5		0ns		Note 2
t_{HOLD}	↓ WC	Input on DS1 – 5		0ns		Note 2
t_{HOLD}	↓ $\overline{ME}$	Input on DS1 – 5		0ns		Note 2
t_{OE} — $\overline{ME}$, SC & WC		↓ $\overline{ME}$ ↓ SC ↓ WC	I/O bus		25ns	Refer to Test Loading Circuit #3.
t_{OD} — $\overline{ME}$, SC & WC		$\overline{ME}$ ↑ SC ↑ WC ↑	I/O bus (3-State)		30ns	
t_w (MCLK pulse width)		↑ MCLK ↓		45ns		
t_{SD} (data setup time)	MCLK ↓	I/O bus		50ns		
t_{SD} ($\overline{ME}$ setup time)	MCLK ↓	$\overline{ME}$		45ns		
t_{SD} (SC setup time)	MCLK ↓	SC		45ns		
t_{SD} (WC setup time)	MCLK ↓	WC		45ns		
t_{HD} (data hold time)	MCLK ↓	I/O bus		0ns		
t_{HD} ($\overline{ME}$ hold time)	MCLK ↓	$\overline{ME}$		0ns		
t_{HD} (SC hold time)	MCLK ↓	SC		0ns		
t_{HD} (WC hold time)	MCLK ↓	WC		0ns		

NOTES:
The values of these parameters were determined by device characterization procedures. They are, however, neither tested nor guaranteed.
1. Write pulse width = $2/F_{XTAL}$, that is, or 8MHz crystal, t_{pw} = 250nsec (typical)
2. Changes on DS1 – 5 are not stored in read mode ($\overline{ME}$ = 0, SC = 0, and WC = 0)
3. During the period when MCLK is high, measurement is made with $\overline{ME}$ = Low, SC = Low, and WC = High.

TEST LOADING CIRCUIT





CLOCK REQUIREMENTS

Crystal Oscillator

The on-chip crystal oscillator circuit is designed for operation using an external series-resonant quartz crystal; alternately the crystal oscillator can be driven with complementary outputs of a pulse generator or interfaced to a master clock source via TTL logic — see accompanying circuits. When a crystal is used, the on-chip oscillator operates at the resonant frequency (f.) of the crystal; the crystal connects to the 8X330 via pins 3(X1) and 2 (X2). The lead lengths of the crystal should be approximately equal and as short as possible; also, avoid close proximity to all potential noise sources. The crystal should be hermetically sealed (HC type can) and have the following electrical characteristics:

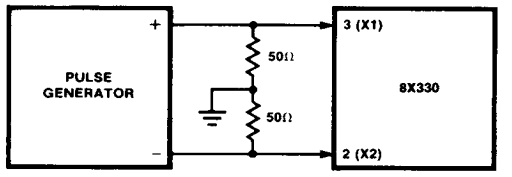
Type: Fundamental mode, series resonant

Impedance at Fundamental:
35-Ω maximum

Impedance at Harmonics and Spurs:
50-Ω minimum

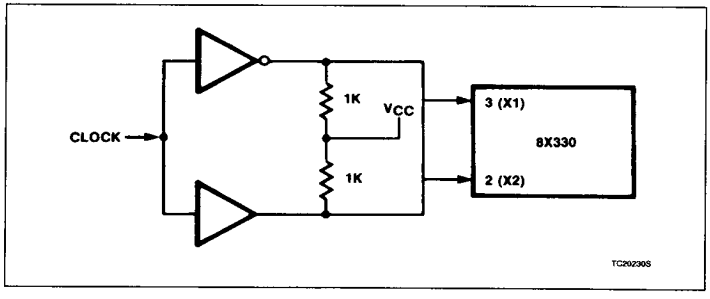
When the crystal oscillator is externally-driven, typical waveforms are as follows:

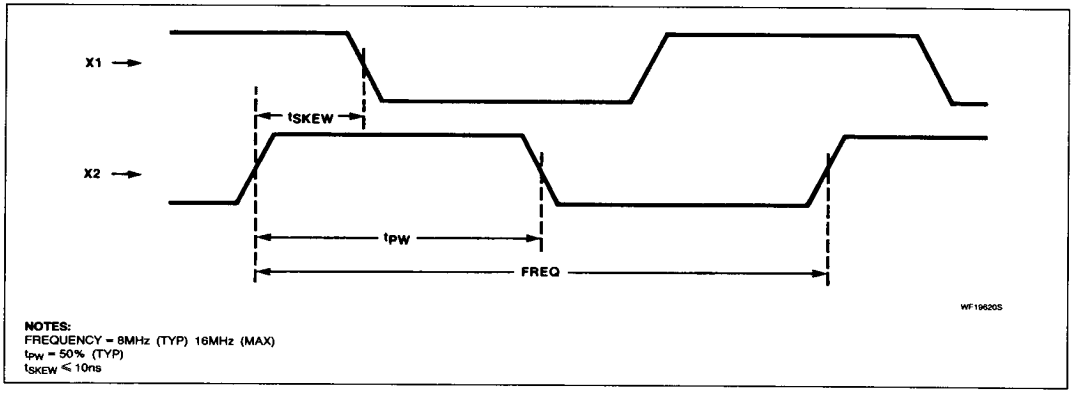
CLOCKING XTAL OSC WITH PULSE GEN



NOTES:
PULSE GEN CHAR:
Z_{OUT} = 50Ω
V_{OUT} = 0 – 2V
RISETIME ≤ 10ns
SKEW ≤ 10ns
COMPLEMENTARY OUTPUTS

CLOCKING XTAL OSC WITH OPEN-COLLECTOR TTL



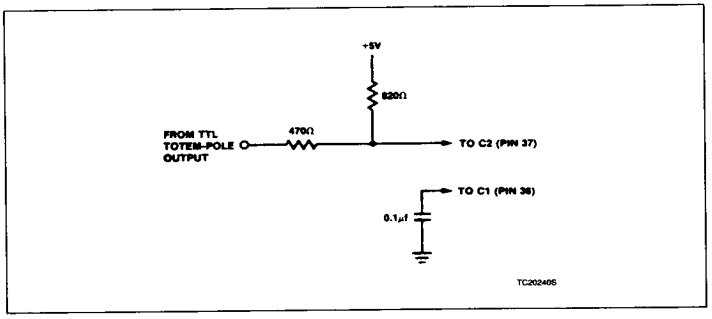


NOTES:
FREQUENCY = 8MHz (TYP) 16MHz (MAX)
t_{PW} = 50% (TYP)
t_{SKEW} ≤ 10ns

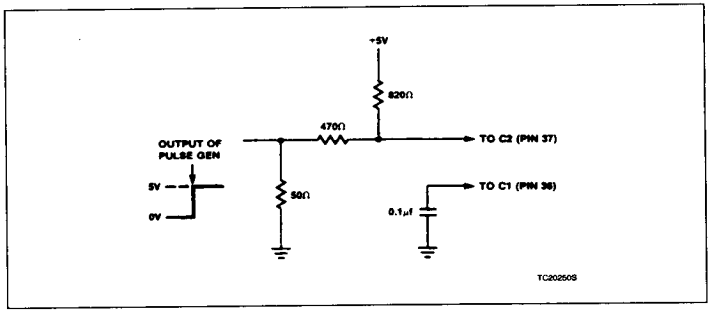
Current-Controlled Oscillator (CCO).

A non-polarized ceramic or mica capacitor is recommended for the current-controlled oscillator. The capacitor connects to the 8X330 via pins 37 (C2) and 36 (C1); lead lengths of the capacitor should be approximately the same and as short as possible. When the input current to the CCO is near zero (maximum frequency), the capacitor value should be chosen so that the high-limit rest frequency of the oscillator does not exceed 24MHz. If the rest frequency is higher than 24MHz, synchronization of the CCO with the crystal oscillator just prior to the read operation, may be impeded. The curves in Figure 9 (current-versus-frequency) and Figure 8 (capacitance-versus-frequency) show how these design parameters affect operation of the CCO over a temperature range of 0°C to 70°C. A suitable test circuit for verification/validation of the current-controlled oscillator is also shown in Figure 10. Like the crystal oscillator, the CCO can be driven with the TTL output of a pulse generator or interfaced to a master clock via TTL logic — see accompanying diagrams.

CLOCKING WITH OPEN-COLLECTOR TTL



CLOCKING WITH PULSE GENERATOR



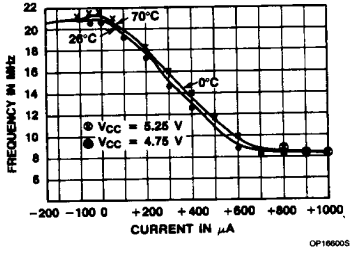


Figure 9. Current-versus-Frequency With: V_{CC} = 5V and Capacitance = 25pF

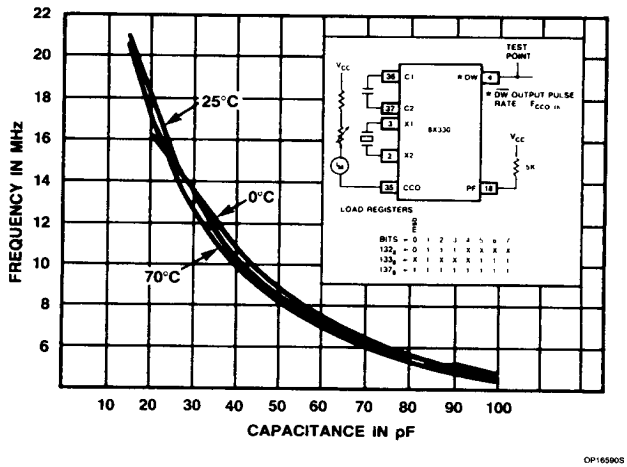
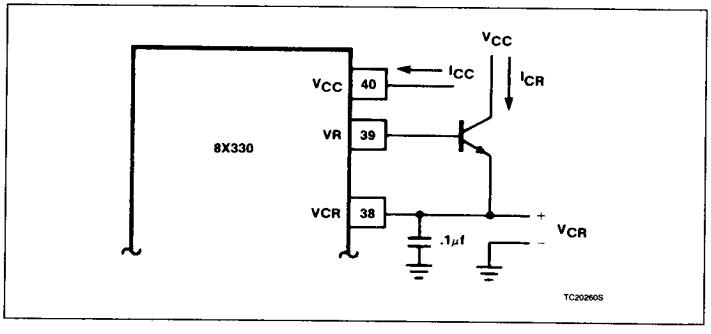


Figure 10. Capacitance-versus-Frequency With: V_{CC} = 5V, VCR = 2.5V, and 1 = 300μA

VOLTAGE REGULATOR

All internal logic of the 8X330 is powered by an on-chip voltage regulator that requires an external series-pass transistor. Electrical specifications for the off-chip power transistor and a typical hook-up are shown in accompanying diagrams. To minimize lead inductance, the transistor should be as close as possible to the 8X330 package and the emitter should be ac-grounded via a 0.1-microfarad capacitor.

TYPICAL HOOK-UP



ORDERING INFORMATION

Order number: N8X330

Package information: Refer to Signetics price list

Supply voltage: 5V (± 5%)

Operating temperature range: 0°C to +70°C

ELECTRICAL SPECIFICATIONS

*PARAMETER	CONDITIONS	LIMITS
h_{fe}	V_{CE} = 2V	> 50
V_{BEON}	V_{CE} = 5V/I_C = 500mA	< 1V
V_{CESAT}	I_C = 500mA/I_B = 50mA	< 0.5V
BV_{CEO}		> 8V
f_t		> 30MHz

NOTE:
*Medium power NPN silicon (0° < T_A < 70°C) recommended parts: 2N5320, 2N5337.