The trap facility is provided so that instructions which are unrecognisable to the hardware can be dealt with in an orderly way. Whenever an unrecognisable instruction is detected, whether in the initial decode stages or in the addressing stages, the trap is sprung as follows. The first three steps are common to the handling of all interrupts:-

* Execution of the instruction is stopped.
* The address of the instruction and the Program Status Word are stored in the system stack.
* The CPU is put into 'Inhibit Interrupt' mode.
* The trap interrupt-handling routine is started by loading the P-register with the start address of that routine, which is held at address X'007E'.
* This trap routine causes the running program to be stopped by executing a HALT instruction.

Note Certain development and other specialized system software may use the trap routine for instruction simulation. In such cases the routine would not stop the program, but would execute a simulation routine before returning to continue normal processing.

The trap facility is supported only on a PTS6810 configuration, and only when all routines are written in Assembly language. 'No Credit' must have been specified at SYSGEN time.