4.1 GENERAL

Two types of control panels are available to provide control and display facilities for the system. These are as follows:-

* System Operator's Panel (standard).

* Computer Full Panel (optional).

A Computer Full Panel may be fitted to PTS6810, 6812, or 6813 machines, but the PTS6813 has an extended computer full panel.

The System Operator's Panel (SOP) may be fitted and used independently of a full panel, whereas full panel operation requires that a SOP be fitted, or that certain facilities are available in the configuration.

4.2 SYSTEM OPERATOR'S PANEL (SOP)

Figure 4.1 shows the layout of the System Operator Panel. The functions of the panel are much the same for PTS6805, 10, 12, and 13, the only difference being that some types have switches, and some have buttons. Figure 4.2 illustrates two different types.

The functions provided by the SOP are described in the following sections.

4.2.1 Safety Key Switch

This is a three position key-operated switch providing control facilities. The three key positions are:-

* NO RTC

  In this position the key cannot be removed and the system is able to run with the Real Time Clock signal inhibited. All other control panel switches are effective.

* RTC

  In this position the key cannot be removed and the system is able to run with the Real Time Clock signal enabled. All other control panel switches are effective.

* LOCK

  In this position the key can be removed and the system is able to run with the Real Time Clock signal enabled. The Bootstrap/IPL switch on the SOP, and all switches on the Computer Full Panel, except the Interrupt buttons, are inhibited.

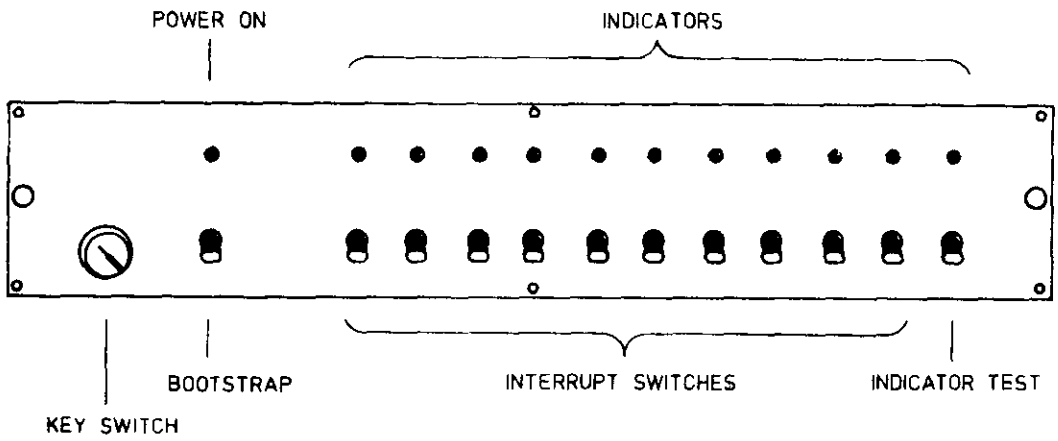

Figure 4.1. System Operator's Panel (SOP).

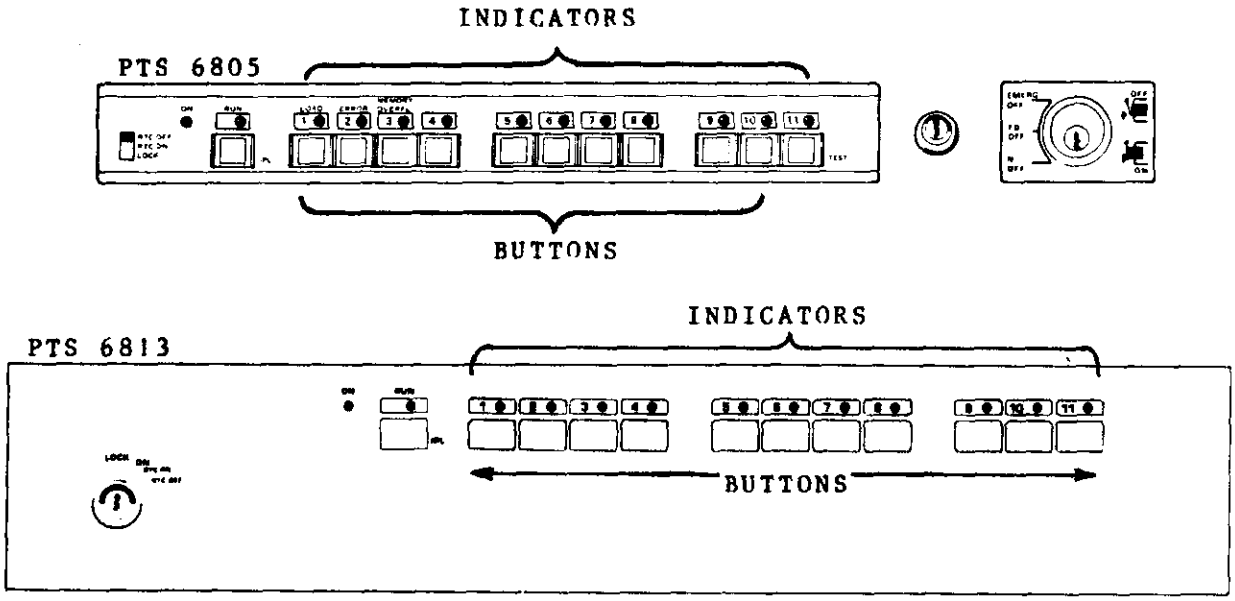

Figure 4.2. PTS 6805 and 6813 SOP's.

4.2.2 Display Indicators

Twelve Indicators are provided, as follows:-

* Power-On Indicator

  This indicator is mounted on the left of the panel, above the Bootstrap/IPL switch. It is used when the SOP is the only panel fitted, to indicate that the basic unit's mains switch is ON, and that power is being supplied to the unit. When the Computer Full Panel is fitted, the SOP's power-on indicator has no function and power-on is indicated on the full panel.

* System Indicators

  Eleven indicators are mounted to the right of the power-on indicator. These may be used as required by the system software and are lit or extinguished by program instructions.

4.2.3 Operator Toggle Switches or Buttons

Twelve single-throw toggle switches or buttons are provided:-

* Bootstrap/IPL

  The bootstrap/IPL switch is mounted to the right of the safety key switch, beneath the power-on indicator, and is operative when the safety key switch is in the NO RTC or RTC position. When operative and depressed the bootstrap switch initiates IPL action as follows:-

  - The bootstrap is loaded into main memory.

  - Current loading parameters are copied into CPU register A15.

  - The CPU is started in RUN mode.

  When using the IPL function, loading may take place from cassette, flexible disk, cartridge disk, or fixed disk.

* Interrupt Switches

  Ten interrupt switches are mounted to the right of the bootstrap/IPL switch. The switches are operative in all positions of the safety key switch and may be used to generate an interrupt to the running program. As the SOP is controlled within the system as an input/output device, program instructions are required to allow interrupts from the switches and to determine which of the switches caused the interrupt.

  The basic interrupt level raised by the switches is the same for all of them, normally level 9, and a hardware priority system within the panel distinguishes between them, giving priority from left to right to the ten switches. If more than one of the switches are depressed simultaneously, only one interrupt is raised. The panel responds with an indication of the highest priority switch depressed when it is interrogated following interrupt action. Following such an action, a second interrupt can only be raised after the release of all the switches depressed.

* Indicator Test Switch

  This switch is mounted on the right of the panel beneath the last system indicator, and provides a test facility for the system indicators. When depressed the switch causes all these indicators to be lit if they are in working order.

4.2.4 Test Panel

Since the SOP functions as an input/output device controlled directly by the channel unit for cassette tape, CHCR, there are certain programming requirements for correct functioning with respect to the operating modes of the channel unit.

The standard addresses, interrupt levels, and the program instructions accepted as control commands to the SOP are as follows:-

* Addresses

  - Standard Address = X'2E'.

  - Alternative Address = X'2F'.

* Interrupt Levels

  - Standard Interrupt Level = Decimal 9.

  - Alternative Interrupt Level = Decimal 11.

* Accepted Instructions

  - OTR.

  This instruction is always accepted and is used to control the system indicators. The value in the register specified by R3 in the instruction is used to select them.

  R3, bits 0 to 4 - Not used.

  R3, bits 5 to 15 - Select indicators 11 to 1 respectively.

  Note The indicators are numbered 1 to 11 from left to right, and a 1 bit set in the appropriate position in register R3 is used to light the corresponding indicator.

  - CIO Start.

  This instruction is used to enable the SOP to raise an interrupt and accept INR instructions. It must be executed at the beginning of the program, or after a CIO Halt instruction has been executed, if interrupts and INR instructions are to be accepted. The contents of the register specified by R3 in the instruction are not used and remain unchanged.

- CIO Halt.

This instruction is used to inhibit interrupts from the SOP. INR instructions sent to the panel after the execution of a CIO Halt instruction, and before the execution of a subsequent CIO Start instruction, will be rejected. The contents of the register specified by R3 in the instruction are not used and remain unchanged.

- INR.

This instruction will be accepted if the SOP has been sent a CIO Start instruction and no subsequent CIO Halt instruction, and providing that the CHCR is not still executing a previously received INR instruction for the panel. The instruction is used to identify the interrupt switch which has caused an interrupt, by transferring a 1 bit into the appropriate position of the register specified by R3 in the instruction.

R3, bits 0 - 5 - Insignificant (set to 1's).

R3, bits 6 - 15 - Interrupt switches 21 to 12.

Note The interrupt switches are numbered 12 to 21 from the left of the panel, switch 12 having the highest priority.

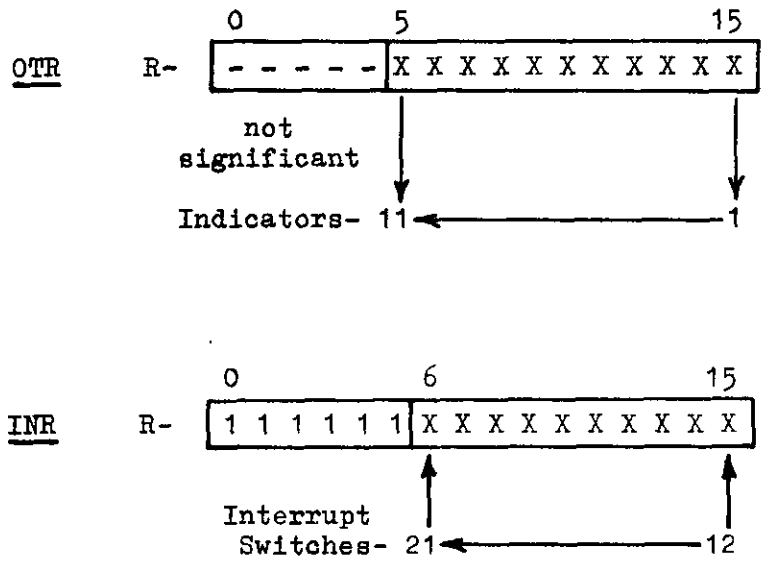

Figure 4.3. Relationship between the indicators and interrupt switches and the bit pattern of the register specified by R3.

4.3 COMPUTER FULL PANEL

Figure 4.4 shows the layout of the Computer Full Panel as fitted to a PTS6805, 10, or 12. The panel may be fitted in conjunction with the SOP to provide additional control and display facilities for system operators and service engineers.
If a panel is not fitted, a blank cover will be fitted in its place.

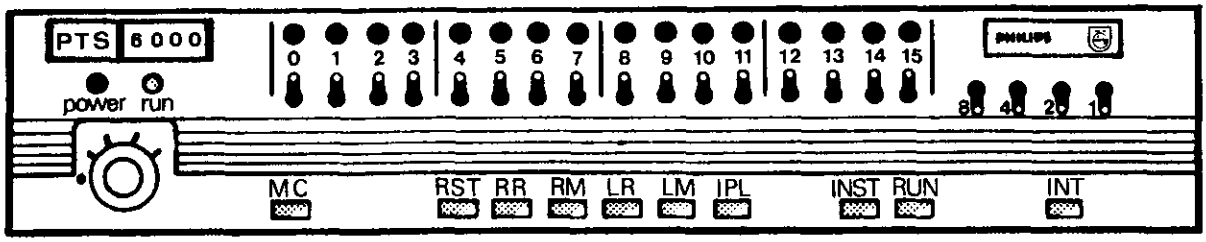

Figure 4.4. PTS6810 or 6812 Computer Full Panel.

The facilities provided by the full panel are listed below.

4.3.1 Display Lamps

Eighteen display lamps are provided as follows:-

* Power-On Lamp

  This lamp is mounted on the left of the panel and is used to indicate that the basic unit's mains switch is ON and that power is being supplied to the unit.

* Run Lamp

  This lamp is mounted to the right of the power-on lamp and is lit when the CPU is operating in RUN mode.

* Data Lamps

  There are sixteen of these, situated one above each data switch and numbered 0 thru 15. The lamps are lit to indicate the contents of the registers, memory, or status word depending on the settings of other control switches. A 1 bit is indicated where a lamp is lit.

4.3.2 Data Switches

There are sixteen numbered data switches mounted centrally on the panel. These are two-position switches used for loading data bits into a register or memory, depending on the setting of other control switches. A 1 bit is loaded when a switch is in the up position.

4.3.3 Register Address Switches

Four switches for register addressing are mounted to the right of the data switches, and they are used to code the address of the register to be used when reading or loading a register from the Data Switches. The switches are labelled with the decimal equivalent of the address value they represent in binary (8, 4, 2, 1) giving an addressing capability of 0 - 15.

4.3.4 Control Buttons

The five control buttons are situated centrally below the Data Switches. The buttons are spring-loaded to return to their original positions after being depressed and each selects and initiates a specific function, as follows:-

* RST - Read Status.

  Depressing this button causes the Program Status Word to be displayed on the lamps. Figure 4.5 shows the format.

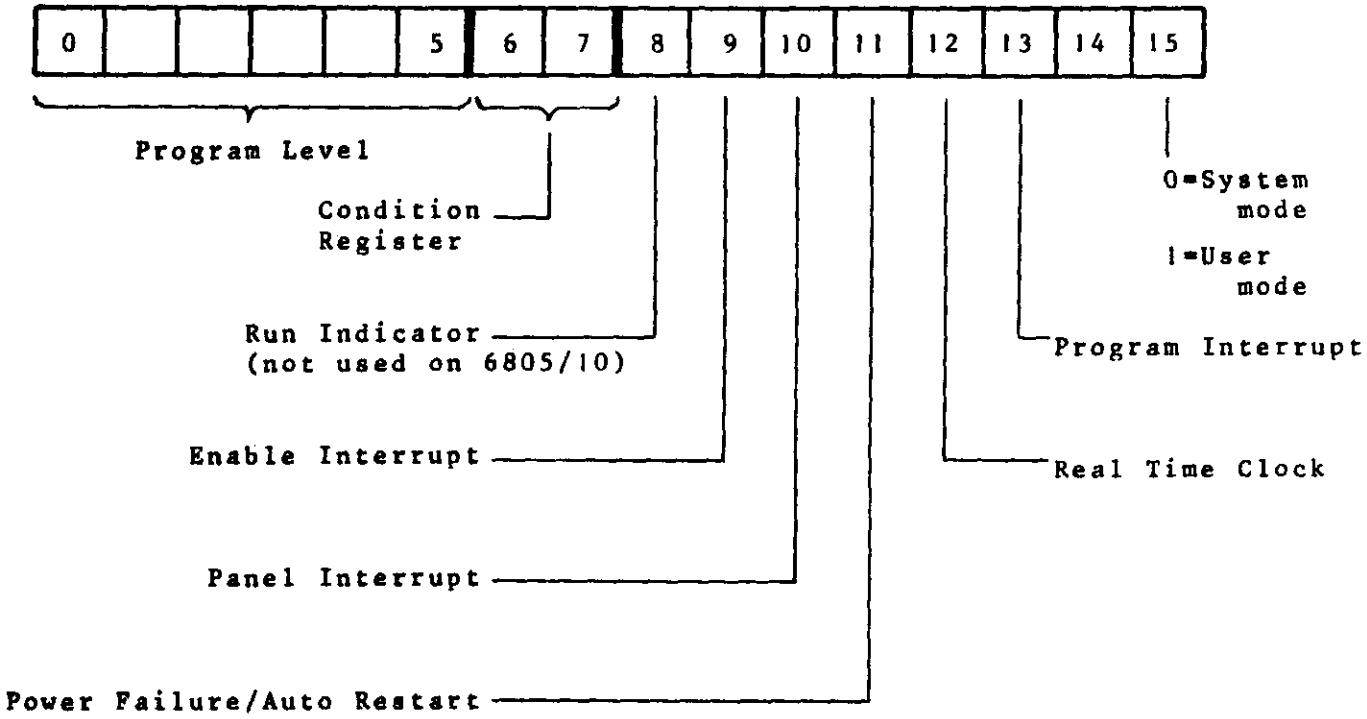

Figure 4.5. PSW display format.

* RR - Read Register.

  Depressing this button causes the contents of the register addressed by the Register Address Switches to be displayed on the Data Lamps.

* RM - Read Memory.

  Depressing this button causes the contents of the memory location addressed from the contents of the P-Register to be displayed on the Data Lamps. The contents of the P-Register are also incremented by 2.

* LR - Load Register.

  Depressing this button causes the value set on the sixteen Data Switches to be loaded into the register addressed by the Register Address Switches. The value is also displayed on the Data Lamps.

* LM - Load Memory.

  Depressing this button causes the value set on the sixteen Data Switches to be loaded into the memory location addressed from the contents of the P-Register. The value is also displayed on the Data Lamps and the P-Register is incremented by 2.

4.3.5 Mode Buttons

The two mode buttons are situated below Data Switches 14 and 15. They select and initiate the following modes of operation:-

* INST - Single Instruction Mode.

  Depressing this button causes the CPU to increment the contents of the P-Register, execute the instruction addressed from its contents, and then stop.

* RUN - Run Mode.

  Depressing this button causes the CPU to execute the instructions of a program commencing at the instruction addressed from the contents of the P-Register plus 2.

4.3.6 Service Buttons

There are three service buttons, listed below:-

* MC - Master Clear.

  Situated below Data Switch 0. Depressing this button raises the master-clear level throughout the system, causing a general reset of all the associated logic.

* INT - Interrupt.

  Situated below the Register Address Switches. Depressing this button raises a control panel interrupt. This button is the only control on the full panel which is operative when the Safety Key Switch of the SOP is in the LOCK position.

* IPL - Initial Program Load.

  Situated below Data Switch 10. This button provides the same automatic program loading facility as the bootstrap switch on the SOP. When the button is depressed it causes the Initial Program Loader to be loaded into central memory and the CPU to be started. Loading is carried out from the device specified by pressing the corresponding SOP switch/button (figure 4.6).

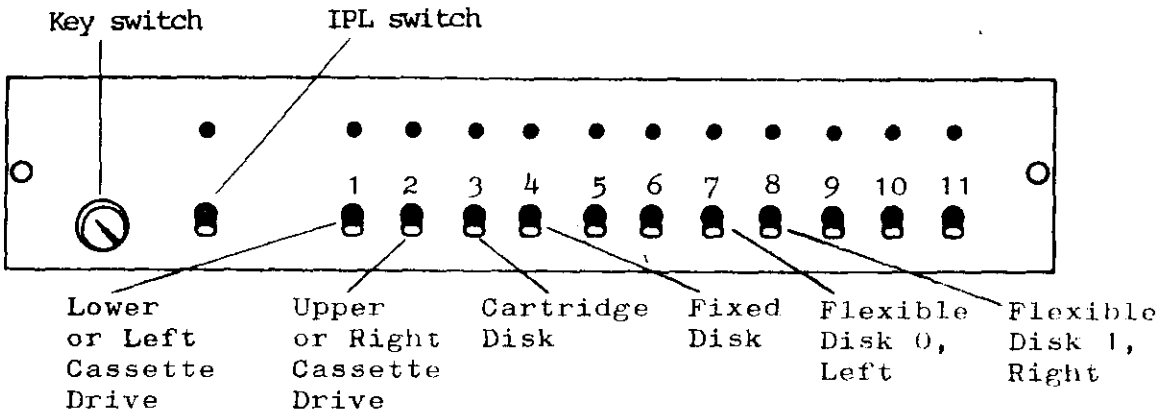

Figure 4.6. SOP switches used for program loading from various media.

4.4 COMPUTER FULL PANEL OPERATION

The full panel provides memory and register loading and display facilities, and program execution may be started and controlled manually.

4.4.1 Loading and Display Facilities

Figures 4.7 and 4.8 show the procedures for loading and displaying the contents of the general purpose registers and of memory locations. The CPU Program Status Word may be displayed by depressing the RST button.

4.4.2 Manual Program Control

In addition to the use of the IPL facility, programs may be started, checked, tested, and altered using the load and display facilities. The manual starting of any program whose start address is known is as follows:-

* Using the load register routine (figure 4.7), load register A0 with the required start address.

* If the program is to be run continuously, press the RUN button.

* If the program is to be run one instruction at a time, press the INST button.

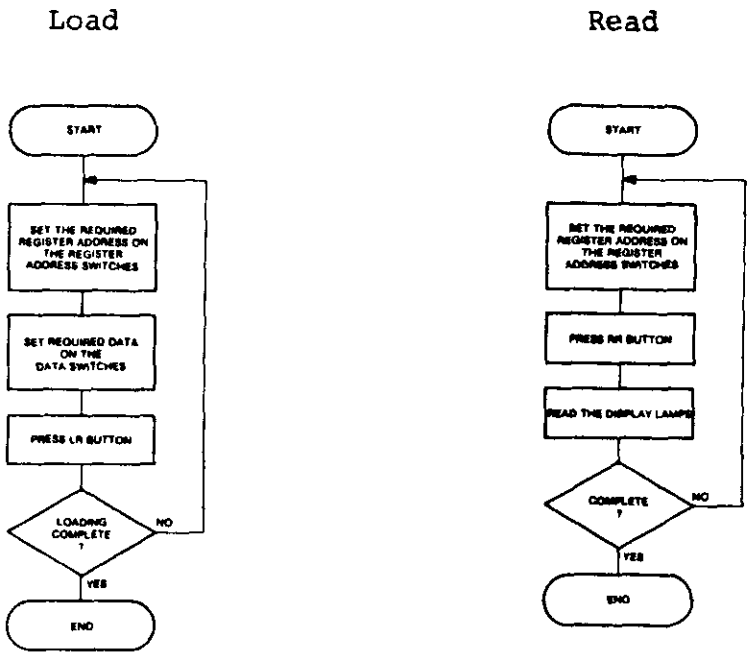

Figure 4.7. Computer Full Panel, Load and Read Register routines.

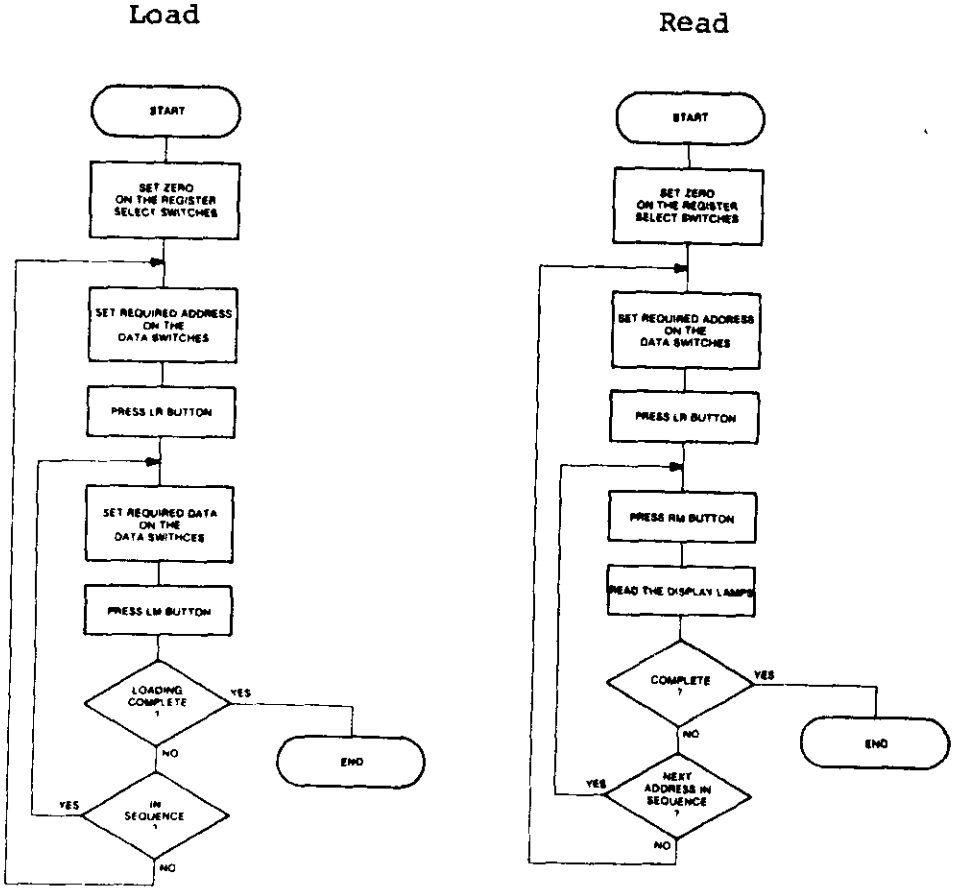

Figure 4.8. Computer Full Panel, Load and Read Memory routines.

4.5 EXTENDED CONTROL PANEL

The Extended Control Panel (figure 4.9) may be fitted to a PTS6813 machine.

This panel provides the facility for displaying an address and its contents at the same time. It also provides more extensive debugging facilities, since processing may be stopped at any address set previously on the upper row of switches. The user may then load new data if so desired.

Addressing from this panel is in terms of words.

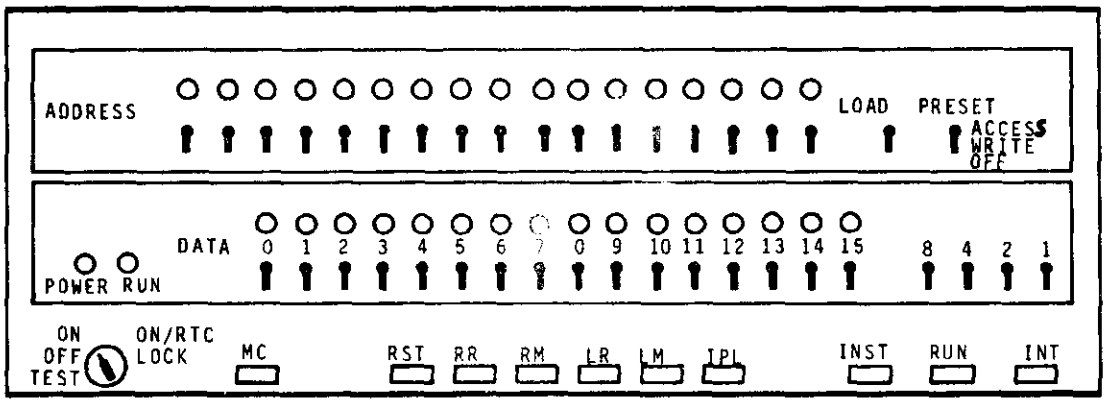

Figure 4.9. Extended Control Panel.

The functions of the displays and switches on the Extended Control Panel are as follows:-

4.5.1 Display Lamps

Seventeen lamps situated above seventeen address switches; when the computer is running, the lamps on the upper part of the panel are lit to indicate addresses, and the contents are displayed on the lower lamps. When the CPU stops, the contents of the next instruction's address is displayed on the lower lamps, and the address of the instruction on the upper lamps.

4.5.2 Address Switches

Seventeen address switches on the upper part of the panel; each switch has two positions, and they are used for loading the appropriate address. A 1 bit is loaded when a switch is in the up position.

4.5.3 LOAD Switch (spring-loaded)

Used to load an address in an address register contained in the control panel.
The required address is set on the address switches. The LOAD switch is pressed downwards and the address is displayed on the address lamps.

4.5.4 PRESET Switch

A three position switch useful for debugging purposes.

* ACCESS - stop on memory address coincidence.
  In this position the CPU stops when a physical address generated by the CPU is identical to the pattern coded on the address keys. When that address is detected, the relating instruction is executed and the CPU enters the idle state.

* WRITE - stop when writing into memory at selected address.
  In this position the CPU only stops if a store operation is performed at the location whose address was set previously on the address keys.

* OFF - disables debugging facilities described above.

4.5.5 Read Memory Procedure

1. Load the address register with the address wanted (see LOAD above).

2. Press RM button. The contents of the memory location will be displayed on the data lamps.

3. The control panel register is incremented by two and the next address is displayed on the address lamps.

Each time the RM button is pressed the address register is incremented.

Figure 4.10 shows the memory display procedure in flowchart form.

4.5.6 Load Memory Procedure

1. Load the address register with the address wanted (see LOAD above).

2. Set the value to be loaded on the data switches.

3. Press LM button.
   The value is displayed on the data lamps. The address register is incremented by 2 and displayed on the address lamps.

Figure 4.11 shows the memory loading procedure in flowchart form.

All other push-buttons and switches have the same functions as described above in the Computer Full Panel section, 4.3.

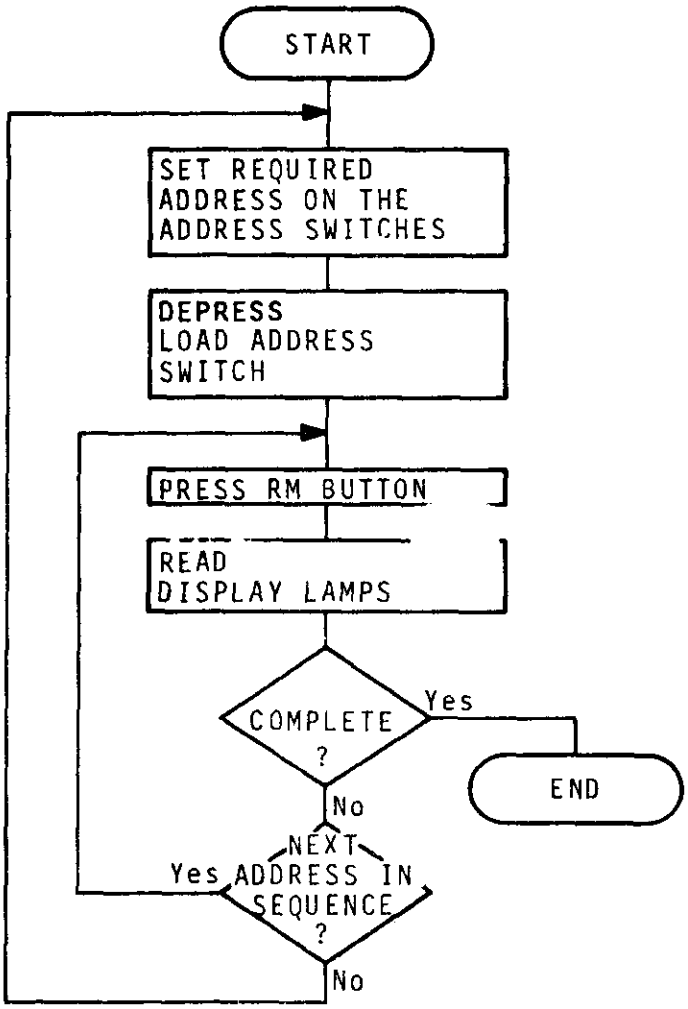

Figure 4.10. ECP procedure for displaying the contents of memory.

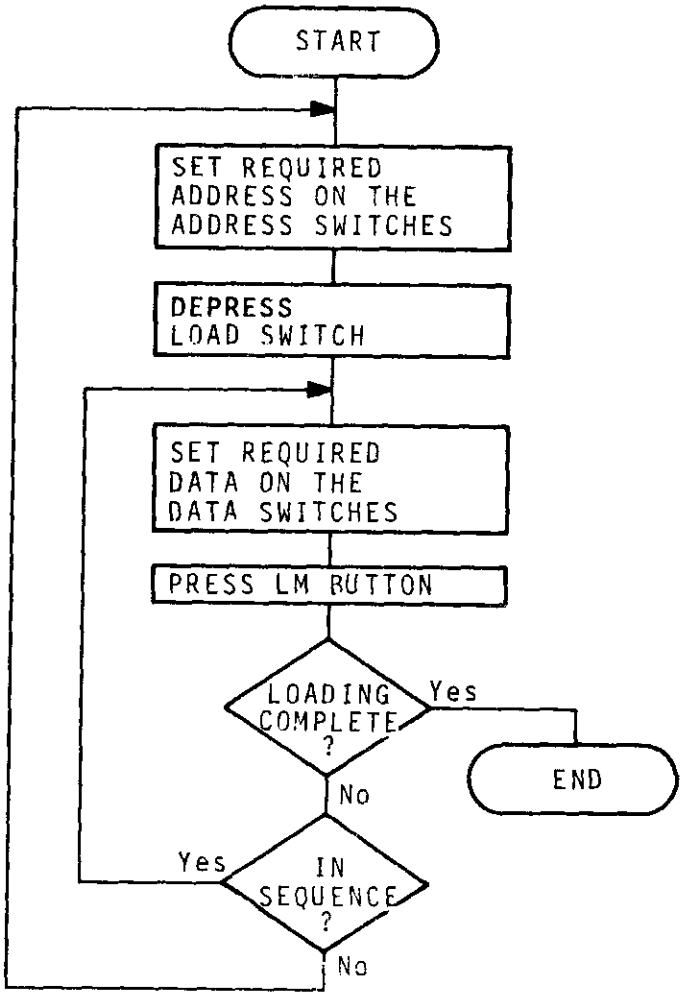

Figure 4.11. ECP procedure for loading data into memory.