2.1 GENERAL

All selector units consist essentially of a power-supply unit and a logic unit. The power-supply unit supplies both the logic unit and the attached input/output devices with the power required. The unit contains a communication section, connected to the channel unit, and up to four buffer circuits which adapt the input/output devices to the communication section.

There two types of selector unit, Selector Unit Modular Local (SUML), and Selector Unit Modular Remote (SUMR).

The device addresses and input priorities of the devices connected to the selector unit are adjustable within the selector unit.

Figure 2.1 shows typical Selector Unit configurations.

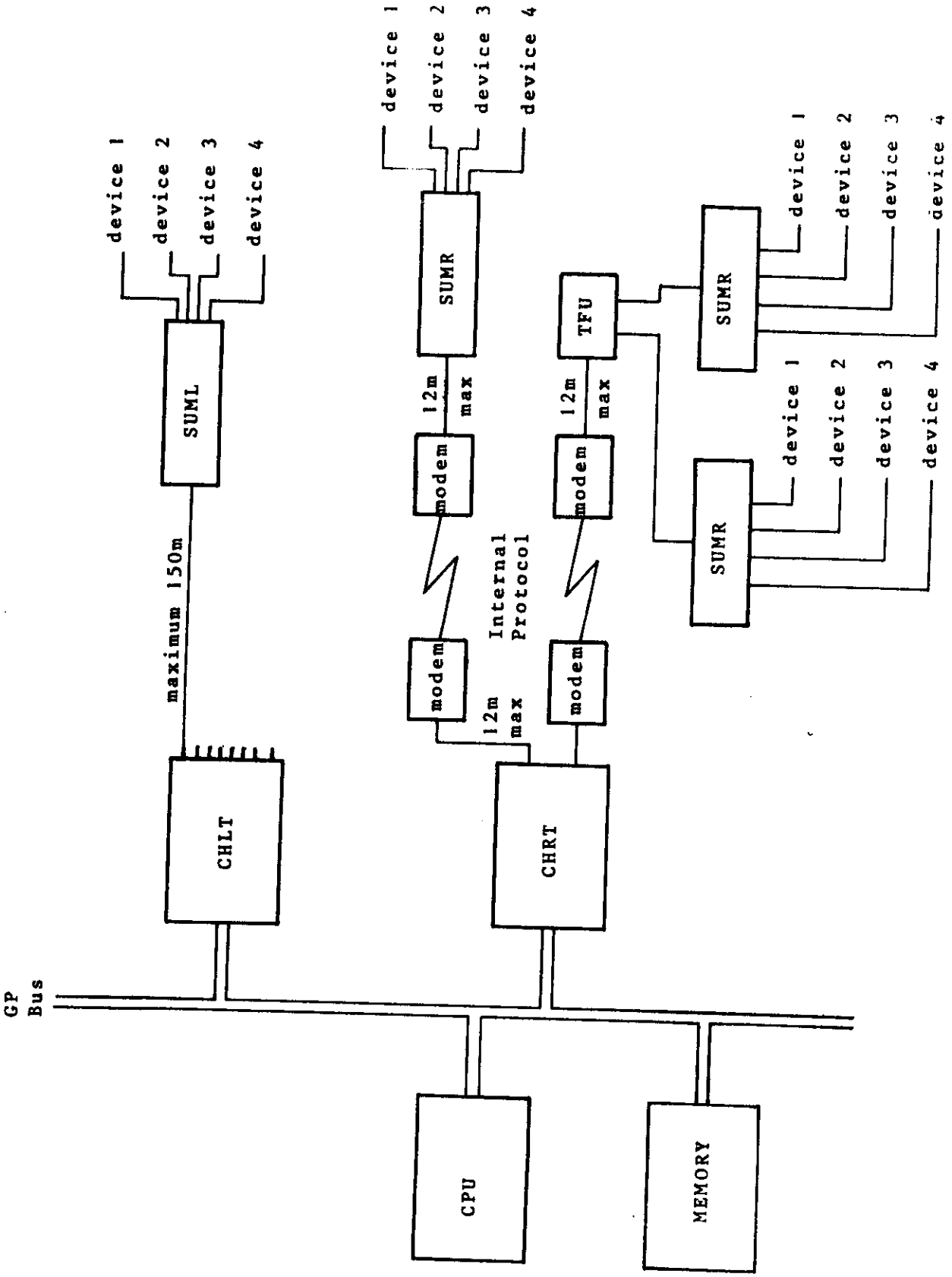


Figure 2.1. Selector Unit Configurations.

2.2 SELECTOR UNIT MODULAR LOCAL (SUML)

In this type of selector unit, up to three input/output devices can be connected through buffer circuits which are built on exchangeable plug-in adaptor boards. However, the printer buffer logic is integrated on the basic board which contains the communication section (figure 2.2).

The device addresses and the input priority levels (to the CHLT) are adjustable by means of jumpers on the adaptor boards (address selection), and on the basic board (priority selection).

Input device addresses are adjustable from 1 to 7.
Output device addresses can be 1, 2, 3 to 6 and priority-levels 1 to 4 (1 is highest priority).
Output device address 2 is always used for the print device.

Priority levels are only adjustable for Input.

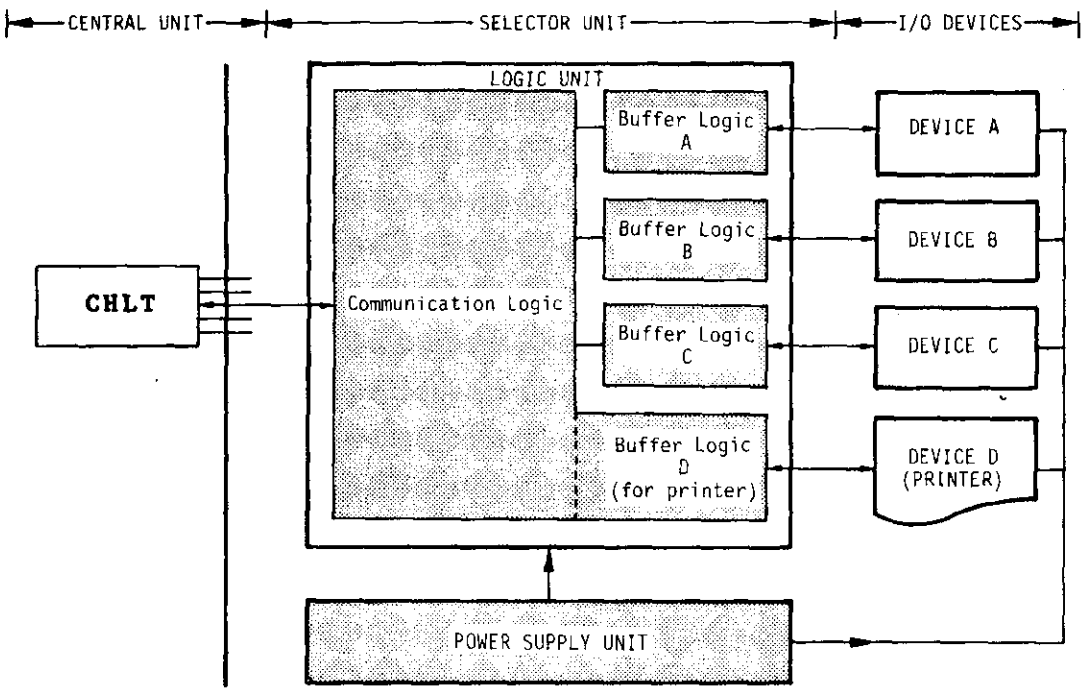


Figure 2.2. Basic structure of a modular selector unit.

ABBREVIATIONS USED IN THE FOLLOWING TEXT:-

ABC	Acknowledge Block Check.
ACK	ACKnowledge.
DIN	Data INput, from SUMR.
DOS	Data Out, Single character mode.
DOB	Data Out, Block mode.
DRD	Data Request Delayed.
DRI	Data Request Immediate.
FIFO	First In First Out.
NAK	Not AcKnowledged.
OBC	Output Block Check.
OER	Output ERror.
ROM	Read Only Memory.
SER	Selector unit ERror.
SUML	Selector Unit Modular, Local.
SUMR	Selector Unit Modular, Remote.
STD	STatus of Device.
SYN	SYNchronization character (X'55').
TFU	TransFer Unit.

2.2.1 Operation in Brief of SUML

2.2.1.1 Layout of Output Messages

* Start Bit.

A complete output message from the CPU to CHLT consists of two bytes, an address byte and a data byte (figure 2.3). The first bit of the message is used as the start bit during the serial transfer between the CHLT and selector unit. The bit is set by CHLT hardware.

* Addresses and Data.

After the start bit, a 3-bit device address and a 3-bit terminal address are present, which specify respectively the terminal (plug on CHLT to which selector unit is connected), and the device (device on selector unit).

The last bit of the address character is reserved for a parity bit which is used only during the serial transfer between CHLT and selector unit. When the message leaves the CPU this bit and the first bit of the data character are not significant.

* Message from CPU to CHLT.

When the output message from the CPU reaches the CHLT, the CHLT will supplement the address and data characters with odd parity bits, and set the start bit to one.

When the CHLT then starts the serial transfer to the addressed terminal (selector unit), the 3-bit terminal address has served its purpose and is cleared (figure 2.3).

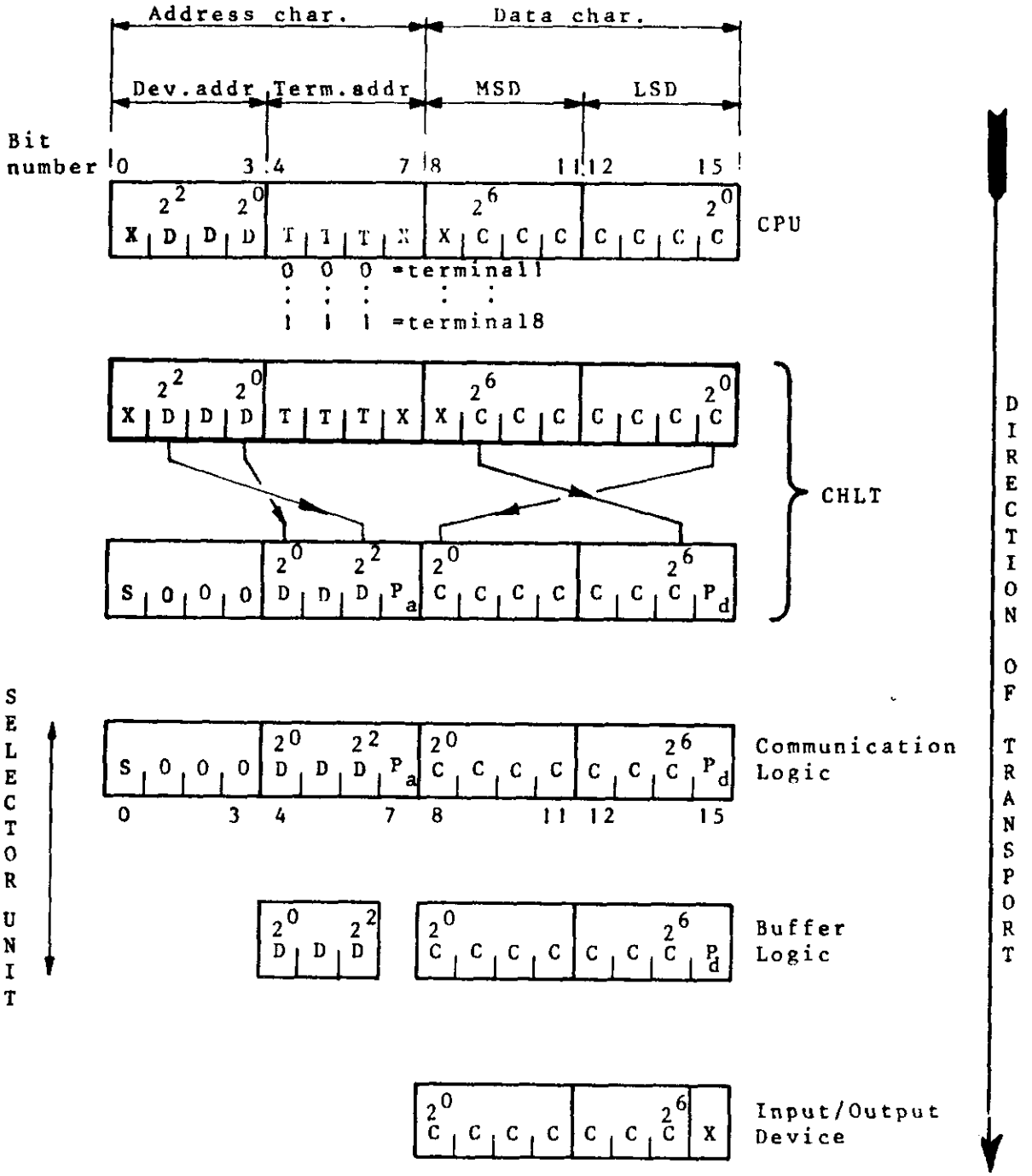
* Message from CHLT to SUML.

The output message from the CHLT is received by the communication logic of the selector unit, where the parity is checked. If the address parity is correct the data character will be passed to the buffer logic of the addressed output device (figure 2.3).

The 3-bit device address is passed on to the buffer circuits, which are each provided with address decoders.

* Character from SUML to Device.

The character code received by the addressed buffer logic will be supplied unchanged to the output device, provided that the communication logic finds that the data character has correct parity.



MSD - Most Significant Digits. LSD - Least Significant Digits.

D - Device Addr. Bits.
T - Terminal No. Bits.
C - Character Bits.

S - Start Bit.
P_a - Addr. Parity Bit.
P_d - Data Parity Bit.

X - Not Significant.

Figure 2.3. Message Transfer between CPU, CHLT, SUML and I/O devices.

2.2.1.2 Layout of Input Messages

Input messages are transferred from selector unit to channel unit and have the same layout as output messages.

* Character from Device to Selector Unit.

The character codes supplied by input devices are first taken into the appropriate buffer circuits in the selector unit, where the device address is encoded. The characters are then, in accordance with input priority, transferred one by one to the communication logic, which generates the required data parity bits and controls the transfer to the CHLT.

* Message from SUML to CHLT and CPU.

When the communication logic is loaded with the information from the buffer logic, the input message (for CHLT) is completed by setting:-

* start bit to one.
* terminal address to zero.
* odd parity for the address byte and character byte..

The serial transfer to the CHLT starts when the communication logic is polled by the CHLT. When the message is received by the CHLT it clears the parity bits and inserts the terminal address before the final transfer to the CPU takes place.

* Administrative Messages from SUML to CHLT.

Apart from the input messages which are supplied by the input devices, there are also some administrative input messages for the CHLT, which are supplied by the selector unit.
These messages have the same layout as shown in figure 2.3. However,the device address in the address byte will also be cleared.

A data character in an administrative input message can contain the following information:-

* Code X'83'. (X'03' when reaching CPU).
  Power failure , which indicates that the selector unit power has just been switched on or has just recovered after a failure.

* Code X'85'. (X'05' when reaching CPU).
  NAK , which indicates that the last character transmitted to the SUML has not been acknowledged, due to a parity error or the device not being in output mode.
  Retransmission will be performed by the software.

* Code X'07'. (X'07' when reaching CPU).
  ACK , which indicates that the message last transmitted to the SUML has been acknowledged.

* Code X'9B'. (X'1B' when reaching CPU).
  Input Trouble , which indicates that four consecutive attempts by the SUML to transfer a character to the CHLT have failed.
  (No hardware controlled ACK has been received from the CHLT).

2.3 SELECTOR UNIT MODULAR REMOTE (SUMR)

In this type of selector unit the communication logic consists of a common block and a printer interface located on a basic board, to which three additional interface boards can be connected in order to adapt three devices (figure 2.4).

The use of a Transfer Unit (TFU) enables two SUMR's to be connected to the same line, otherwise only one may be connected.

Each adaptor board is given a specific device address, selected by means of removable jumpers on the adaptor boards.

Table 1 shows which input and output addresses are used for various devices.

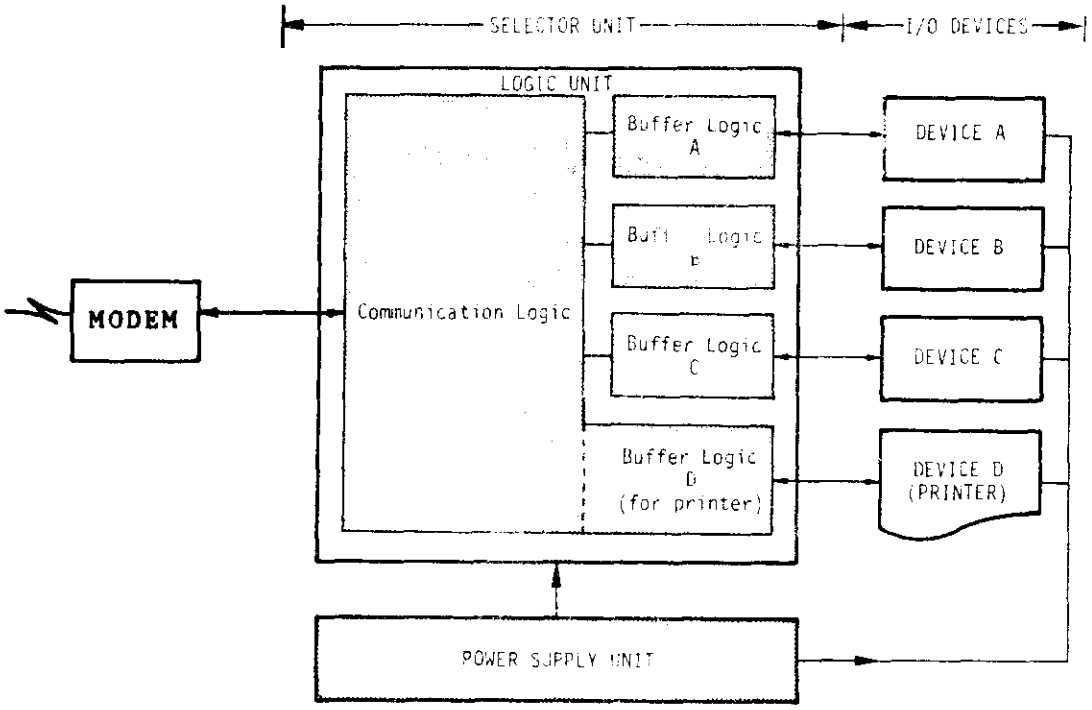


Figure 2.4. The structure of the Selector Unit Modular Remote.

DEVICE	MAIN ADDRESS	RESERVE ADDRESS
Permanent printer interface	2	-
Keyboard	1	5
Numeric indicator	4	3
Signal display	3	5
Printer (on optional adaptor board)	3	6
Display (VDU)	4	3
Other devices	6	any of 1 thru 5

Table 1. Device Addresses.

Input devices should be arranged in priority succession depending on input rate and access time for each device. The permanent printer interface and the three adaptor boards can be given any of four levels, selected by jumpers in a selection field in the communication logic of the SUMR. The priority level is applicable to the adaptor board position and not to the adaptor board itself. (figure 2.4).

The permanent printer interface, which always has device address 2, contains a 40 character FIFO buffer and logic for indicating printer status, e.g. printer operable, or voucher/passbook correctly inserted.

There is also an operational ROM package to generate two triple spaced characters usually used to print a trade mark. The generation is started by codes X'13' and X'14' respectively.

2.3.1 Operation in Brief of SUMR

2.3.1.1 General.

A SUMR transfers data asynchronously via a modem in full duplex mode between a CHRT and terminal devices.

2.3.1.2 Line Procedure.

Data to/from the SUMR is transferred on the line either character-by-character with demand of acknowledgement for each character, or block-by-block where the acknowledgment is checked after a complete block has been transferred. Block transmission and character transmission can be mixed on the line. Block transmission gives a higher transfer rate than character transmission; the transmission procedure is selected by software for output from a CHRT, and by a jumper on the relevant adaptor board for input.

If a character or block is not acknowledged because of parity failure during output transfer, it is retransmitted under program control. If there is parity failure during input to the CHRT for character-by-character transmission, then the character is retransmitted by the SUMR. For block transmission it depends whether or not the device is able to retransmit the block.

The SUMR contains logic for both Vertical and Longitudinal Redundancy Checks (VRC and LRC) on output from a CHRT. For input to a CHRT, either character or block transmission, a VRC is performed by the SUMR, and the data character is supplemented with an odd parity bit.

2.3.1.3 Message Layout.

Both input and output messages from/to a SUMR have a format of either 16 bits or 9 bits.

The 16 bit format (figure 2.5) is called data format, and the 9 bit format (figure 2.6) is called receipt format because ACK and NAK have that length.

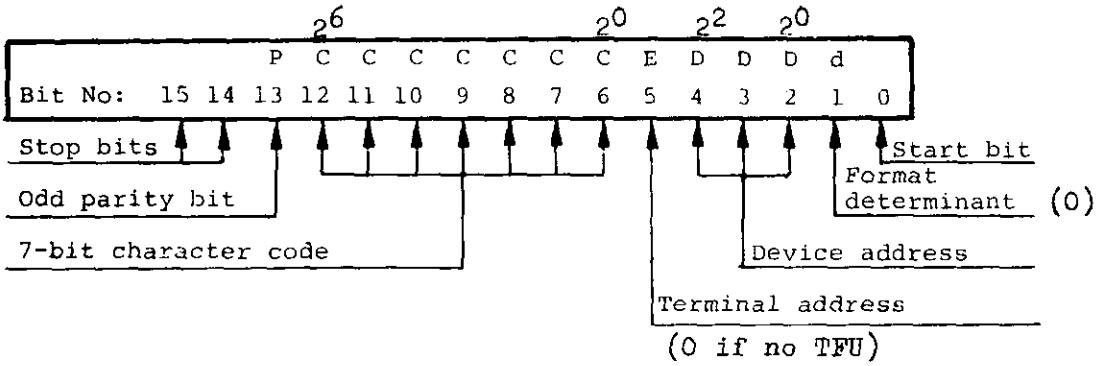


Figure 2.5. Data Format message.

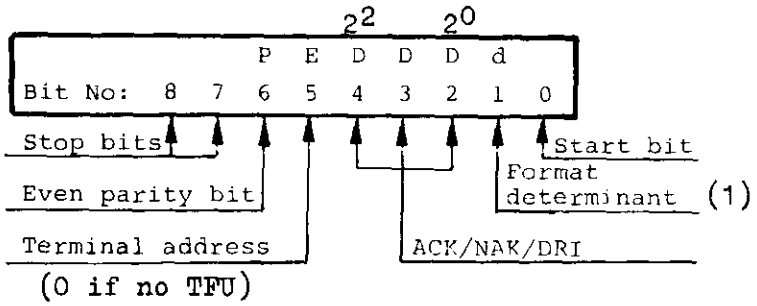


Figure 2.6. Receipt Format message.

2.3.1.4 Messages To and From the SUMR.

The formats shown in figure 2.7 are as they appear when measured on the line.

1. Output to SUMR, Data formats.

Message	St	d	D	D	D	E	C	C	C	C	C	C	C	P	Sp	Sp	
SYN	0	0	1	1	1	0/1	1	0	1	0	1	0	1	0/1	1	1	Each 500 ms*
Dos	0	0	1	---	6	0/1	DATAZONE							0/1	1	1	Single character
DOB	0	0	1	---	6	0/1	DATAZONE							0/1	1	1	Blockwise
OBC	0	0	0	0	0	0/1	DATAZONE							0/1	1	1	Read and clear LRC-VRC

*** If no other communication within the 500ms.**

2. Output to SUMR, Receipt formats.

Message	St	d	D	D	D	E	P	Sp	Sp	
ACK_{in}	0	1	1	1	1	0/1	0/1	1	1	Data in, acknowledge
NAK_{in}	0	1	0	0	0	0/1	0/1	1	1	Data in, not acknowledge

3. Input from SUMR, Data formats.

Message	St	d	D	D	D	E	C	C	C	C	C	C	C	P	Sp	Sp	
DIN	0	0	1	---	7	0/1	DATAZONE							0/1	1	1	Data from input device
STD	0	0	1	---	7	0/1	DATAZONE							0/1	1	1	Same as DIN but the program recognizes that STD/DRD comes from output devices
DRD	0	0	1	---	6	0/1	0	0	0	0	0	0	0	0/1	1	1	
ABC	0	0	0	0	0	0/1	0	0/1	0/1	1	0	0	0	0/1	1	1	VRC/LRC status
SER	0	0	0	0	0	0/1	1	1	0	0	0	0	0	0/1	1	1	Selector unit error

$2^0 \rightarrow 2^2$ $2^0 \rightarrow 2^6$

4. Input from SUMR, Receipt format.

Message	St	d	D	D	D	E	P	Sp	Sp	
ACK_{out}	0	1	1	1	1	0/1	0/1	1	1	Data out, acknowledge
NAK_{out}	0	1	0	0	0	0/1	0/1	1	1	Data out, not acknowledge
DRI	0	1	1	---	6	0/1	0/1	1	1	ACK and data request from an output device

Figure 2.7. Formats of Messages to and from the SUMR.

2.3.1.5 Output Messages from CPU to CHRT.

There are three kinds of output messages, shown in figure 2.8.

* A data message to an output device (1-6).
* An Output Block Control (OBC) message.
* A Synchronization (SYN) message.

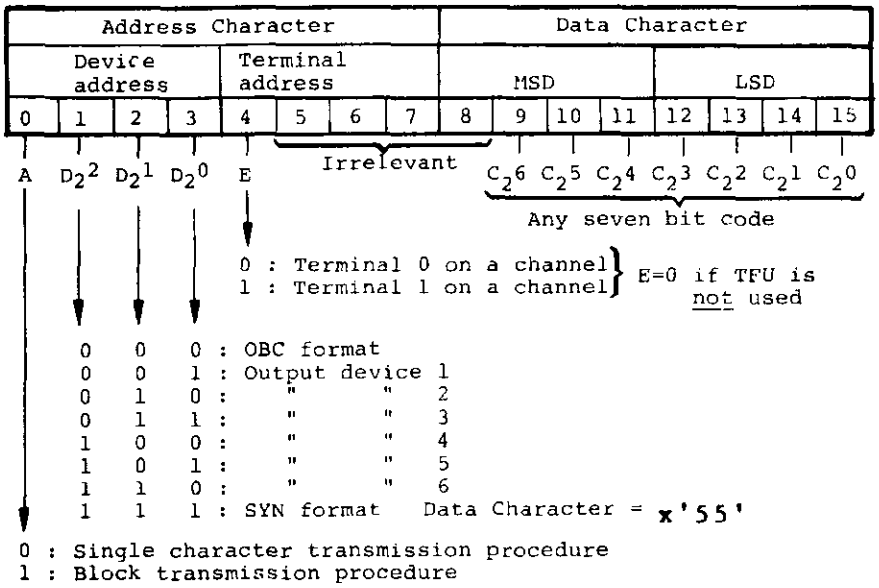


Figure 2.8. Layout of output messages from CPU to CHRT.

2.3.1.6 Input Messages from CHRT to CPU.

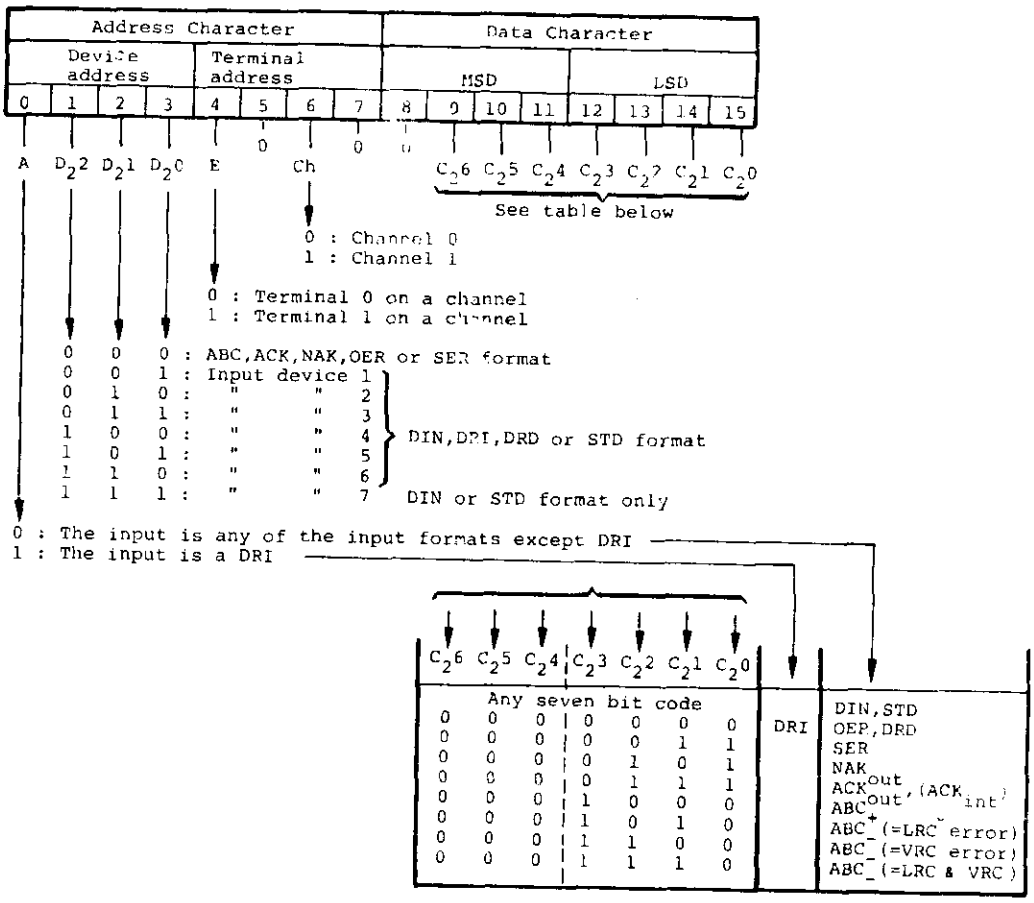


Figure 2.9. Layout of Input Messages from CHRT to CPU.

Input messages, shown in figure 2.9, can be divided into four basic types.

* data messages , which are either Data INput (DIN) messages from an input device (1-7), or STatus information from an input or output Device (STD),(1-7).

* data request messages , either 'Data Request Immediate' (DRI) which replaces ACK from the same output device, or 'Data Request Delayed' (DRD).

* receipt messages , like ACK and NAK, or 'Acknowledge Block Control' (ABC) which is the reply to an OBC message.

* error messages , which indicate 'Selector Unit Error' (SER) or 'Output Error' (OER) if the CHRT does not receive a reply within 100 ms.

Note A characteristic of receipt and error messages is that the Device Address is cleared.

2.3.1.7 Transfer Principle.

For every data message transferred between a SUMR and a CHRT, or vice versa, a receipt message is sent in the opposite direction. This applies to both character and block transmission.

During block transmission the receipt significance is omitted, but there are circuits to check that there is a reply for every message transmitted.

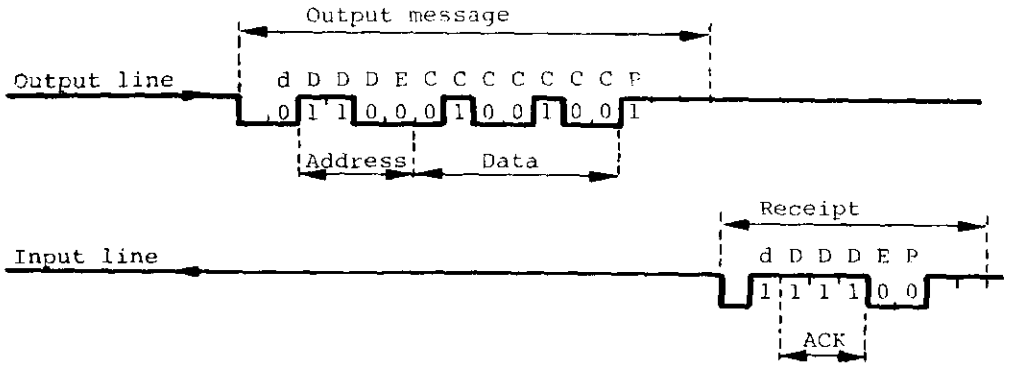


Figure 2.10. Output message with receipt, ACK or NAK.

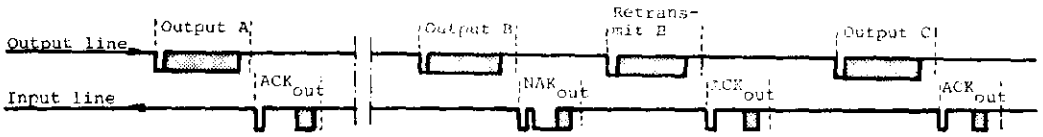


Figure 2.11. Single character output transmission.

Figure 2.11 shows an example of single character transmission of three data characters, namely A, B, and C. The SUMR detects a parity failure in character B, and replies 'NAK', which results in a retransmission of the character by the system software.

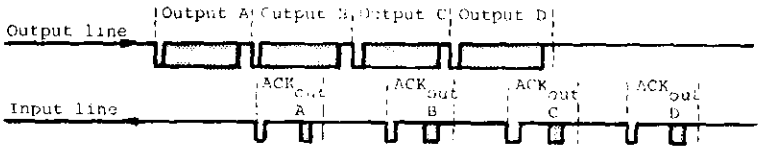


Figure 2.12. Block output transmission.

In block transmission, figure 2.12, the CHRT does not have to wait for the receipt of the previous message before the next one is transmitted to the SUMR (this is not applicable to printers).

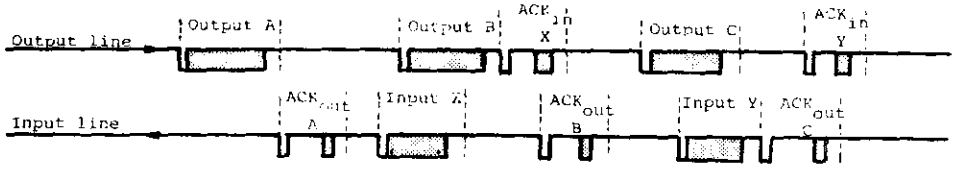


Figure 2.13. Simultaneous output and input, character transmission.

From figure 2.13 it can be seen that data messages and replies may be mixed if simultaneous input and output transmission occurs.

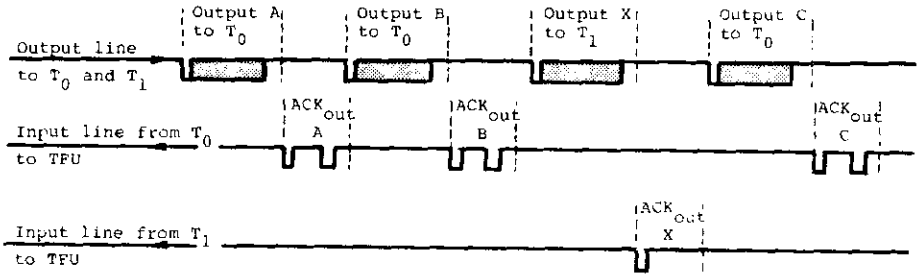


Figure 2.14. Mixed output to Terminal 0 and Terminal 1.

If two SUMR's are connected to the same telephone line via a transfer unit (TFU), data is sent to both terminals at the same time, as shown in figure 2.14. Both SUMR's receive the messages, but only the one whose identity corresponds to the value of bit E replies with ACK or NAK.

Note: A new character can not be transmitted until the previous one is received. Data is sent either to one terminal or to the other.

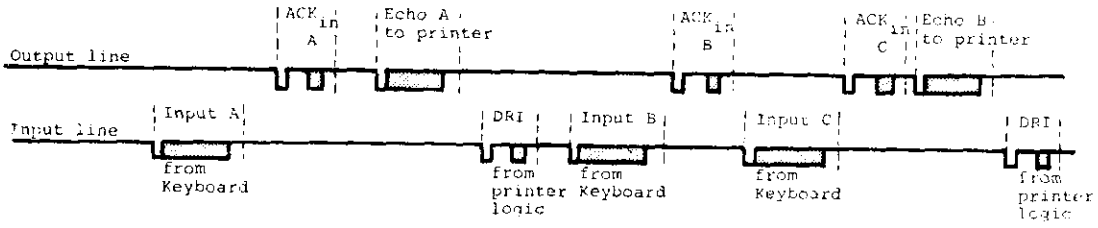


Figure 2.15. Example of Echo.

Figure 2.15 shows an example of input data from a keyboard and the 'echo' of the same data sent back to a printer. The usual ACK is replaced by a 9-bit receipt message, Data Request Immediate (DRI) which means ACK and Data Request.

Figure 2.15 also shows that several characters from the keyboard may be stored in the computer before they are echoed back to the terminal printer.

The selector unit error function, SER, includes the steps to be taken when an error situation occurs and a recovery of SUMR logic is needed.

SER handles the following situations:-

* Power-on in SUMR.
* Short power break (dip in +5V) in SUMR.
* Power-on in a device having a power supply of its own.
* Carrier missing from modem.
* Time-out at transmission attempt.

The last point only inhibits input from connected devices but the other four cause a general terminal reset.

All five situations set a flip-flop which, when the error situation clears, initiates transmission of an error status message, SER (figure 2.16), which is loaded into the transmit buffer via a multiplexer.

Sp	Sp	P	C 2^6	C 2^5	C 2^4	C 2^3	C 2^2	C 2^1	C 2^0	E	D 2^2	D 2^1	D 2^0	d	St
1	1	X	0	0	0	0	0	1	1	X	0	0	0	0	0

Figure 2.16. A SER message.

A retransmission of SER is initiated, besides the usual retransmission at NAK, if an ACK is not received within the 'Time-out' period, 250mS.

When ACK is received the SUMR returns to normal status.

The various I/O procedures are illustrated in figures 2.17 to 2.22, and an outline of the internal structure of a Channel Unit in figure 2.23.

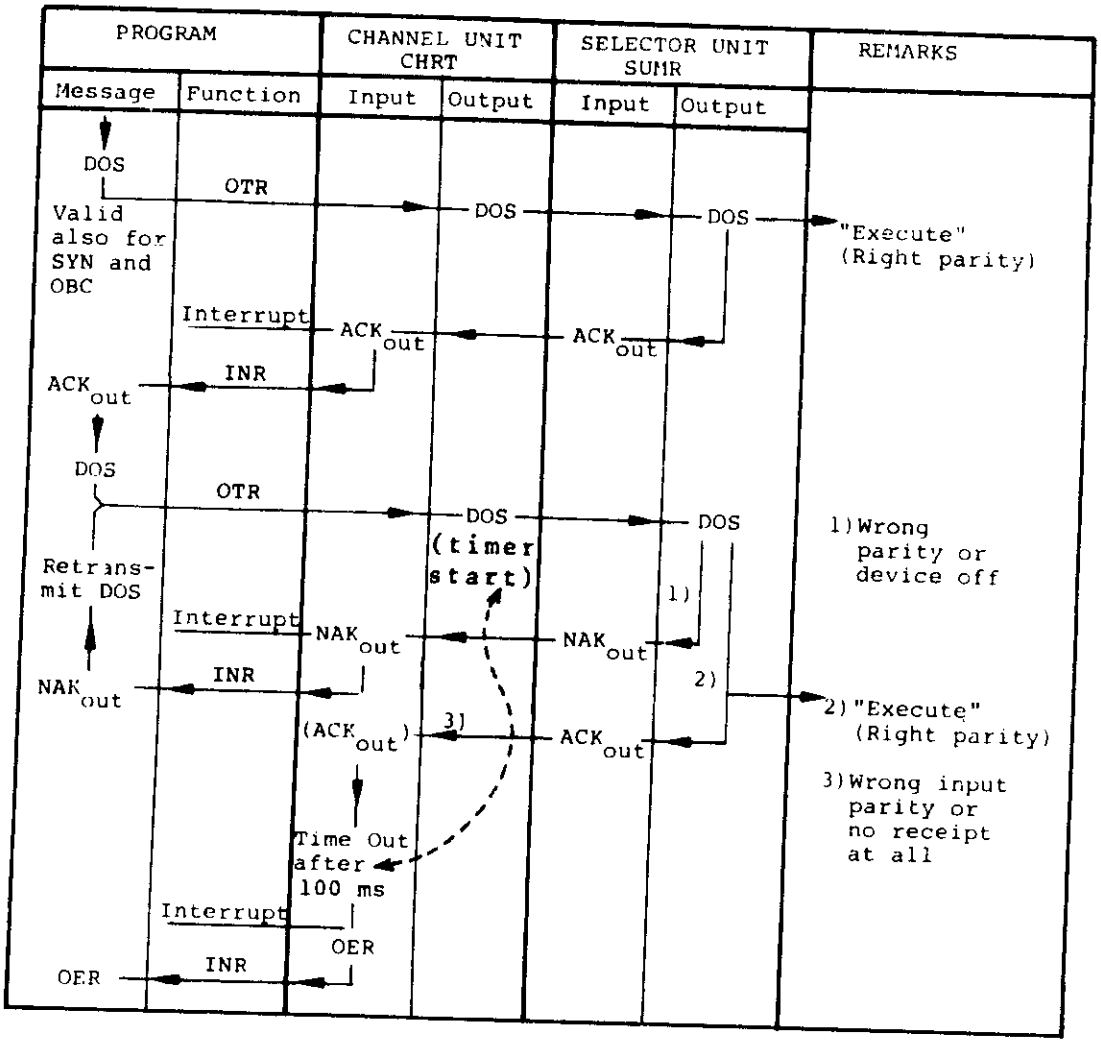


Figure 2.17. Character-by-character Output Procedure; no Data Request.

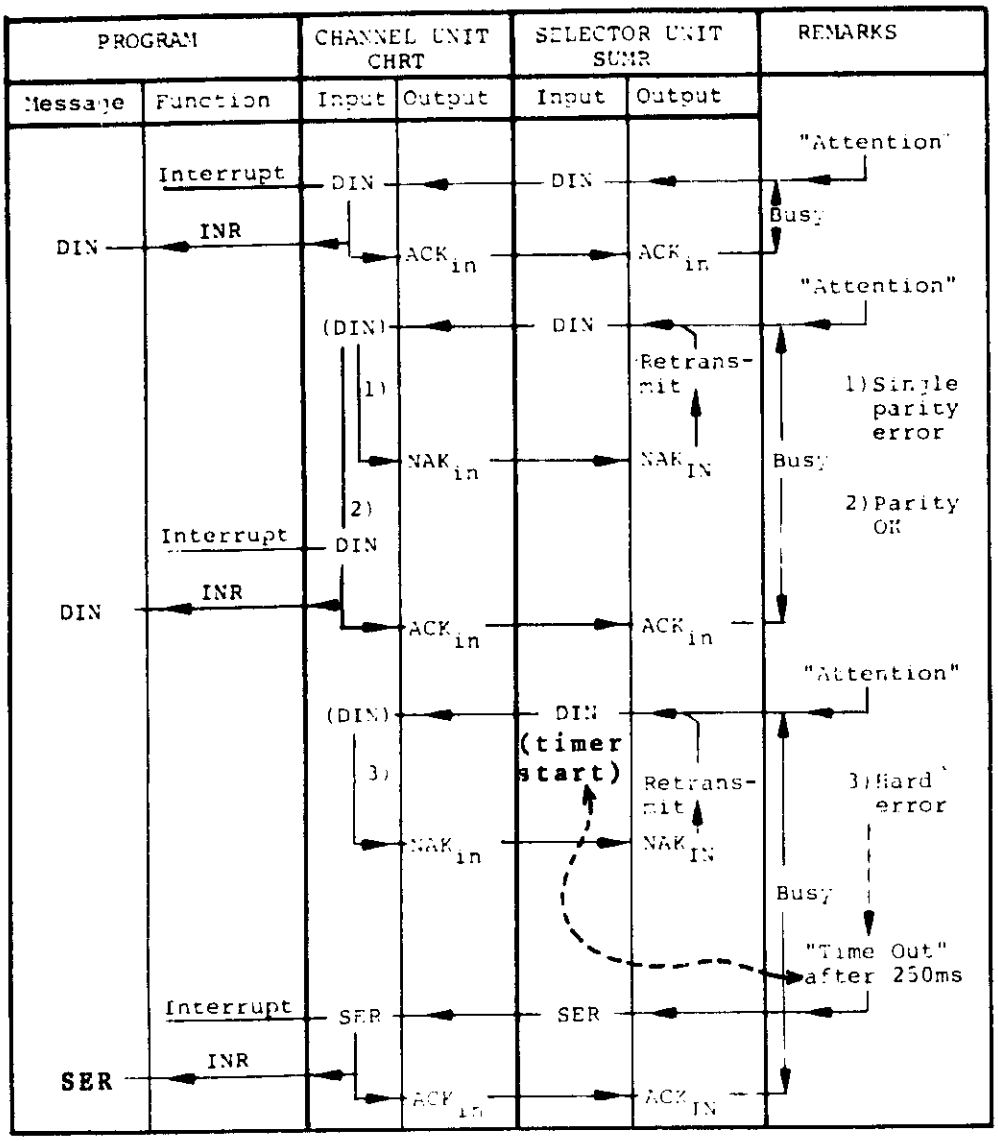


Figure 2.18. Character-by-character Input Procedure.

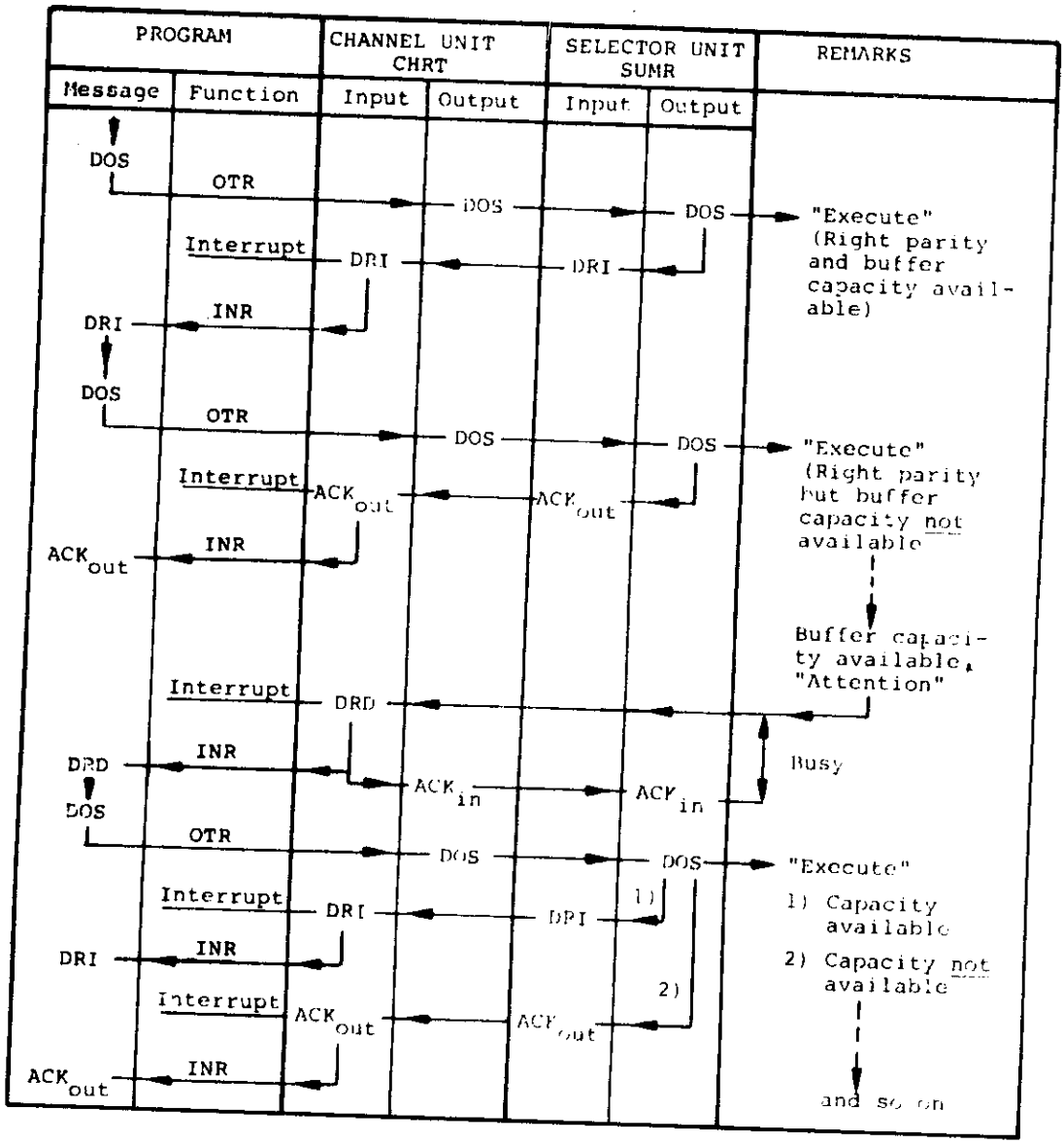


Figure 2.19. Character-by-character Output Procedure with Data Request.

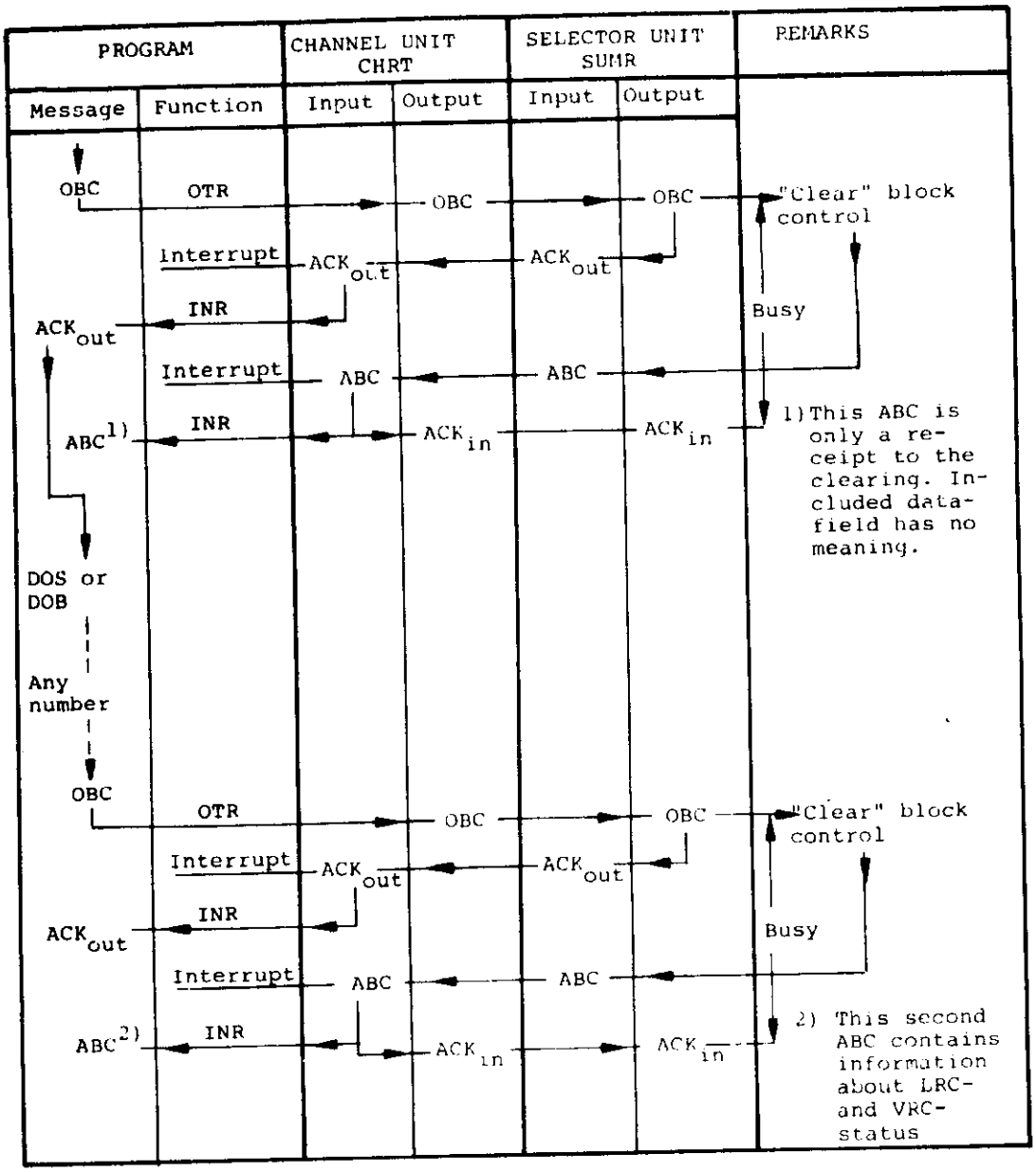


Figure 2.20. Output Procedure with OBC and ABC.

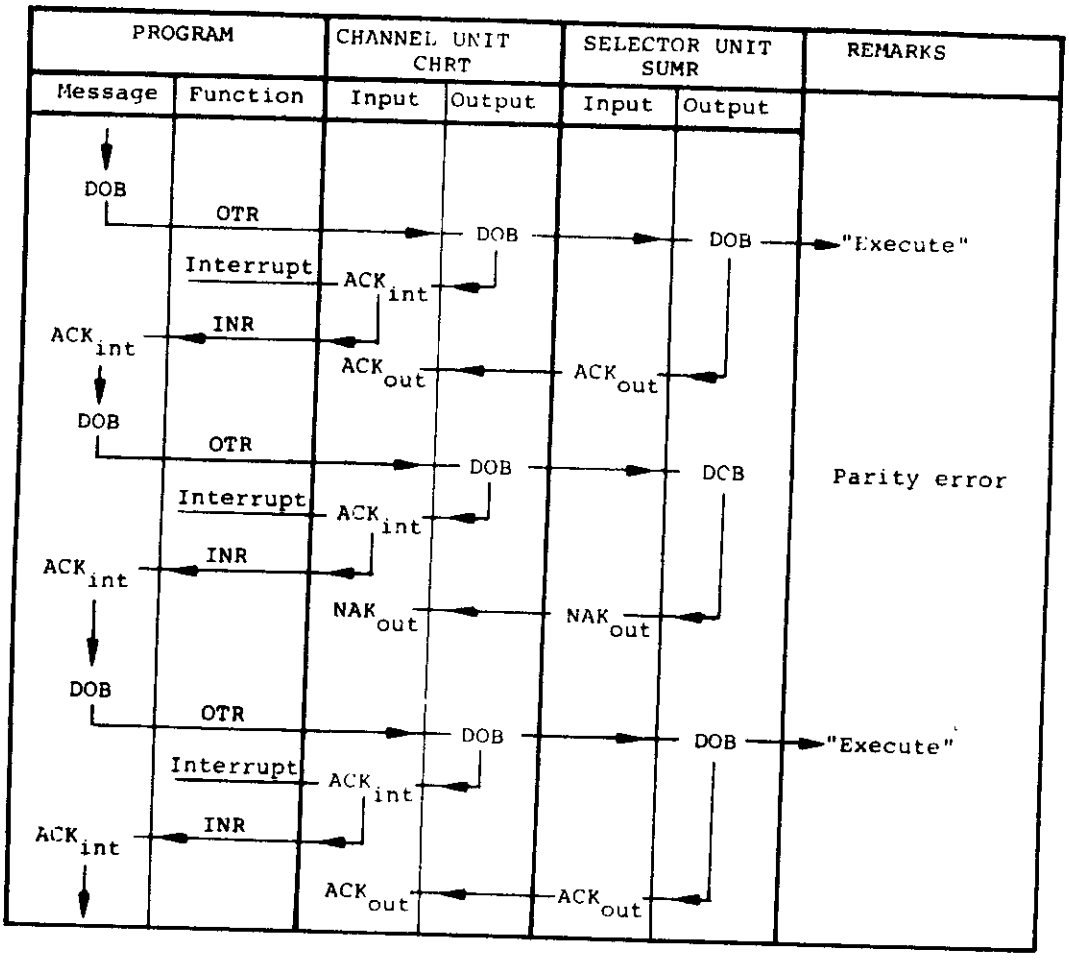


Figure 2.21. Block Output Procedure.

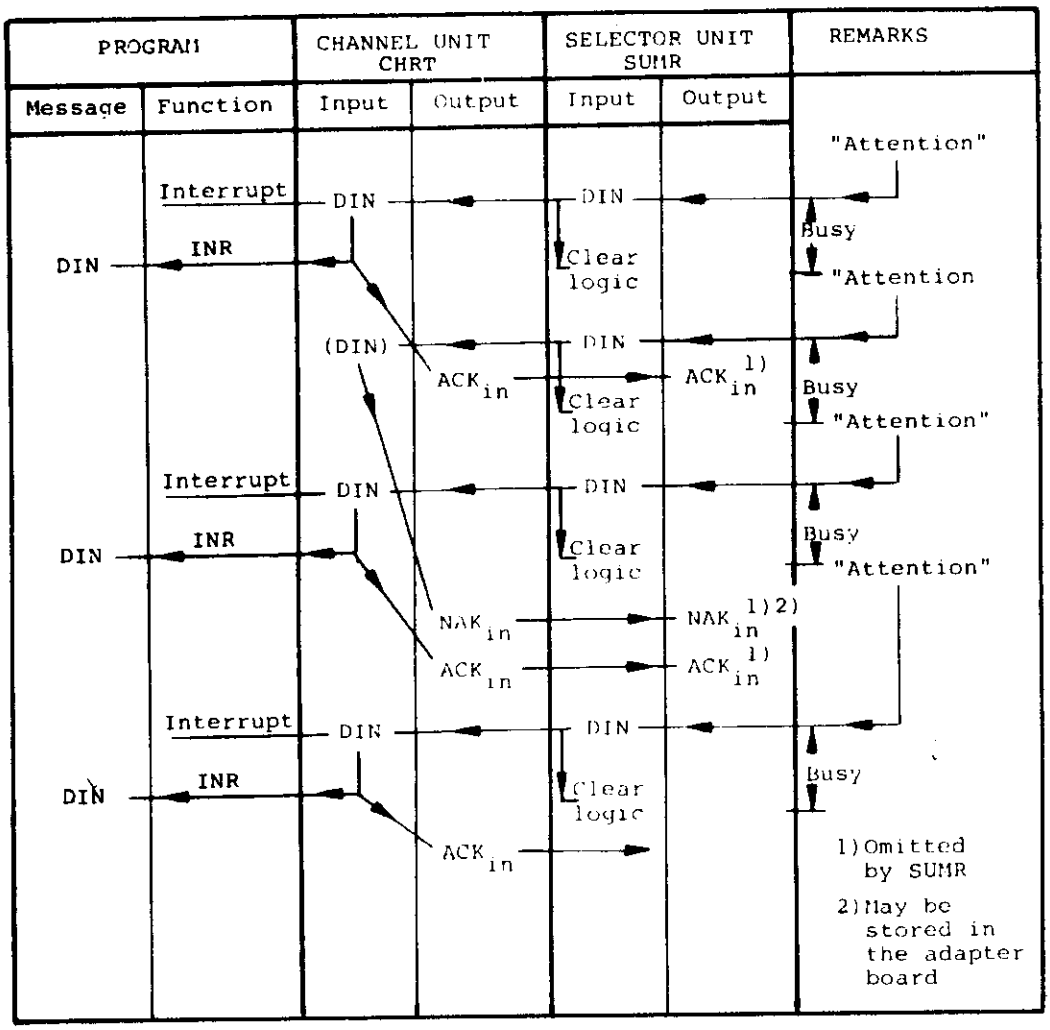


Figure 2.22. Block Input Procedure.

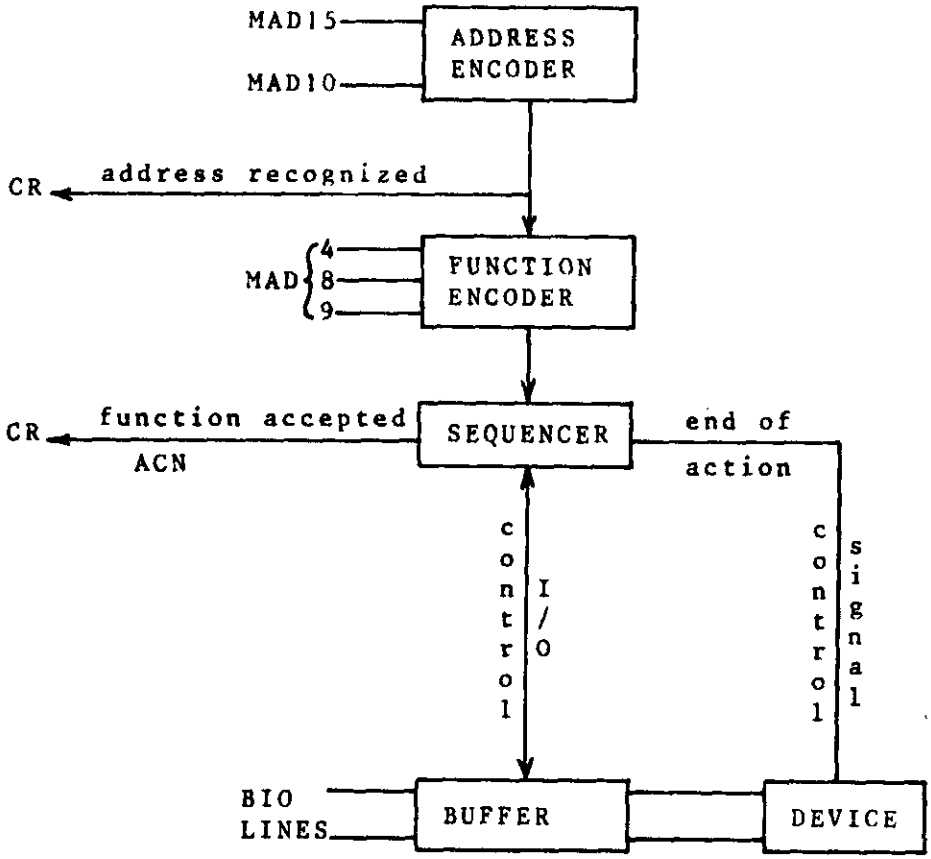


Figure 2.23. Channel Unit Internals.