10.1 CONFIGURATION

As seen in chapter 9, the operation of the Programmed Channel imposes a load upon the CPU because it has to execute instructions in order to effect the required transfers. The Input Output Processor (IOP) relieves the CPU of this load by performing the data transfers in its hardware. This offers a faster method of block data transfer between memory and peripherals, and allows the CPU, after initializing the IOP, to continue processing while the I/O is handled by the IOP. The G.P. Bus remains the data path used. Initialization of the IOP is carried out by the CPU using the ordinary programmed channel.

Channel unit states and sequences are as described for the programmed channel in Chapter 9 except that the interrupt raised in exchange state is replaced by a 'break' signal wired directly to the IOP from a channel unit. Figure 10.1 shows that, when the programmed channel is used, the wait and exchange state interrupts are wired together. When an IOP is used these two signals are separated, and the exchange state interrupt is wired directly to the IOP and known as a 'break', as shown in figure 10.2.

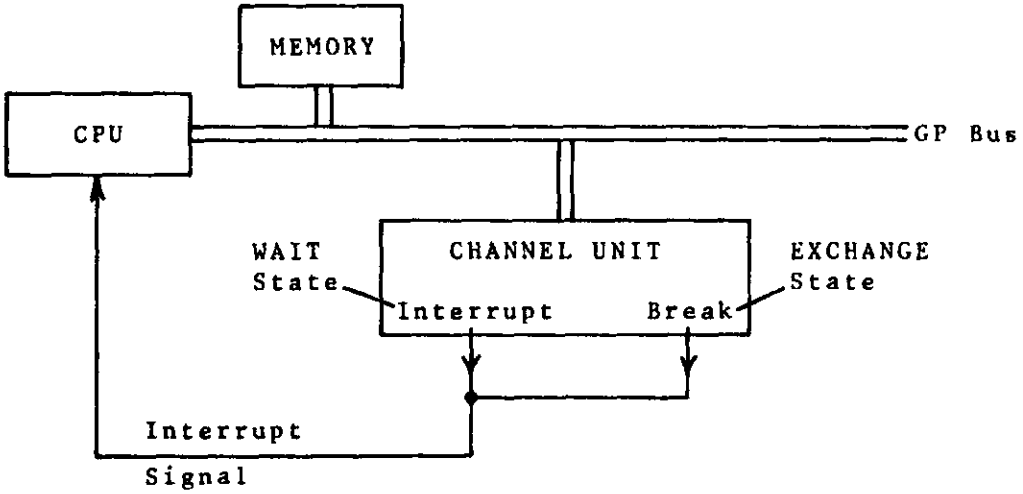

Figure 10.1. Channel Unit Interrupt Lines, no IOP.

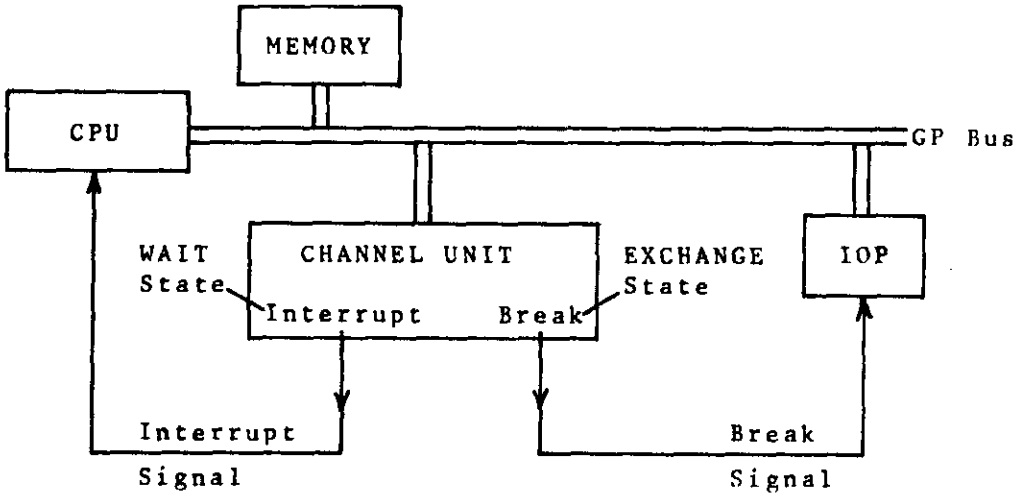

Figure 10.2. Channel Unit Interrupt Lines with IOP.

Up to 8 IOP's may be configured in a PTS system, each of which is able to control up to 8 channel units. Each IOP is known as a channel, and its 8 subdivisions are known as sub-channels. Associated with each sub-channel is a pair of 16-bit registers which are used to hold information relating to the transfer to be carried out by that sub-channel and its channel unit. These registers are referred to as control registers and they hold the transfer parameters which are used and updated by the IOP during transfer operations.

Sub-channels are allocated priorities from 0 thru 7 so that, in the event that more than one break signal is present at a particular moment, the IOP deals with the channel unit having the highest priority break signal outstanding, 0 being the highest priority level. The address of a channel unit which is connected to an IOP consists of 6 bits as shown in figure 10.3.

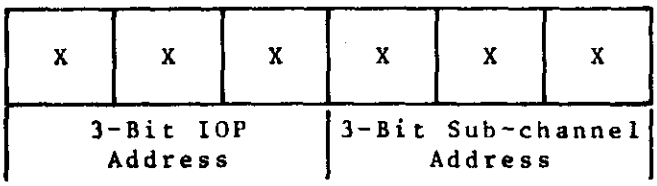

Figure 10.3. Address of a Channel Unit attached to an IOP.

10.2 INSTRUCTIONS AND CONTROL WORDS

Before a transfer is initiated the two registers in the IOP must be correctly set up.

Two instructions are available to write to or read from the control registers in the IOP. They are restricted to use in system mode, and are as follows:-

* WER Write External Register.
  The contents of a specified CPU Register are set into a specified IOP Register.

* RER Read External Register.
  The contents of a specified IOP Register are set into a specified CPU Register.

Layouts of these instructions are shown in figure 10.4, and those of the Control Words in figure 10.5.

In figure 10.4, Channel Address is the address of the IOP, of which there may be 8 in the system, and Sub-channel Address is the priority level of the channel unit which is to be used in the transfer. The CPU register involved in the operation is defined by the 3 bits, R.

WER is used in the setting up of an IOP for a transfer, and RER to check the control words at transfer end, or in the event of an error.

Any or all of the 8 sub-channels in an IOP may be in use at a time, and there is no need to check the status of any sub-channel before using the IOP, except the sub-channel which it is intended to activate. The status of the desired sub-channel should always be checked because a WER instruction is always actioned by the CPU, even if the sub-channel is already busy, and this would result in any transfer in progress being corrupted.

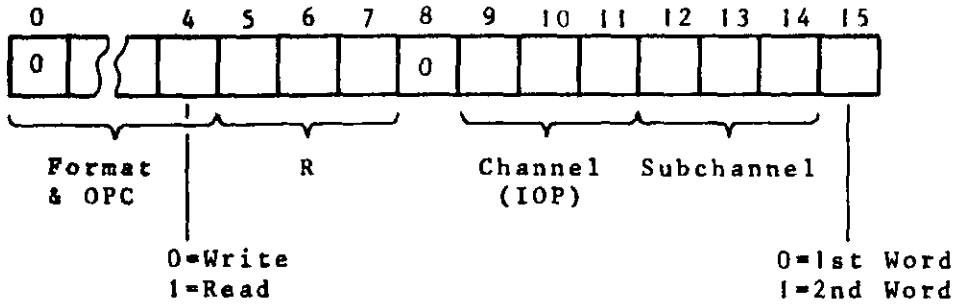

Figure 10.4. Layouts of WER and RER instructions.

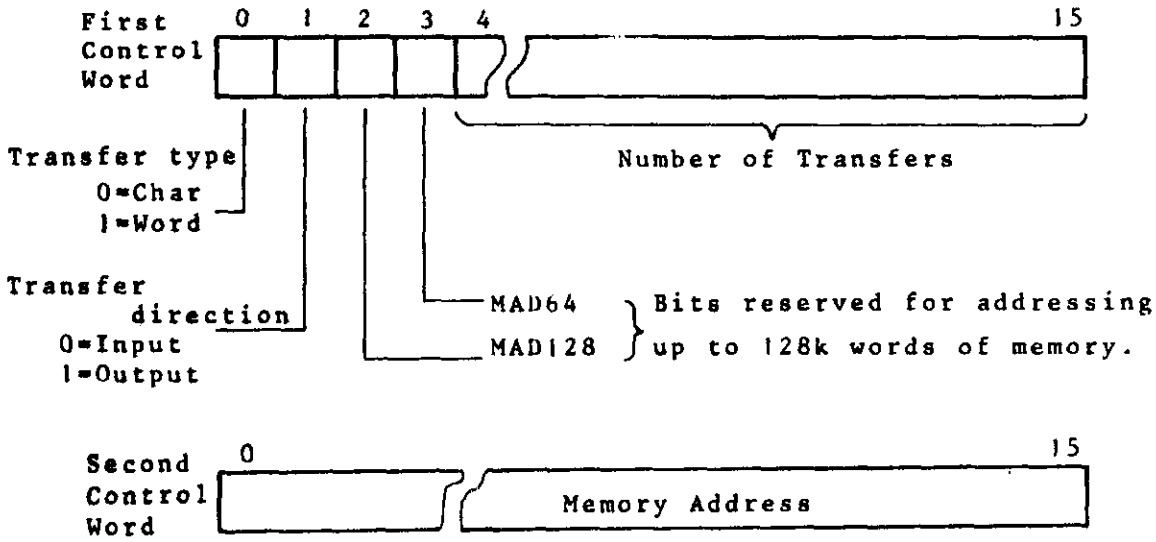

Figure 10.5. Layouts of Control Words.

If the required sub-channel is found not to be busy, the program may set up the two control registers using two WER instructions and start the channel unit concerned using a CIO Start instruction.
The channel unit switches to execute state for input, or to exchange for output. After receiving a character or word in execute state, a switch is made to exchange. In exchange state the channel unit emits a break signal to the IOP.

The transfer will now carry on independently without any further program action until it is complete and the channel unit switches into wait state and issues an interrupt to the CPU. The interrupt routine for the relevant channel unit will intercept the interrupt signal and switch the unit into inactive state if necessary, by issuing an SST instruction.

If the status returned by the channel unit indicates that an error condition exists, the contents of the IOP's control registers may be accessed (by RER) and used in either error recovery or error reporting routines.

10.3 MODES OF OPERATION

Three separate control paths are used during an IOP transfer, and the IOP may be in one of three distinct modes of operation associated with each data flow path.

1. Scan Mode.
   The IOP is scanning its Break lines for pending I/O requests.

2. CPU to IOP (CPU Mode).
   The CPU is the master of the exchange and is issuing WER or RER instructions to the IOP in order to initialize it for a transfer, or establishing the status of a completed transfer.

3. IOP to Memory or Channel Unit (Exchange Mode).
   The IOP is the master of the exchange and is controlling a transfer between memory and a channel unit or vice-versa. In this mode the IOP is responding to a break signal raised by a channel unit in exchange state, and is updating the transfer parameters held in its control registers. On completion of a transfer the channel unit generates an interrupt and the IOP reverts to Scan mode unless another break signal is outstanding, in which case it remains in exchange mode.

If a power failure occurs when the IOP is master of the exchange, the current exchange is aborted or completed and control of the G.P. Bus is returned to the CPU, regardless of outstanding break signals.