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Systems

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Field Support Manual
Central Processor Unit (CP1A)
P853

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Great care has been taken to ensure that the information contained in this handbook is accurate and complete. Should any errors or omissions be discovered, however, or should any user wish to make a suggestion for improving this handbook, he is invited to send the relevant details to:

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1.1 INTRODUCTION

Computer CP1A consists of a double-eurocard on which is mounted a 16-bit bipolar microprocessor operating in association with a 32 kword software memory and a 2 kword firmware memory. Software memory consists of a dynamic MOS RAM that can be accessed in either word or character mode and which provides storage for user programs, system stack and system interrupt address vectors.
Firmware memory consists of a 1 kword MOS ROM and a 1 kword static MOS RAM which together provide storage and working space for the bootstrap, interrupt routines control panel functions, test programs, etc.

An optional, dedicated ROM contains a 256-word Initial Program Loader (IPL); an initial program loader can also be entered from a remote source.
The computer is used with either a UPL Bus or a GPBS. A dedicated Bus Manager manages all system bus operations; dedicated Interrupt Handlers handle single-line and binary-coded interrupts. Also provided are parallel and serial data interfaces for the Operator Panel and Hand-Held Panel.

1.2 PHYSICAL DESCRIPTION (FIGURE 1.1)

The CP1A consists of a multilayer, double eurocard. The card is normally mounted vertically in card guides, and locates in the system backpanel by a 3x32-pin edge connector.

1.3 TECHNICAL DATA

1.3.1 PERFORMANCE DATA

16-bit bipolar µP
32 kword software RAM
1 kword firmware RAM
1 kword firmware ROM
Can address up to 256 external registers
Can address up to 64 I/O devices
Choice of control panels (Operator Panel or Hand-Held Panel)
Basic cycle time = 380nS
107 instructions in 2 formats and 8 addressing modes
Instruction timing (see table 1.1)
Independent Bus Manager compatible with UPL Bus and GPBS
Bus timing (see table 1.2)
Full DMA facility
64 interrupts and traps
Integral IPL and facility for remote IPL entry

1.3.2 POWER REQUIREMENTS

+ 5VL	at	2.8A (typ.)
+12VL	at	100mA (typ.)
-12VL	at	45mA (typ.)
+ 5VM	at	600mA (typ.)
+12VM	at	70mA (Stand-by)
		420mA (Operating)

Note: A -5VM supply is generated internally.

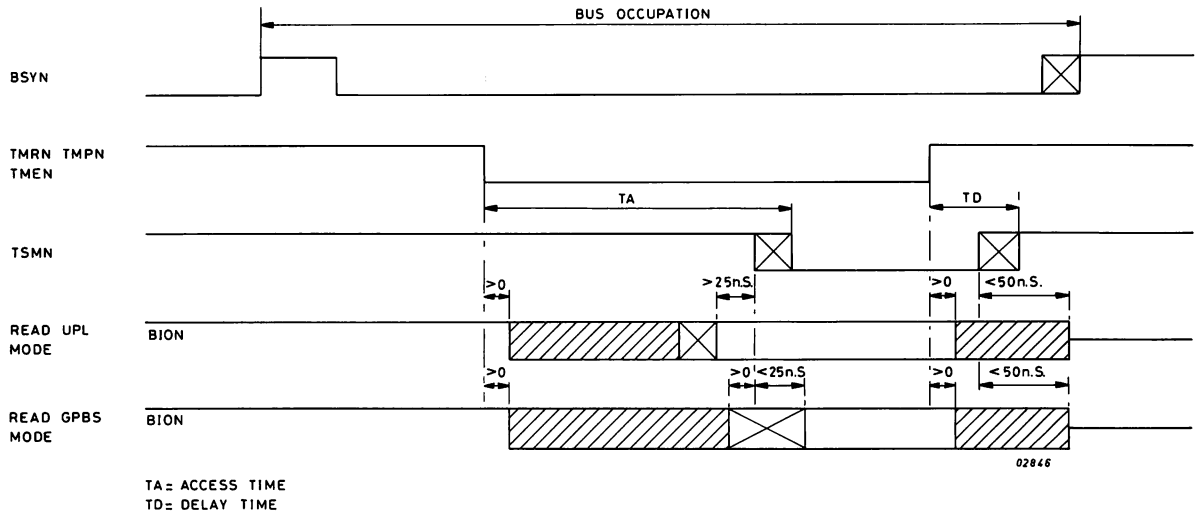
1.3.3 PHYSICAL CHARACTERISTICS

The double eurocard is multilayered and measures 162mm x 234mm x ⩽ 10mm.

Format Code	T8	T1	T2	T3	T3B	T4-T5	T6-T7
LD	9C 3.42	10C 3.8	16C 6.08	15C 5.7	23C 8.74	22C 8.36	28C 10.64
ST				19C 7.22	23C 8.74	26C 9.88	32C 12.16
AB	9C 3.42	10C 3.8	16C 6.08	15C 5.7	15C 5.7	22C 8.36	28C 10.64
With Load:- AD,SU,AN,OR,	9C 3.42	10C 3.8	16C 6.08	15C 5.7	15C 5.7	22C 8.36	28C 10.64
XOR,C1,C2 With Store:-				20C 7.6	20C 7.6	27C 10.26	33C 12.54
IM				20C 7.6	20C 7.6	27C 10.26	33C 12.54
CM				19C 7.22	19C 7.22	26C 10.26	32C 12.16
TM-TNM		10C 3.8					
RF-RB	10C 3.8						
I/O	13C 4.94 + I/O						
MU*		73C 27.74	79C 30.02	78C 29.64	78C 29.64	85C 32.3	91C 34.58
DV*		115C 43.7	121C 45.98	120C 45.6	120C 45.6	127C 48.26	133C 50.54
TB,TAS,TAR	If left character, add 1 cycle here: n = Number of Bit Tested in Character			38C+2nC 14.4+0.76n	38C+2nC 17.1+0.76n	45C+2nC 17.1+0.76n	51C+2nC 19.38+0.76n
ML	n = Number of Load Operations		50C+6nC 19+2.28n	19C+6nC 7.22+2.28n	24C+8nC 9.12+3.09n	26C+6nC 9.88+2.28n	32C+6nC 9.88+2.28n
MS	n = Number of Store Operations			17C+6nC 6.46+2.28n	18C+6nC 6.84+2.28n	24C+6nC 9.12+2.28n	30C+6nC 11.4+2.28n
DA-DS *		20C-27C 7.6-10.26	32C-39C 12.16-14.82	31C-38C 11.98-14.44	31C-38C 11.98-14.44	38C-45C 14.44-17.10	44C-51C 16.72-19.38
LC			20C 7.6	19C 7.22	19C 7.22	26C 9.88	32C 12.16
SC	For left character add 3C more			23C 8.74	23C 8.74	30C 11.4	36C 13.68
ECR		10C 3.8					
CW		12C 4.56	18C 6.84	17C 6.46	17C 6.46	24C 9.12	30C 11.4
CC			22C 8.36	21C 7.98	21C 7.98	28C 10.64	34C 12.92
EX with no Trap		14C 5.32	20C 7.6	19C 7.22	19C 7.22	26C 9.88	32C 12.16
CF		22C 8.36	28C 10.64	27C 10.26	27C 10.26	34C 12.92	40C 15.20
RTN				28C 10.64	32C-47C 12.16-17.86		
LDA		16C 6.08					
Set Bit Reset Bit	12C 4.56						
HLT/ENB	12C 4.56						
S ≠ N	12C+nC 4.56+0.38n						
SN	14C+2nC 5.32+0.76n	(11C if register contents are 0					
D ≠ N	17C+2nC 6.46+0.38n	n = 0 - 16C DRA, DLA - 16C+nC if n = 0 - 15C					
DN	16C+2nC 6.08+0.76n	15C if both register contents are 0					

Notes: - Execution time in microsec's.
- * = Typical values, because they are pattern dependent.
- C = 1 cycle = 380 ns.

Table 1.1 INSTRUCTION TIMING



TA = Access Time
TD = Delay Time

	Bus Occupation Timing (Typical)	Bus Occupation Timing (Maximum)
Single Memory Exchange	GPBS : 1.3μS UPL Bus : 1.25μS	GPBS : 1.79μS UPL Bus : 1.72μS
I/O Exchange	GPBS : 688nS+TA+TD UPL Bus : 555nS+TA+TD	GPBS : 1.05μS+TA+TD UPL Bus : 890nS+TA+TD
Locked Memory Exchange	GPBS : 4.72μS UPL Bus : 4.67μS	GPBS : 5.59μS UPL Bus : 5.52μS

Table 1.2 BUS OCCUPATION TIMING

1.3.4 ENVIRONMENTAL CONDITIONS

CLIMATIC

PARAMETER		OPERATING	NON-OPERATING	TRANSPORT
Temperature Range		0 to 50°C	-40 to 70°C	-40 to 70°C
Temperature Gradient		⩽ 1°C/mn	⩽ 1°C/mn	⩽ 1°C/mn
Pressure		600 to 1100mb	600 to 1100mb	600 to 1100mb
Humidity Without Condensation	RH% TRE D Point	⩽ 95% ⩽ 40% ⩽ 30%	⩽ 95% ⩽ 40% ⩽ 30%	

MECHANICAL

PARAMETER	OPERATING	NON-OPERATING	TRANSPORT
Vibration: Freq. Range	10 to 58Hz.	10 to 500Hz.	10-500Hz.
Peak Value	0.75 mm	0.75mm	0.75mm
Freq. Range	58 to 500Hz.		
Acceleration	0.5g	1g.	2.5g.
Sweep rate	1 oct./mn	1 oct./mn	1 oct./mn
Shock: Acceleration	5g	15g	15g
Duration	11mS	11mS	11mS
Motion	Half-Sine One Direction:-OZ	Half-Sine One Direction:-OZ	Half-Sine Six Directions

1.4 INTERFACES

SYSTEM CONNECTOR J1

Pin No.	Mnemonic	Function
J1A01	-12VL	-12V Logic Power Supply
02	+5VM	+5V Memory Power Supply
03	INCL	Interrupt Clock
04	IRALN	Interrupt Request Access L (level 14)
05	IRAMN	Interrupt Request Access M (level 15)
06	0V	GND
07	RSLN	Reset Logic
08	ACN	Accepted
09	0V	GND
10	TSMN	Timing Slave to Master
11	TMRN	Timing Master to Random Access Memory
12	0V	GND
13	MAD01	Master Address 01
14	MAD03	Master Adddres 03
15	MAD05	Master Address 05
16	MAD07	Master Address 07
17	MAD09	Master Address 09
18	MAD11	Master Address 11
19	MAD13	Master Address 13
20	MAD15	Master Address 15
21	WRITE	WRITE=1 for write function =0 for read function
22	0V	GND
23	BI000N	Bidirectional Input Output 00
24	BI001N	Bidirectional Input Output 01
25	BI002N	Bidirectional Input Output 02
26	BI003N	Bidirectional Input Output 03
27	BI004N	Bidirectional Input Output 04
28	BI005N	Bidirectional Input Output 05
29	BI006N	Bidirectional Input Output 06
30	BI007N	Bidirectional Input Output 07
31	+12VM	+12V Memory Power Supply
32	+5VL	+5V Logic Power Supply

These connections are not part of the System Bus (CONTD.)

Note: N= active low.

SYSTEM CONNECTOR J1

Pin. No.	Mnemonic	Function
J1B01	ERQN	Enable Request
02	BUSRN	Bus Usage Request
03	MSN	Master Selected
04	OV	GND
05	BSYN	Bus Busy
06	OKO	OK Out (the bus can be claimed by another master)
07	RIPLN	Remote Initial Program Loading
08	RTCN	Real Time Clock
09	BAWOFN	Battery Was Off
10	STOPN	Stops current computer activity
11	OV	GND
12	MADE0	Master Address Extended 0
13	MADE1	Master Address Extended 1
14	OV	GND
15	MADE2	Master Address Extended 2
16	MADE3	Master Address Extended 3
17	MADE4	Master Address Extended 4
18	MADE5	Master Address Extended 5
19	MADE6	Master Address Extended 6
20	MADE7	Master Address Extended 7
21	OV	GND
22	IRAAN	Interrupt Request A (level 4)
23	IRABN	Interrupt Request B (level 5)
24	IRACN	Interrupt Request C (level 6)
25	IRADN	Interrupt Request D (level 7)
26	OV	GND
27	IRAEN	Interrupt Request E (level 8)
28	IRAFN	Interrupt Request F (level 9)
29	IRAGN	Interrupt Request G (level 10)
30	IRAHN	Interrupt Request H (level 11)
31	+5VL	+5V Logic Power Supply
32	+5VL	+5V Logic Power Supply

These connections are not part of the System Bus (CONTD.)

Note: N= active low.

SYSTEM CONNECTOR J1

Pin. No.	Mnemonic	Function
J1C01	+12VL	+12V Logic Power Supply
02	+5VM	+5V Memory Power Supply
03	BCI	Binary-Coded Interrupt
04	IRAIN	Interrupt Request Access I (level 12)
05	IRAKN	Interrupt Request Access K (level 13)
06	OV	GND
07	PWFN	Power Failure
08	CLEARN	A General Reset
09	OV	GND
10	TMPN	Timing Master to Peripheral
11	TMEN	Timing Master to External Register
12	OV	GND
13	MAD00	Master Address 00
14	MAD02	Master Address 02
15	MAD04	Master Address 04
16	MAD06	Master Address 06
17	MAD08	Master Address 08
18	MAD10	Master Address 10
19	MAD12	Master Address 12
20	MAD14	Master Address 14
21	CHA	CHA=1 for character exchange =0 for word exchange
22	OV	GND
23	BIO08N	Bidirectional Input Output 08
24	BIO09N	Bidirectional Input Output 09
25	BIO10N	Bidirectional Input Output 10
26	BIO11N	Bidirectional Input Output 11
27	BIO12N	Bidirectional Input Output 12
28	BIO13N	Bidirectional Input Output 13
29	BIO14N	Bidirectional Input Output 14
30	BIO15N	Bidirectional Input Output 15
31	+12VM	+12V Memory Power Supply
32	+5VL	+5V Logic Power Supply

These connections are not part of the System Bus (CONTD.)

Note: N= active low

HHP CONNECTOR J3

Pin. No.	Mnemonic	Function
J3A01	SDPM	Serial Data Panel to Master
02	RTCE	Real Time Clock Enable
03	RESETN	A Reset Signal to the HHP
04	-12V	-12V Power Supply to the HHP
05	(Dummy)	
B01	LOCK	HHP Commands are inhibited and Automatic Restart is enabled
02	SDMP	Serial Data Master to Panel
03	OV	GND
04	+5V	+5V Power Supply to the HHP
05	+12V	+12V Power Supplyto the HHP

OP CONNECTOR J4

Pin No.	Mnemonic	Function
J4A01	0V	GND
02	RUNN	Sets CPU to 'RUN' mode
03	0V	GND
04	PONN	Planned Off (interrupts CPU)
05	0V	GND
06	ARE	Automatic Restart Enable
07	0V	GND
08	LOCK	OP Commands are inhibited and Automatic Restart is enabled
09	0V	GND
10	INCODE 5	Input Data Bit 5
11	INCODE 4	Input Data Bit 4
12	INCODE 3	Input Data Bit 3
13	INCODE 2	Input Data Bit 2
14	INCODE 1	Input Data Bit 1
15	INCODE 0	Input Data Bit 0
16	0V	GND
J4B01	RTCE	Real Time Clock Enable
02	0V	GND
03	SWOFN*	Software Off (a write-to external-register response to a PONN signal or data communication input)
04	0V	GND
05	(Dummy)	
06	SHEXN	Strobe Hardware External Not (strobes OUTCODE)
07	0V	GND
08	OUTCODEN7	Output Data Bit 7
09	OUTCODEN6	Output Data Bit 6
10	OUTCODEN5	Output Data Bit 5
11	OUTCODEN4	Output Data Bit 4
12	OUTCODEN3	Output Data Bit 3
13	OUTCODEN2	Output Data Bit 2
14	OUTCODEN1	Output Data Bit 1
15	OUTCODEN0	Output Data Bit 0
16	0V	GND

* Not used in P853 systems / N= active low

1.5 APPLICATION NOTES

The CP1A is intended to be used in P853 systems.

1.6 INSTALLATION DATA

1.6.1 STRAP-OPTIONS (SEE FIGURE 1.1)

1.6.2 MOUNTING

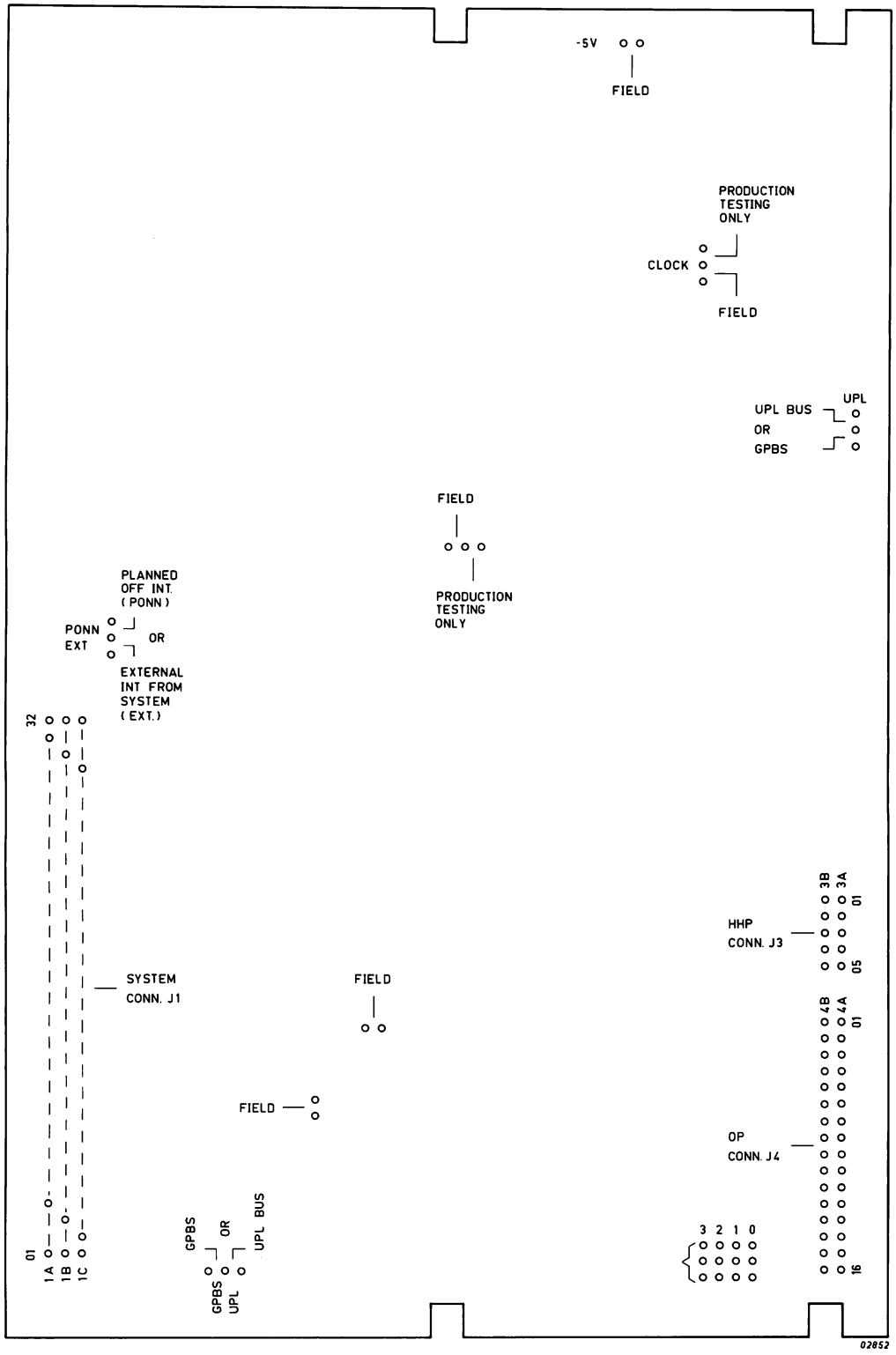
The double-eurocard locates vertically by edge connector J1 into the system backpanel and by card guides.

1.6.3 INTERCONNECTIONS

The CP1A can be connected to either an Operator Panel or an Hand-Held Panel at a maximum cable-length of 10m.

1.6.4 COMPATIBILITY

CP1A is compatible with UPL Bus and GPBS backpanels.



Straps for selection of automatic IPL device.
Straps are not to be fitted if Remote IPL device is connected.

Figure 1.1 CP1A STRAPS AND CONNECTORS

2 FUNCTIONAL DESCRIPTION

LIST OF ILLUSTRATIONS

LIST OF TABLES

2.1 CP1A HARDWARE ORGANIZATION (FIGURE 2.1)

The hardware of the CP1A is organized around a 16-bit address/data bus (A/D Bus) and a 16-bit internal master address bus (IMAD Bus). The multiplexed address/data lines of the μP are connected directly to the A/D Bus and the μP can access external units, 32kwords of Software Memory (also called Main Memory or Stack RAM), 2kwords of Firmware Memory (OP/HHP ROM and OP/HHP RAM), the IPL ROM, and two Mode ROM's by producing an address strobe signal (ASTRO) and depositing an address in the Address Latch.

When an external unit or Software Memory is accessed, the Bus Manager produces an enable memory signal (EMADN) which gates the address onto the System Bus lines. In the case of a Software Memory access, the address is supplied via the Refresh/Access Selector circuits whose other inputs (from the Refresh Address Generator) ensure that the dynamic MOS memory chips are periodically refreshed. The Ram Control Logic provides control and timing signals that select the required mode of operation (word or character, write or read, etc.) and also multiplex the address into row and column co-ordinates (RAS and CAS).

When Firmware Memory is accessed, the μP produces firmware (FIRMN) and request (REQN) signals. In combination with the address bits on the IMAD lines, these signals drive the Mode ROM's whose outputs provide the control signals that select the required area and function of Firmware Memory (OP/HHP ROM or OP/HHP RAM write or read) or select the IPL ROM.

In order to transfer data around the System, the μP and Bus Manager produce various control signals and enable signals that allow 16-bit data to be deposited in the Data Latch. Data transfers are bidirectional, and as well as consisting of data transfers between μP and memory, are of two kinds: Programmed Channel and Input Output Processor (IOP). Programmed channel transfers can be made between μP and peripheral unit but are relatively slow; IOP transfers can be made between Memory and peripheral unit and are very much faster, but they can only be made with the assistance of an external IOP Control Unit. The IOP method is, in effect, a form of direct memory access. A third option (DMACU) allows true DMA between Memory and CU's having DMA facilities.

The Bus Manager and its associated circuits control the operations of the asynchronous System Bus. The Bus Manager allocates the Bus to the unit having highest priority in accordance with the system priority scheme, and it also monitors Bus operations. An associated Time-Out circuit frees the Bus if the Bus hangs up due to a faulty unit or incorrect accessing operation. The Bus Manager can handle Memory, Peripheral and External Register accesses and has full bus-hand-shaking capabilities. Whenever not other unit requires the Bus it is automatically allocated to the CP1A.

The basic cycle time of the CP1A is 380nS, and the μP and system clocks are derived from a crystal-controlled oscillator and frequency-dividing stages.

Manual control of the CP1A is normally provided by either a Hand-Held Panel (HHP) or an Operator Panel (OP). Either panel may be used up to 10 metres away from the CP1A card.

In the case of the HHP, the panel commands are encoded and supplied to the CP1A as serially-coded data that are processed by the OP/HHP ROM Microprogram. When the microprogram is running it uses the OP/HHP RAM as a program stack, vector address store and flag store. In order to load an external program the operator must set up the device parameters on the HHP keyboard and push the IPL button. Pushing the button results in the Bootstrap loading the IPL Program into Software Memory. The IPL program then automatically loads the external program into Software Memory from the unit specified by the device parameters.

In the case of the Operator Panel, a smaller range of commands and controls are available and data are transferred between the panel and μP in parallel form. The panel operations are processed by the OP/HHP Firmware Microprogram. The CP1A Bootstrap and IPL Program routines can be triggered from the panel.

The CP1A can also run with no panel connected. In this case it is possible to trigger the Bootstrap and load the IPL into Software Memory from an external Data Communications Control Unit (DCCU).

Program sequences can be altered by the operation of the 63-level interrupt and trap system. The system consists of a group of several high-level interrupts (sometimes called internal interrupts), a group of intermediate-level, single-line interrupts and a larger group of low-level, binary-coded interrupts. The high-level group includes a non-maskable Firmware Interrupt, and maskable Power Failure/Automatic Restart, Link-to-Monitor or Stack Overflow, Real-Time Clock, and Control Panel interrupts. The Link-to-Monitor or Stack Overflow interrupt is entirely internal i.e. it is handled inside the μP chip. The rest of the interrupts (single-line and binary-coded) down to and including level 60 are assigned in accordance with the system interrupt priority scheme. Interrupt levels 62 and 63 are assigned to trap actions. In general the trap on the detection of special instruction formats and codes.

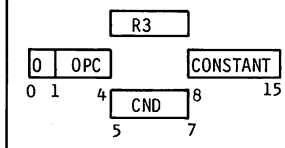
The Control and Status circuits monitor the states of the CP1A and latch them into flip-flops. The μP can obtain the system status by accessing the Status Buffer.

The Firmware Memory also contains a CP1A microdiagnostic routine. This program can be initiated from a control panel to test the CP1A.

2.2 CP1A SOFTWARE ORGANIZATION (TABLES 2.1 - 2.6)

CP1A instructions are the same as P851M instructions with the addition of some new instructions. Full details of P851M instructions are given in the appropriate programming guide. However, a summary of the CP1A instruction formats, addressing modes and instruction set are given in tables 2.1 and 2.2. Tables 2.3 - 2.6 detail the new instructions and the new trap. Note that ELR, ESR and RTF instructions can be executed only when the μP is switched to the Firmware State.

INSTRUCTION FORMATS



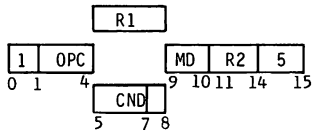
OPC : Operation Code
R3 : Register (scratchpad A0-7) on which the operation is performed.
CND : Condition for relative branching (when specified by OPC).

CND 5	6	7	Branch
0	n	n	if CR = bits 6,7
1	n	n	if CR ≠ bits 6,7
1	1	1	unconditional

CR = CONDITION REGISTER

CONSTANT: An 8-bit positive constant, branch displacement, or OPC extension.

a) Format 0



OPC : Operation Code
R1 : Register (scratchpad A0-15) on which the operation is performed
bit 8 = 0 : A0-7
bit 8 = 1 : A8-15
CND : Condition for absolute branching (when specified by OPC). (Conditions same as for format 0).
MD : Addressing Mode
R2 : Register (scratchpad A0-15) of 2nd operand or address of 2nd operand.
bit 14 = 0 : A0-7
bit 14 = 1 : A8-15
S : Store bit for memory reference instructions:
0 = store result in R1
1 = store result in memory

b) Format 1

ADDRESSING MODES

Type	Format 1 MD 9	10	R2 11	12	13	14	Effective Address of Operand	
T1	0	0	x	x	x	x	R2	Register-to-Register. R2 contains the operand.
T2	0	1	0	0	0	0	P	Long Constant. The following word after the instruction is the operand.
T3	0	1	non-zero				(R2)	Address in Register. R2 contains the address (A0-A15) of the operand.
T4	1	0	0	0	0	0	(P)	Address in Next Word. The following word is the operand address.
T5	1	0	non-zero				(P) + (R2)	Indexed Address. The following word, indexed by (A0-A15), as specified by R2, contains the operand address
T6	1	1	0	0	0	0	[(P)]	Indirect Address. The following word specifies the location containing the operand address
T7	1	1	non-zero				[(P) + (R2)]	Indirect indexed Address. The following word, indexed by (A0-A15), specifies the location containing the operand address
T8	format 0							Short Constant. No 2nd operand is used

Table 2.1 INSTRUCTION FORMATS AND ADDRESSING MODES

LOAD/STORE INSTRUCTIONS		FORMAT	NOTE
LD	Load Register	T4-T7	*
LDR	Load Reg./Reg.	T1,T3	*•
LDK	Load Constant	T8,T2	*
ST	Store Register	T4-T7	*
STR	Store Reg./Reg.	T3	*•
ML	Multiple Load	T4-T7	*
MLR	Multiple Load/Reg.	T3	*•
MLK	Multiple Load Const.	T2	*
MS	Multiple Store	T4-T7	*
MSR	Multiple Store/Reg.	T3	*•
ELR	Extended Load/Reg.	T2	*
ESR	Extended Store Reg.	T2	*
LDA	Load Address	Special	*

ARITHMETIC INSTRUCTIONS		FORMAT	
AD	Add	T4-T7	*
ADR	Add Reg./Reg.	T1,T3	*
ADK	Add Constant	T8,T2	*
SU	Subtract Word	TA-T7	*
SUR	Subtract Reg./Reg.	T1,T3	*
SUK	Subtract Constant	T8,T2	*
MU	Multiply	T4-T7	
MUR	Multiply Reg./Reg.	T1,T3	
MUK	Multiply Constant	T2	
DV	Divide	T4-T7	
DVR	Divide Reg./Reg.	T1,T3	
DVK	Divide Const.	T2	
DA	Double Add	T4-T7	
DAR	Double Add Reg./Reg.	T1,T3	
DSK	Double Subtract Const.	T2	
C2	Two's Complement	T4-T7	
C2R	Two's Complement/Reg.	T3	
IM	Increment Memory	T4-T7	
IMR	Increment Memory/Reg.	T3	
NGR	Negate Register	T1	
CM	Clear Memory	T4-T7	
CMR	Clear Memory Register	T3	
CW	Compare Words	T4-T7	*
CWR	Compare Word Reg./Reg.	T1,T3	*
CWK	Compare Word Constant	T2	*

SHIFT INSTRUCTIONS		FORMAT	
SLA	Left Arithmetic Shift	T8	
SRA	Right Arithmetic Shift	T8	
SLL	Left Logical Shift	T8	
SRL	Right Logical Shift	T8	
SLC	Left Circular Shift	T8	
SRC	Right Circular Shift	T8	
SLN	Left Shift and Norm.	T8	*
SRN	Right Shift and Norm.	T8	*
DLA	Double Left Arith. Shift	T8	
DRA	Double Right Arith. Shift	T8	
DLL	Double Left Logic Shift	T8	
DRL	Double Right Logic Shift	T8	
DLC	Double Left Circ. Shift	T8	
DRC	Double Right Circ. Shift	T8	
DLN	Doub.Left and Norm. Shift	T8	*
DRN	Doub.Right and Norm. Shift	T8	*

CONTROL INSTRUCTIONS		FORMAT	NOTE
ENB	Enable Interrupts	T8	
HLT	Halt	T8	
RIT	Reset Int. Inter.	T8	
INH	Inhibit Interrupts	T8	
LKM	Link to Monitor	T8	
RTF	Return from Firmware	T8	

INPUT/OUTPUT INSTR.		FORMAT	
CIO	Control Input/Output	T8	
INR	Input to Reg.	T8	+
OTR	Output from Reg.	T8	+
SST	Send Status	T8	
TST	Test Status	T8	+
RER	Read Ext. Reg.	T8	+
WER	Write Ext. Reg.	T8	+

LOGICAL INSTR.		FORMAT	
AN	Log. AND	T4-T7	* +
ANR	Log. AND Reg./Reg.	T1,T3	* +
ANK	Log. AND Constant	T8,T2	* +
OR	Log. OR	T4-T7	* +
ORR	Log. OR Reg./Reg.	T1,T3	*
ORK	Log. OR Constant	T8,T2	* +
XR	Exclusive OR	T4-T7	*
XRR	Ex. OR Reg./Reg.	T1,T3	*
XRK	Ex. OR Constant	T8,T2	*
TM	Test Mask	T1	*
TNM	Test Not Mask	T1	*
CI	One's Complement	T4-T7	* +
CIR	One's Compl. Reg./Reg.	T1,T3	*
TB	Test Bit	T3-T7	
TSB	Test and Set Bit	T3-T7	
TRB	Test and Reset Bit	T3-T7	

CHARACTER HANDL. INSTR.		FORMAT	
LC	Load Character	T-T7	* +
LCR	Load Charac./Reg.	T3	* +
LCK	Load Charac. Const.	T2	* +
SC	Store Character	T4-T7	* +
SCR	Store Charac./Reg.	T3	* +
CC	Compare Character	T4-T7	* +
CCR	Compare Charac./Reg.	T3	* +
CCK	Compare Charac./Const.	T2	* +
ECR	Exch. Charac.Reg./Reg.	T	* +

BRANCH INSTRUCTIONS		FORMAT	
AB	Absolute Branch Cond.	T8,T2	
ABR	Absolute Branch Reg.	T1,T3	
ABI	Absolute Branch Indir.	T4-T7	
RB	Relative Branch Backw.	T8	
RF	Relative Branch Forw.	T8	
CF	Call Function	T2	*
CFR	Call Function Reg.	T1,T3	*
CFI	Call Function Indir.	T4-T7	*
RTN	Return	T3	*
EX	Execute	T4-T7	
EXR	Execute Register	T1,T3	
EXK	Execute Constant	T2	+

* Privileged instruction when A15 is addressed.
• Privileged instruction when instruction is Type 3B.
+ Trap will occur in some conditions.

Privileged instruction may only be executed while the µP is switched to System Mode. Any attempt to execute these instruction while the µP is switched to User Mode will cause a trap. The µP can be legally switched to System Mode by executing an LKM instruction.

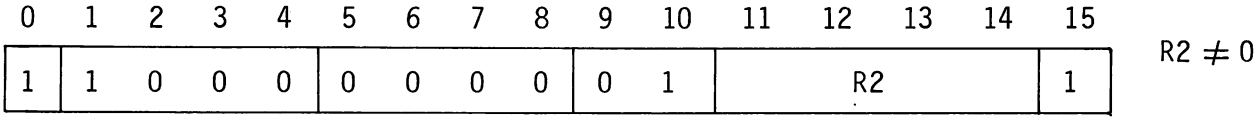
Table 2.2 INSTRUCTION SET

TEST AND SET BIT

BIT POSITION CALCULATION

The effective address (calculated according to the addressing modes) gives the byte address of the first byte of the bit string.
The unsigned arithmetic value of the register A2 gives the bit position in the string.

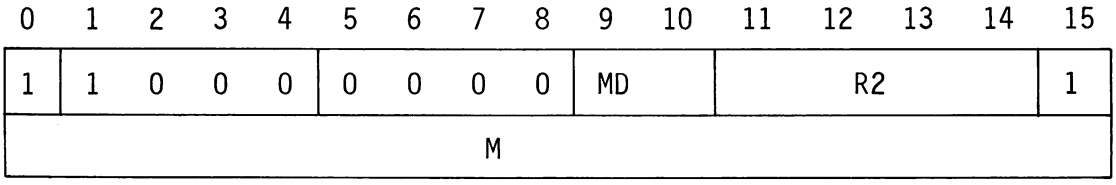
T3 FORMAT:



The effective address of the first byte of the string is in R2. The bit number (A2) from this address is tested:

- If this bit is 0, it is changed into 1 and CR becomes 00
- If this bit is 1, it is left unchanged and the CR becomes 01
- The lock mechanism is activated

T4, T5, T6, T7 FORMATS:



The effective address of the first byte of the string is obtained as follows:

T4 : MD = 10, R2 = 0 ; EA = M
T5 : MD = 10, R2 0 ; EA = M + R2
T6 : MD = 11, R2 = 0 ; EA = (M)
T7 : MD = 11, R2 0 ; EA = (M + R2)

The bit number (A2) from this position is tested (see T3 format for operation description).

Table 2.3 TEST AND SET BIT INSTRUCTION

TEST AND RESET BIT

The bit position calculation is the same as in Test and Set Bit.

T3 FORMAT:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
1	1	0	0	1	0	0	0	0	0	1	R2				1	R2 ≠ 0

The affective address of the first byte of the string is in R2.
The bit number (A2) from this address is tested:

- If this bit is 0, it is left unchanged and the CR becomes 00
- If this bit is 1, it is changed into 0 and the CR becomes 01
- The lock mechanism is activated

T4, T5, T6, T7 FORMATS:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	0	0	1	0	0	0	0	MD		R2				1
M															

The effective address of the first byte of the string is obtained as indicated above and the operation on the bit is the same as in T3 format.

Table 2.4 TEST AND RESET BIT INSTRUCTION

TEST BIT

The bit position calculation is the same as in Test and Set Bit.

T3 FORMAT:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	0	1	0	0	0	0	0	0	1	T3				1

$R2 \neq 0$

The effective address of the first byte of the string is in R2. The bit number (A2) from this address is tested:

- If this bit is 0, the CR takes the value 00
- If this bit is 1, the CR takes the value 01

T4, T5, T6, T7 FORMATS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	0	1	0	0	0	0	0	M	D	R2				1
M															

The effective address of the first byte of the string is obtained as indicated above and the operation on the bit is the same as in T3 format.

LOAD ADDRESS

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	1	1	0	R1				0	0	R2				0
M															

The content of R2 is added to M, the result is loaded into R1. CR is unchanged.
This instruction is trapped if R1 = 0.
Also trapped if R1 = A15 in User Mode.

Table 2.5 TEST BIT INSTRUCTION AND LOAD ADDRESS INSTRUCTION

/7C TRAP

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	1	1	0	1	0	0	0	X	X	X	X	X	X	X	X

When such a code is detected, a trap occurs that does the following operations:

- The address of this instruction is saved at location (A15)
- PSW is saved at location (A15)-2
- A15 takes the value (A15)-4
- The Enable bit is reset to 0
- The User bit is reset to 0
- P is loaded with the contents of the memory at address /7C

Tabel 2.6 /7C TRAP

2.3 SYSTEM BUS INTERFACE

2.3.1 PROGRAMMED CHANNEL DATA TRANSFERS

Programmed channel data transfers are used to transfer data between CP1A and Control Units (CU) and also to transfer initialization-parameters to an Input Output Processor Unit (IOP). Input/Output instructions (see table 2.2) are used to start and control the transfer of data. A separate instruction is needed to transfer each word or character and the instructions include those that are used to test the availability and status of the CU. There are two types of Programmed Channel Operation. In inhibit mode the CP1A cycles on a test-CU loop until the CU is available for data transfers - this method is slow.
In interrupt mode the CP1A initiates a data transfer and then jumps back to the main program. When the word or character has been transferred the CU produces an Interrupt signal which is serviced by the µP.

2.3.2 INPUT OUTPUT PROCESSOR CHANNEL DATA TRANSFERS

The CP1A sends the initialization parameters - block length, memory start address, transfer type (write or read) - to the IOP and then initializes the CU. When the IOP is triggered it transfers data between Memory and the CU. Before each word or character can be transferred the CU must send a Break Request signal to the IOP. When the data transfer is completed, the CU generates an Interrupt signal which is serviced by the CP1A.

2.3.3 DMACU DATA TRANSFERS

Some CU's are fitted with DMA interfaces. Data can be transferred between Memory and one of these units over a direct connection that requires no intervening control unit.

2.3.4 OUTLINE OF CP1A SYSTEM BUS ALLOCATION (FIGURE 2.2)

Before it obtains use of the bus, the CP1A microprocessor generates various control signals that are latched into the Bus Manager (BM) by the bus request strobe signal (BRQSI). These signals set up the BM to operate in one of the following modes:

a) Memory access with lock mode
b) Memory access without lock mode
c) Peripheral access without lock mode
d) External register access without lock mode
   (lock mode is used to retain control of the bus for more than one access cycle)

If the following conditions are true, the BM allocates use of the bus to the CPiA:

a) No other master has requested use of the bus (BUSRN is hi)
b) No other master has been selected to use the bus (MSN is hi)
c) The bus is not busy (BYSN is hi)

When it has allocated use of the bus, the BM continues to monitor the BUSRN line so that it can detect a new bus request generated by another master. It also sets its OKO output lo and this signal is daisy-chained through the other masters in accordance with the System Bus priority scheme. (The master that is the first in the chain has highest priority).
Details of system CU bus interface operations are given in the appropriate CU manuals.

After it has obtained use of the bus the CP1A sets the busy line BSYN lo. It then generates control signals EMADN, EBON, WRITE as required by the type of data transfer, and either signal TMRN, TMPN or TMEN is set lo in accordance with the type of unit being accessed. When the BM receives a TSMN signal from the accessed unit it sets its ready line RDY lo so that the µP knows that the data transfer address has been accepted. If a TSMN signal is not received within a nominal 6.5µS, an artificial TSMN signal is generated by the Time-Out circuit so that the Bus will not hang up and prevent further operations.

2.4 CONTROL PANEL INTERFACES

2.4.1 HAND-HELD PANEL (TABLE 2.7 AND FIGURE 2.3)

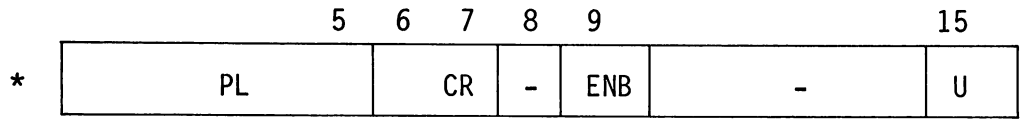
Commands and data are transferred between HHP and CP1A over a 4.8kbaud, V24/V28 serial-data interface. A list of command and data codes is given in the table. Full details of command and data codes are given in the HHP Field Support Manual.

In the CP1A, a Serial Data Panel-to-Master (SDPM) start bit causes a firmware interrupt. Control passes to the Firmware Microprogram (OP/HHP ROM), which saves the contents of registers A0 to A15 and the PSW on the Firmware Memory stack (OP/HHP RAM). It then starts a software timer and accesses the Status Buffer to discover the source of the Interrupt. When the source is known, the software timer synchronizes and reads in the serial data code. After the data has been decoded the Microprogram takes the appropriate actions. If it is necessary for the µP to send data or commands to the HHP it does so over a Serial Data Master-to-Panel (SDMP) line. The CP1A is capable of resetting the HHP and it normally provides it with +12V, +5V and -12V power supplies.

Operating the HHP LOCK switch sets the CP1A so that it will automatically load the IPL Program or restart after a power failure. It also inhibits all HHP functions except an INT command and therefore allows the HHP to be disconnected without disturbing the CP1A.

Operating the RTC switch generates a Real Time Clock Enable signal which is supplied to the CP1A to gate the Real Time Clock signal to the µP.

COMMAND		CODE	DATA	CODE
HHP TO CP1A			REG.ADDR. + DATA	(3x) +(3x3x3x3x):
MCL	Master Clear	40	0	30
LR	Load Register	41	1	31
RR	Read Register	42	2	32
RST*	Read Status	43	3	33
IPL+	Load IPL	44	4	34
LM	Load Memory	45	5	35
INT•	Interrupt	46	6	36
RM	Read Memory	47	7	37
LA	Load Address	48	8	38
INST	Instruction Step	49	9	39
RA	Read Address	4A	A	3A
RUN	RUN	4B	B	3B
P.ACC	Preset Access	4C	C	3C
P.W	Preset Write	4D	D	3D
TEST	Test	4E	E	3E
P.OFF	Preset Off	4F	F	3F
LM2	Load Memory 2	55		
RM2	Read Memory 2	57	MEMORY ADDR.	(BxBxBxBxBx):
CP1A TO HHP:			0	B0
RUNZ0	Not Running	40		
RUNZ1	Running	41	F	BF



PROGRAM STATUS WORD - PSW
(HHP DISPLAY FOR RST COMMAND)

PL = Program Level
CR = Condition Register
ENB = Interrupts Enabled
U = User Mode

• Panel Interrupt (level 3)

+ IPL Program loaded into Software Memory Addresses /0000 thru /01FE.
(Device parameters in /01E0 thru /01EF)
The PSW is set to that:
PL = 63
ENB = 0
U = 0

Table 2.7 HHP COMMAND/DATA CODES

2.4.2 OPERATOR PANEL (TABLES 2.8 AND 2.9)

OP commands are transferred on single lines but data codes are transferred on six parallel lines (OP to CP1A) by the using an RER instruction to address /F6, and eight parallel lines (CP1A to OP) by using a WER instruction to address /F6. Full details of the OP are given in the appropriate technical manual.

The IPL Program is loaded from the OP by setting the thumbwheel switch for the required device parameters and press the RUN button. The resulting RUNN signal is supplied to the CP1A where it causes a firmware interrupt. Control transfers to the firmware microprogram, which saves the contents of registers A0 to A15 and then accesses the Status Buffer to discover the origin of the interrupt. The contents of the IPL ROM are loaded into Software Memory locations /000 thru /1FE (Device Parameters in /1E0 thru /1FE). The required Device Parameters are read into the CP1A by executing an RER instruction to access the OP Interface. The external program is loaded into Software Memory from the selected device.

When the CP1A is powered up the positive-going edge of the power monitor signal (Power Failure Not - PWFN/AR) generates a level 0 interrupt which switches the CP1A to firmware mode at OP/HHP ROM address 0. The microprogram tests if the ARE signal is set i.e. that the RESTART button has been pressed.
If it has the following operations occur:

a) CP1A generates a CLEARN system bus signal to reset the system
b) The PSW is loaded with PL = 00, ENB = 0, U = 0
c) Control branches to Software Memory address 0 and the CP1A is set to the RUN state

When the system has been operating it is possible to shut it down by using the planned-off facility. Pressing the ON button sets the Planned-Off Not signal (PONN) and generates a firmware interrupt. The firmware microprogram identifies the source of the interrupt by accessing the Status Buffer and then operates in accordance with the state of the CP1A:

a) If CP1A is in the RUN state a level 4 interrupt is generated and optional CP1A software produces a WER instruction that, via the OP, puts the system power supply into Maintain Mode by generating a SWOFN signal.
b) If CP1A is in the IDLE state no level 4 interrupt is generated but hardware puts the system power supply into Maintain Mode by generating a Software Off Not signal (SWOFN) and sending it to the OP.

In either case operations can be resumed where they were stopped by setting the OP power switch to MEMORY ON and then back to MASTER ON.

Note: If an OP is not connected the level 4 interrupt is reserved for another purpose.

Pressing the REMOTE button sets the LOCK signal which locks the operation of the system and also permits the OP to be disconnected without disturbing the CP1A. Pressing the TIMER button generates a Real Time Clock Enable signal (RTCE) that gates the Real Time Clock to the μP.

FUNCTION	SIGNAL(S) TO CP1A
MEMORY OFF/MEMORY ON MASTER ON	MEM OFF = NONE MEM ON = VM VOLTAGES ONLY MAS ON = VL + VM VOLTAGES
RUN	RUNN
RESTART	ARE
ON	PONN
REMOTE	LOCK
TIMER	RTCE

Table 2.8 OP FUNCTION SIGNALS

THUMBWHEEL CODE	SIGNIFICANCE	DISPLAY CODE	SIGNIFICANCE
0	TEST		
	T.B.F.		

Table 2.9 OP DATA CODES

2.4.3 NO PANEL CONNECTED

The CP1A can operate with no panel connected, and it is also possible to load a remote IPL program from a DCCU. In this case a Remote Initial Program Load Not (RIPLN) signal is used to trigger a firmware interrupt from the DCCU and four straps are used to set the device parameters of the DCCU (one device only).

When the system has no battery back-up, the Bootstrap is automatically loaded whenever the CP1A is powered up by switching on the system.

When the system has a battery back-up and the CP1A is powered up it will execute either an Automatic Restart routine (if the Battery Was Off Not (BAWOFN) signal is set to 1) or the Bootstrap will be triggered and the IPL Program will be loaded.

2.5 CP1A OPERATING STATES

The CP1A has three possible operating states:

a) INITIAL STATE - This state is transitional between power-up and the IDLE or RUN state.
b) IDLE STATE - In this state no program is running and the CP1A is waiting for a command.
c) RUN STATE - In this state a program is running.

At power-up the RSLN input to the CP1A is at 0 and the CP1A (including the µP) is reset. When the RSLN signal goes to 1 the reset is removed.

When the PWFN goes to 1 a firmware interrupt is generated and control switches to the firmware microprogram (OP/HHP ROM start routine. The routine checks whether a LOCK input from an HHP or OP is present. If LOCK is at 0, i.e. not present, the CP1A switches to IDLE state. If LOCK is at 1, i.e. present, the start routine checks if the battery was connected when the power failed (or was switched off) i.e. it checks if the Software Memory (dynamic MOS) data was lost. If the data was lost the IPL Program is loaded because the external program must be reloaded. If data was not lost the Automatic Restart interrupt is generated and the program restarts at the point were it was stopped. In eiher case the CP1A switches to RUN state.

2.6 INTERRUPTS AND TRAPS (FIGURE 2.5)

There are sixty four interrupts and traps. They can be grouped as follows:

a) Four high-level interrupts (levels 0 - 3), three of which are connected directly to the µP and the fourth of which is internal to the µP.
b) Twelve intermediate-level interrupts (level 4 - 15) which are single-line terrupts interrupts from external units. These interrupts are encoded by two Interrupt Handlers (IHs) for onward transmission to the third IH on the common BCI line.
c) Fourty five low-level interrupts (levels 16 - 60) which are binary-coded interrupts produced by IHs fitted to external units. These serial inputs are supplied to the third IH on the common BCI line.
d) Traps

An interrupt of group (b) or (c) that is accepted by the CP1A results in an EXTIN signal which interrupts the µP.

2.6.1 HIGH-LEVEL INTERRUPTS 0 - 3 (TABLES 2.10 AND 2.11)

These interrupts are enabled by an ENB instruction and inhibited by an INH instruction. After an interrupt has occured it is normally reset by an RIT instruction. But this operation is not permitted during an Automatic Restart sequence . In all four cases the action that is taken in response to the interrupt is dependant upon the software interrupt routine.

LEVEL	CONDITION	ACTION
0	Power Failure or Power-Off (PWFN goes to 0)	μP completes execution of current instruction, saves PC and PSW on Software Memory stack and vectors to Software Memory Address /0000.
1*	Link-to-Monitor instruction or a Stack Overflow condition	As above, but control vectors to Software Memory Address /0002.
2	Real Time Clock (RTC) from system power supply gated to μP by the Real Time Clock Enable signal from HHP or OP	As above, but control vectors to Software Memory Address /0004.
3	Panel Interrupt (PANEL INT) from HHP	As above, but control vectors to Software Memory Address /0006.

* This interrupt is internal to the μP.

Table 2.10 HIGH-LEVEL INTERRUPTS

2.6.2 INTERMEDIATE (4-15) AND LOW-LEVEL (16-60) INTERRUPTS (TABLE 2.11, FIGURE 2.5 AND 2.6)

These interrupts are maskable and are enabled by an ENB instruction and inhibited by an INH instruction.

An interrupt that occurs on one of the single-line inputs is encoded by its associated IH and is transmitted to the third IH on the BCI line. Reception of a BCI code is synchronized by Interrupt Clock (INCL) pulses. The format of a BCI code is shown in the illustration. If a BCI code is transmitted simultaneous with a BCI code produced by another source, the code having the higher priority (lower number) is given precedence, i.e. the lower priority code is suppressed. This is possible because the BCI line of each source is connected to a wired-or bus. A zero on the bus is used to reset and eliminate a BCI code emanating froma source having a lower priority than a contending source. For example, suppose that there are three contending BCI codes:

a) 011000 - level 24
b) 001001 - level 9
c) 001011 - level 11

The most significant digit is 0 in all three cases so a 0 is placed on the BCI line.
The next digit is 0 for (b) and (c) so a 0 is placed on the BCI line. This 0 resets source (a) and it is eliminated.

The next digit is a 1 for (b) and (c) so a 1 is placed on the BCI line.
The next digit is a 0 for (b) and (c) so a 0 is placed on the BCI line.
The next digit is a 0 for (b) but a 1 for (c) so a 0 is placed on the BCI line. This 0 resets and eliminates source (c).

The last digit is a 1 so a 1 is placed on the BCI line.

The successful BCI code is compared with the current value of the Program Level Register (PLR). If it has a lower value (higher priority) an EXIN signal interrupts the µP. The µP then executes an RER /00FF instruction which, via the Mode ROMs, sets signal CSINT to 0. The new BCI code is transferred to the µP on the A/D Bus (RDY goes to 1 when the transfer is completed). The µP then conforms a WER /00FF instruction, which writes the new BCI code into the PLR. The new interrupt level is decoded and control branches to the appropriate software interrupt routine.
Intermediate and low-level interrupts are reset by I/O Commands. When the PL Reg. IH is cleared, the contents of the PL Reg. are set to 111111 (level 63).

Note: When an interrupt is generated and reset by an I/O Command without being serviced (because the CP1A is in Inhibit Interrupt Mode) the interrupt system must be reset by executing an RTN-A15 instruction.

2.6.3 TRAPS

A D-Format trap to Software Memory Address /7C occurs whenever an instruction has the form 01101000xxxxxxxx (addressing mode T8). Control branches to a software routine which either simulates decimal arithmetic instructions or provides character handling routines that permit the efficient packing of characters in memory, ASCII to binary code conversion, etc.
An I-OP (Illegal Operation) trap to Software Memory Address /7E occurs when:

a) The CP1A is in System Mode and an unallocated instruction code is detected
b) The CP1A is in User Mode and either an unallocated or a priviledged instruction code is detected.

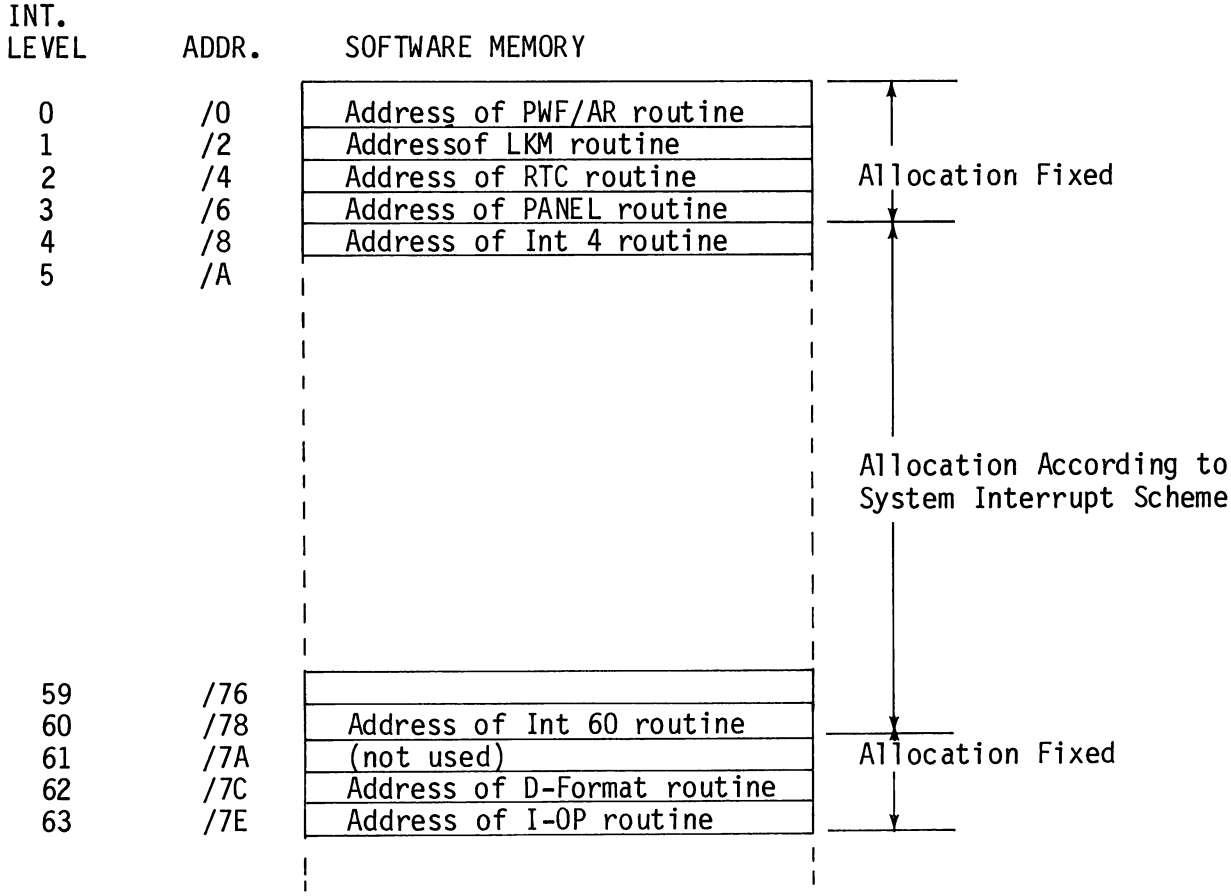


Table 2.11 SOFTWARE INTERRUPT ADDRESS VECTORS

2.7 MEMORY ORGANIZATION

2.7.1 SOFTWARE MEMORY (FIGURE 2.7 - 2.9 AND TABLE 2.12)

The Software Memory consists of 32, 16kword x 1-bit dynamic MOS RAM chips that are configured as shown in the illustration. Each half of the memory is read or written with words or characters in accordance with the settings of the MAD0, WRITE, MAD15 and CHA inputs to the RAM Control Logic. Note that characters are always written from or read to the right half of the BION bus (BION 8 - 15).

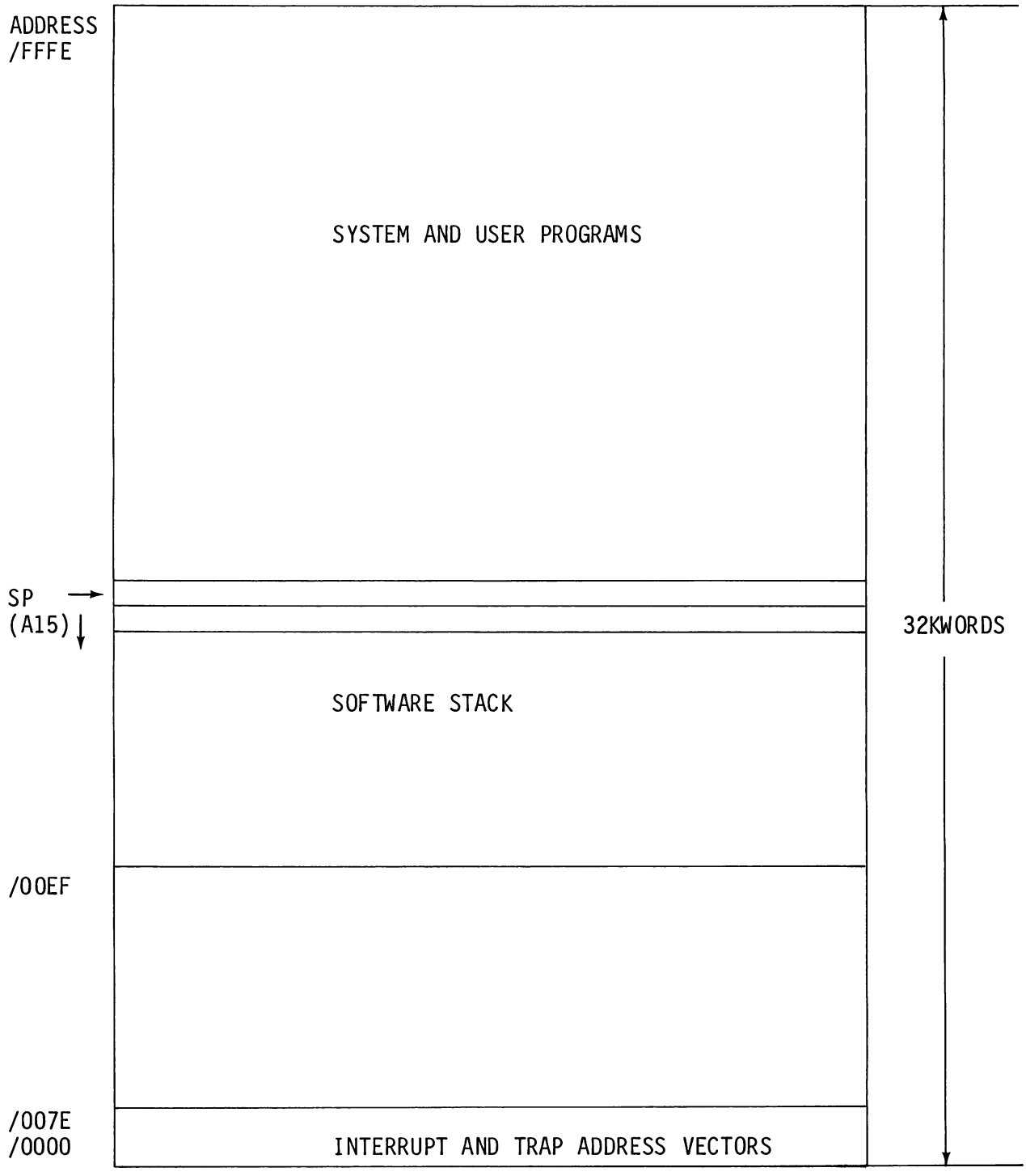
Memory data are periodically refreshed by the Refresh Address Generator. A RAS-only refresh cycle is generated every 12.16µS and each cycle refreshes 128 addresses. If a refresh request occurs during an access cycle, the access cycle is completed before the refresh cycle is allowed to start.

Note that the UPL Bus has eight extra (extended) address lines (MADE 0 - 7). These are not used by the CP1A so when the Address Buffer is selected they are set to 00000000. If a MADE line is set high by an external unit or by a fault condition, the CP1A RAM Control Logic is automatically disabled.

Note: External Master Control Units may access the Software Memory in either Word or Character mode, but the CP1A can access the Software Memory only in Word mode.

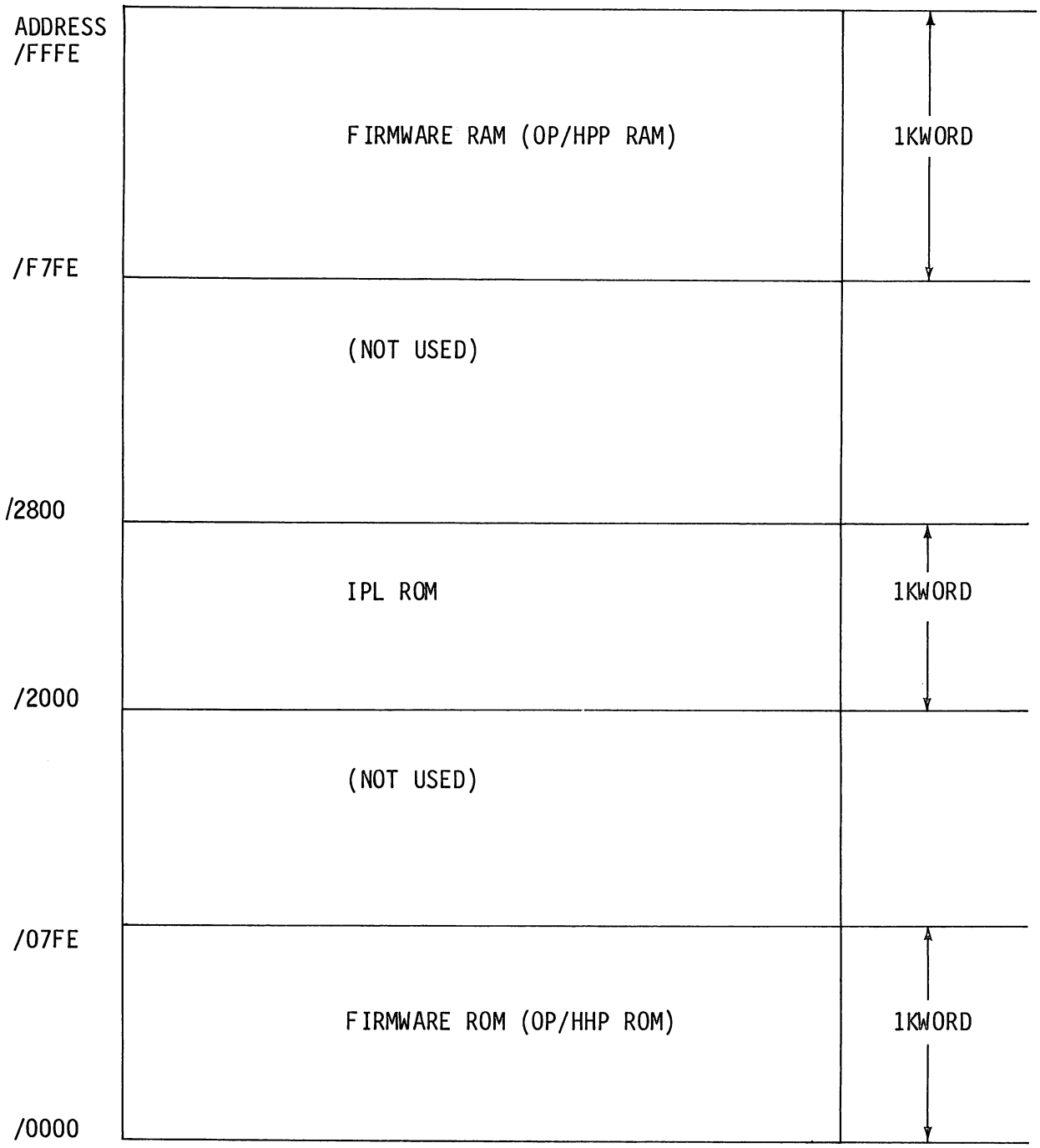
2.7.2 FIRMWARE MEMORY (TABLES 2.13 AND 2.15)

The firmware Memory consists of a 1kword ROM and a 1kword RAM that are organized as shown in the tables. The firmware addressing range includes that of the IPL ROM.



Note: IPL Program occupies locations /0000 to /01FE
(Device parameters in /01E0 to /01FE)

Table 2.12 SOFTWARE MEMORY ALLOCATION



IMAD01:	IMAD02:	SELECTS:
0	0	OP/HHP ROM
0	1	IPL ROM
1	1	OP/HHP RAM

Table 2.13 FIRMWARE MEMORY ARRANGEMENT

ADDRESS	
/0 3 F 2	HHP DISPLAY
/0 3 4 E	
/0 3 4 C	IPL BOOTSTRAP
/0 2 F C	
/0 2 F A	TEST (MICRODIAGNOSTICS)
/0 2 1 A	
/0 2 1 8	HHP FUNCTIONS
/0 0 E A	
/0 0 E 8	INITIALIZATION
/0 0 D 6	
/0 0 D 2	REMOTE IPL VECTOR ADDRESS TO IPL BOOTSTRAP
/0 0 D 0	
/0 0 C E	PLANNED OFF
/0 0 C C	
/0 0 C 8	HALT
/0 0 A C	
/0 0 A A	EPINT
/0 0 5 A	
/0 0 5 8	AUTOMATIC IPL VECTOR ADDRESS TO IPL BOOTSTRAP
/0 0 3 6	
/0 0 3 4	IDLE
/0 0 2 E	
/0 0 2 C	AUTOMATIC RESTART
/0 0 1 A	
/0 0 1 8	START
/0 0 0 4	
/0 0 0 2	ADDRESS VECTOR TO EPINT
/0 0 0 0	ADDRESS VECTOR TO START

Table 2.14 OP/HHP ROM ALLOCATION

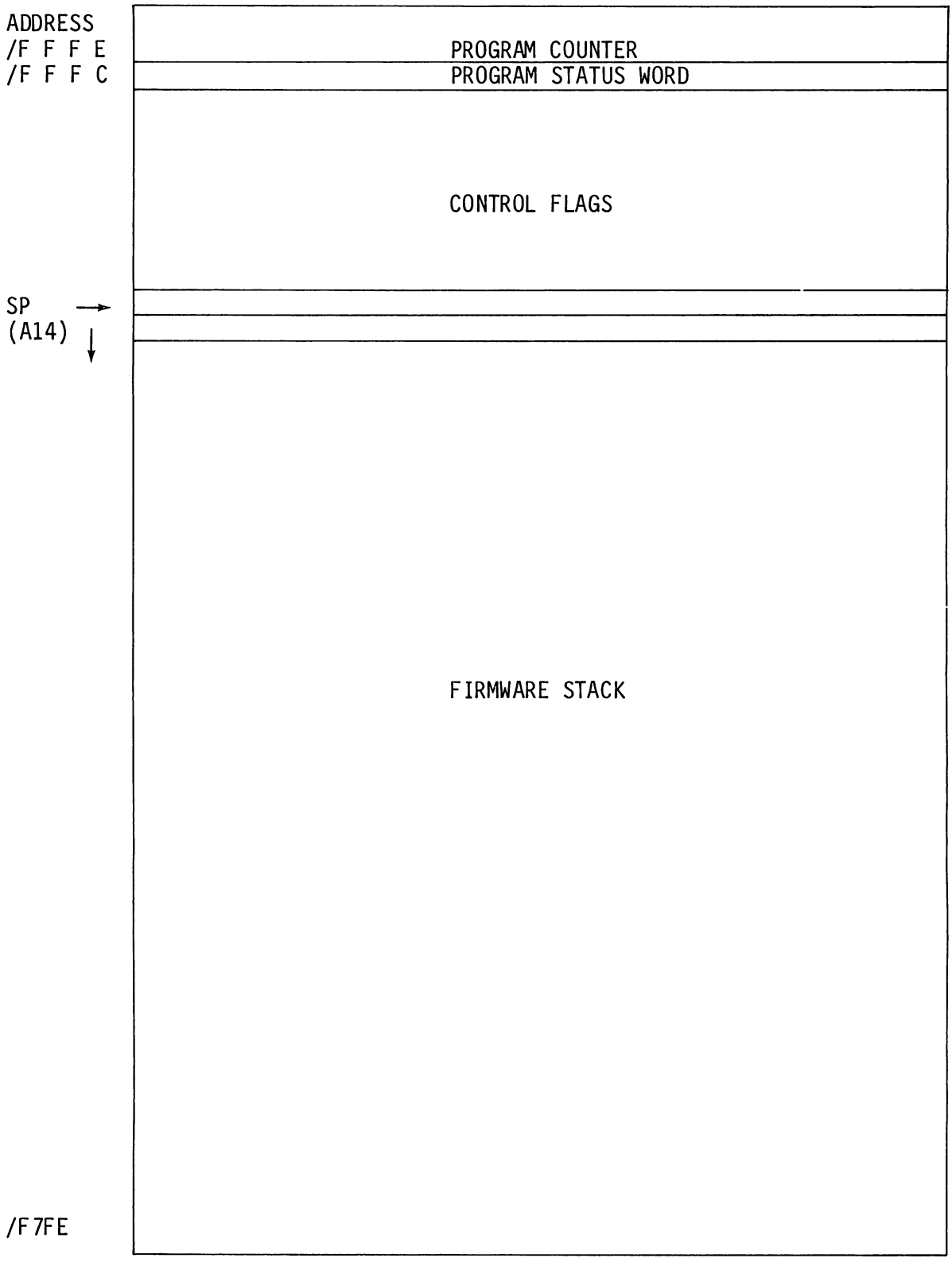


Table 2.15 OP/HHP RAM ALLOCATION

2.8 MICRODIAGNOSTICS

The CP1A microdiagnostic program resides in firmware memory and it consists of the following sections:

a) µP and A/D Bus tests
b) CU command test *
c) Software Memory tests
d) End of microdiagnostic routine
* Applicable only when the HHP is connected.

It is normally used when the CP1A is off line, i.e. is not executing System and/or User programs, and it checks that the basic functions of the CP1A are working before more comprehensive programs for testing the system may be loaded and executed.

It is triggered from either the HHP or the OP using the appropriate procedure, as detailed below:

a) HHP - Press the MCL button
Load the CU Address into the HHP Indicator
Simultaneously press the TEST and 0 buttons

b) OP - Set the thumbwheel switch to 0
Press the RUN button

Note: The microdiagnostic program is not cyclic so it must be retriggered to be re-executed.

2.8.1 µP AND A/D BUS TESTS

The following functions are tested:

a) A/D Bus (no line stuck at 0 or 1)
b) AN, OR and XR instructions
c) SLC, SLA, SRC, SLL and DRL instructions
d) The contents of the Condition Register (CR) are set to 11, i.e. overflow occured, due to the execution of an SLA instruction.

At the end of this section the contents of the scratchpad should be:

A0	/0000	A8	/8888
A1	/1111	A9	/9999
A2	/2222	A10	/AAAA
A3	/3333	A11	/BBBB
A4	/4444	A12	/CCCC
A5	/5555	A13	/DDDD
A6	/6666	A14	/EEEE
A7	/7777	A15	/FFFF

If an error occurs, error code '1' should be displayed on the HHP or OP and the program should stop.

2.8.2 CU COMMAND SET

The CU specified by the address set up on the HHP is tested with a Halt Command. If the CR is not set to 0, i.e. the command is not accepted, error code '2' should be displayed on the HHP and the program should stop.

2.8.3 SOFTWARE MEMORY TESTS

Pattern /0000 is written into every address and is read and checked.
Pattern /FFFF is written into every address and is read and checked.
The address number is written into every address and is read and checked.
If an error occurs, error code '3' should be displayed on the HHP or OP and the program should stop. In the case of the HHP, the operator may use the panel to read:

a) The address number of the faulty address in A0
b) The test pattern in A1
c) The read pattern in A2

2.8.4 END OF MICRODIAGNOSTIC PROGRAM

At the end of the microdiagnostic routine, code '4' should be displayed on the HHP or OP and the program should stop.

In the case of the HHP, the operator may use the panel to read the contents of the scratchpad. The contents should be as follows:

A0	/0000	A8	/8888
A1	/1111	A9	/9999
A2	/2222	A10	/AAAA
A3	/3333	A11	/BBBB
A4	/4444	A12	/CCCC
A5	/5555	A13	/DDDD
A6	/6666	A14	/EEEE
A7	/7777	A15	/FFFF

2.9 FIRMWARE FLOWCHART (FIGURE 2.10)

The flowchart outlines the functions of the firmware microprogram. The address references are those of the Assembler Listing.

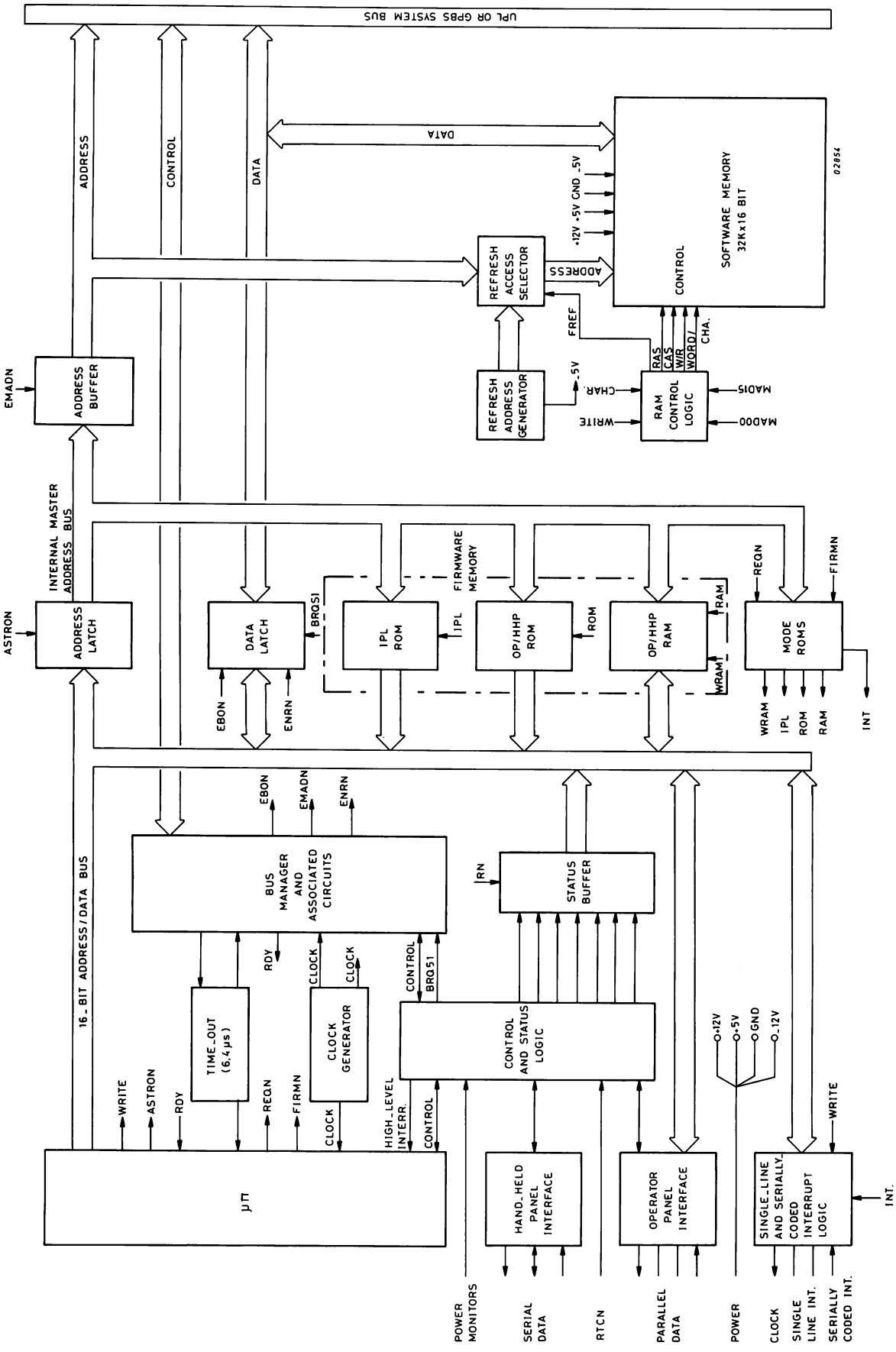


Figure 2.1 CP1A BLOCK DIAGRAM

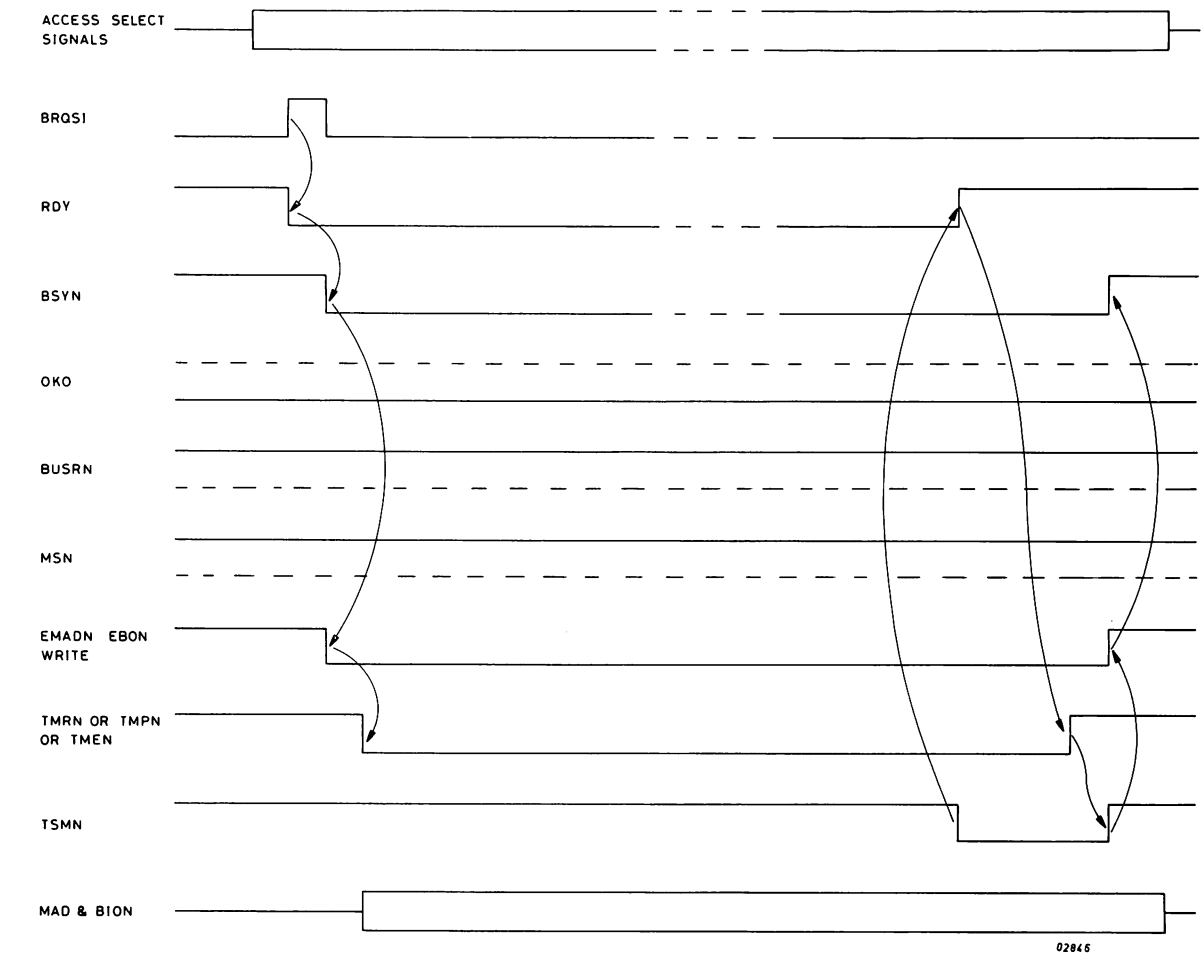


Figure 2.2 OUTLINE OF CP1A SYSTEM BUS ALLOCATION

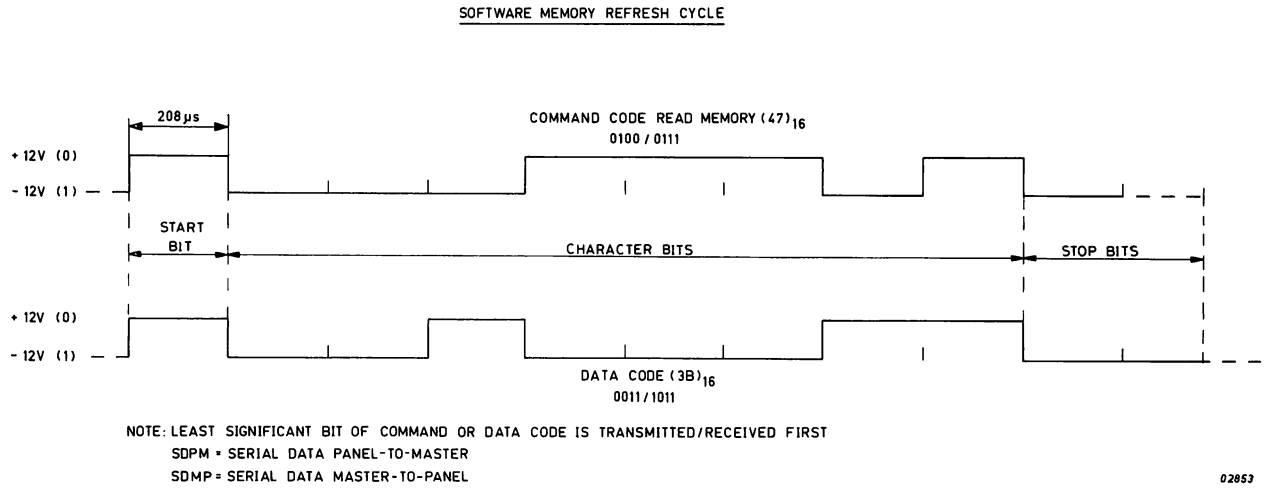
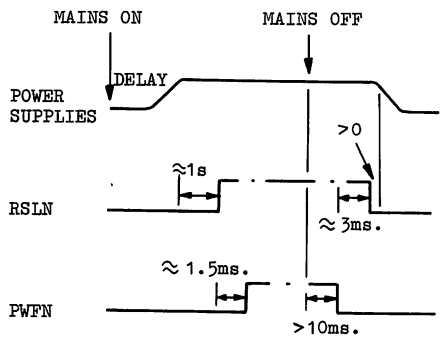


Figure 2.3 HHP COMMAND/DATA FORMATS

Note: Least significant bit of command or data code is transmitted/received first

SDPM = Serial Data Panel-to-Master
SDMP = Serial Data Master-to-Panel

P853 SYSTEM POWER CONTROL SIGNALS



Full details of the power supplies are given in the 6U6 rack and power supply field support manual. (P853 systems)

Figure 2.4 CP1A OPERATING STATES

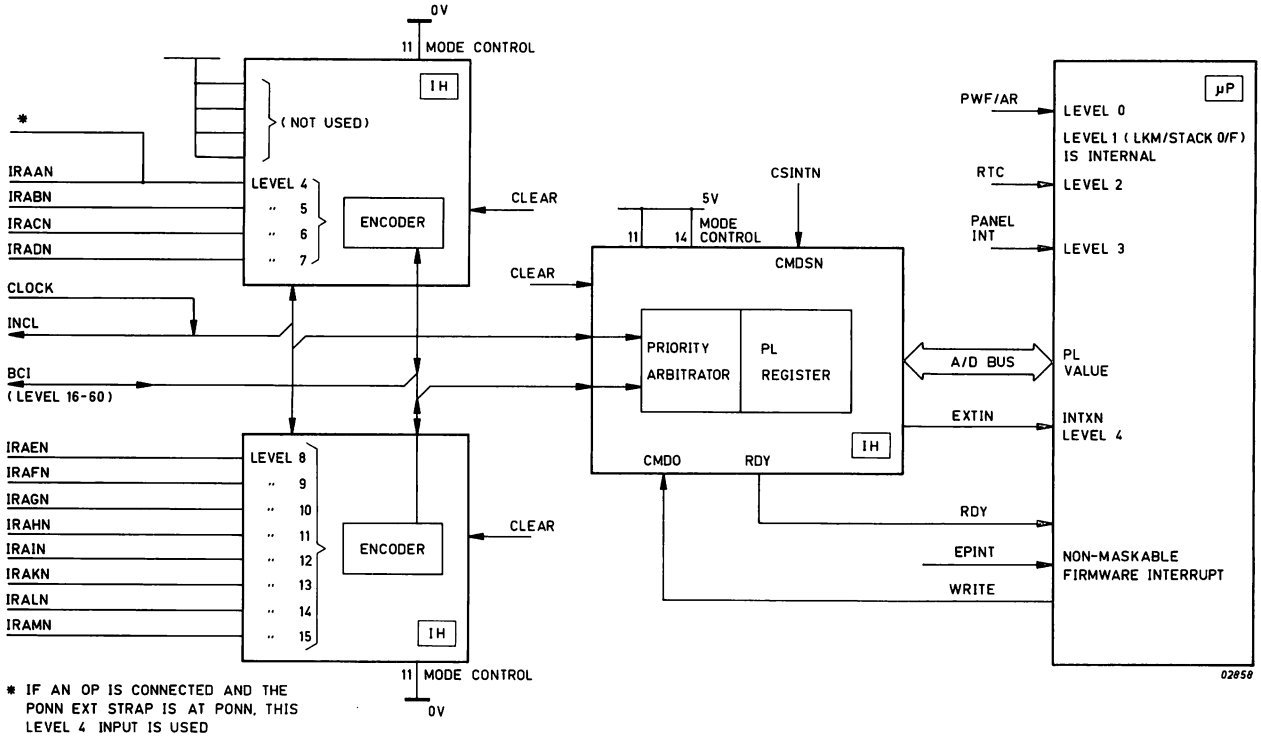
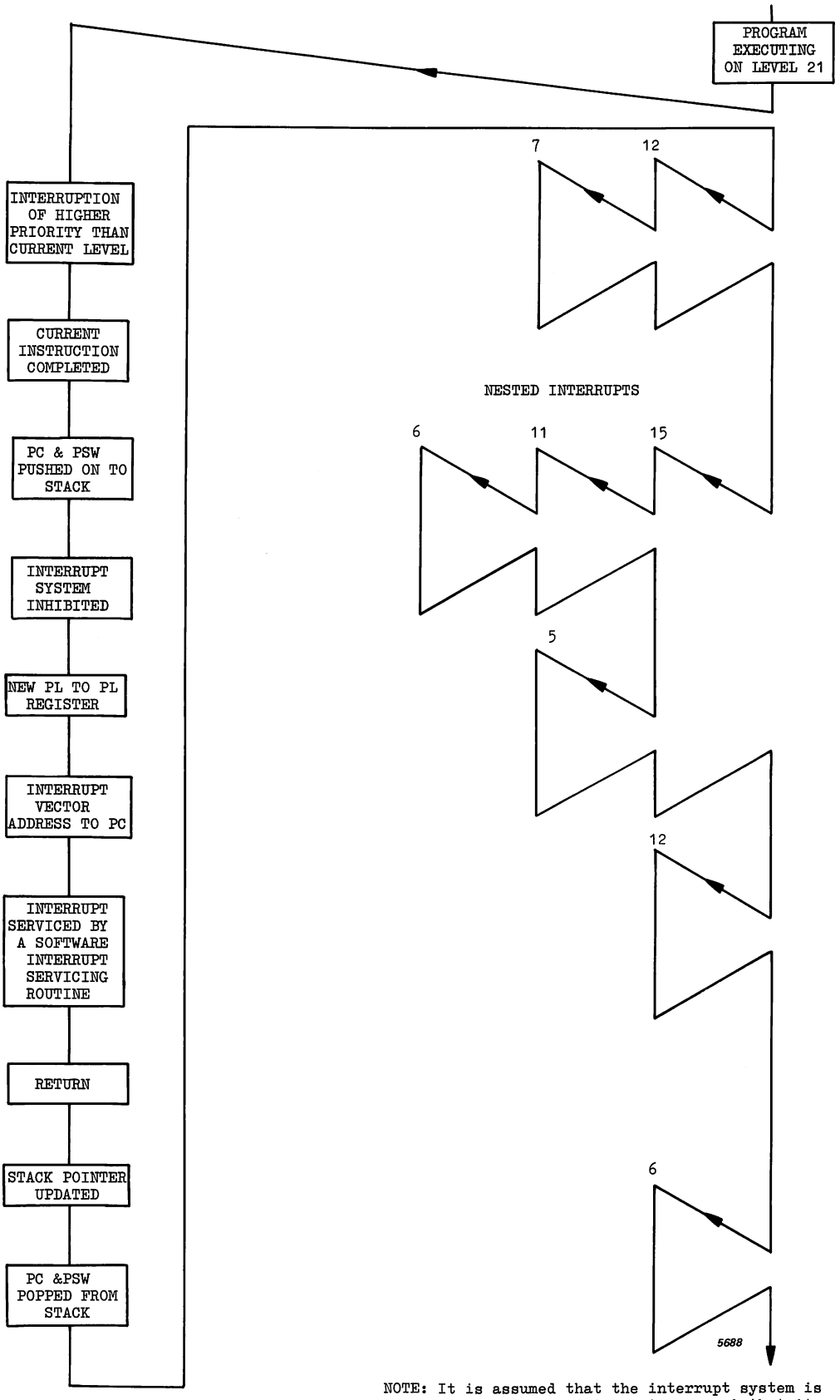


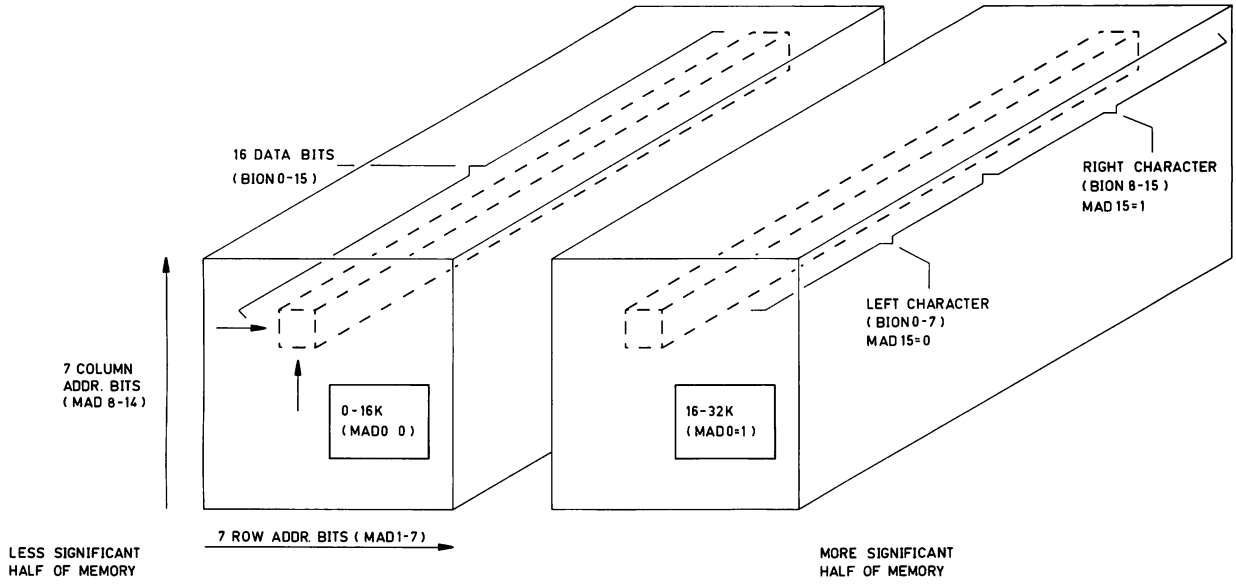
Figure 2.5 INTERRUPT HANDLERS AND BCI FORMAT

Note: In this application the distinction and stop bits are always set to 1.



NOTE: It is assumed that the interrupt system is enabled when an interrupt occurs & that it is reenabled at the start of the Software Interrupt Servicing Routine.

Figure 2.6 OUTLINE OF INTERRUPT OPERATION

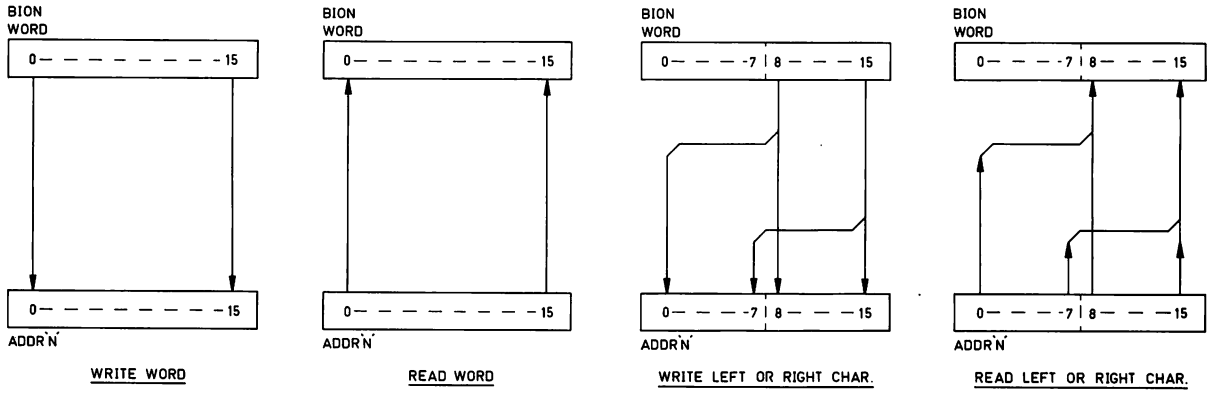


X = IRRELEVANT

WRITE	MAD 15	CHAR.	RAM FUNCTION	
1	X	0	WRITE WORD	MAD0=0 =0-16K MAD0=1 =16-32K
1	0	1	WRITE LEFT CHARACTER	
1	1	1	WRITE RIGHT CHARACTER	
0	X	0	READ WORD	
0	0	1	READ LEFT CHARACTER	
0	1	1	READ RIGHT CHARACTER	

02866

Figure 2.7 SOFTWARE MEMORY CONFIGURATION



NOTE: THE CP1A CAN ACCESS THE SOFTWARE MEMORY IN WORD MODE ONLY

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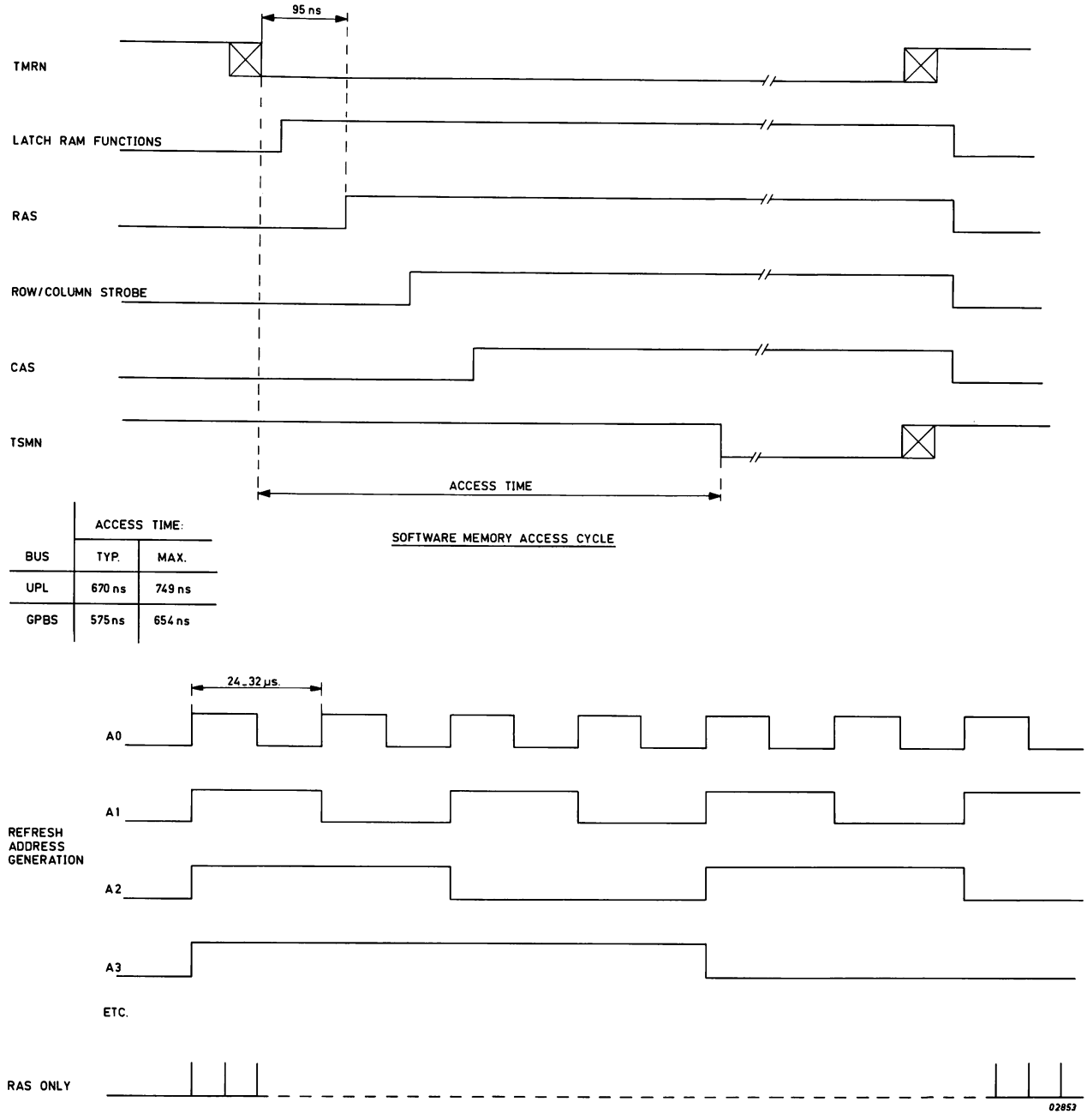
Note: The CP1A can access the Software Memory in word mode only.

Figure 2.8 WRITE/READ/WORD/CHARACTER ARRANGEMENT



	ACCESS TIME:	
BUS	TYP.	MAX.
UPL	670 ns	749 ns
GPBS	575 ns	654 ns

Figure 2.9 SOFTWARE MEMORY TIMING

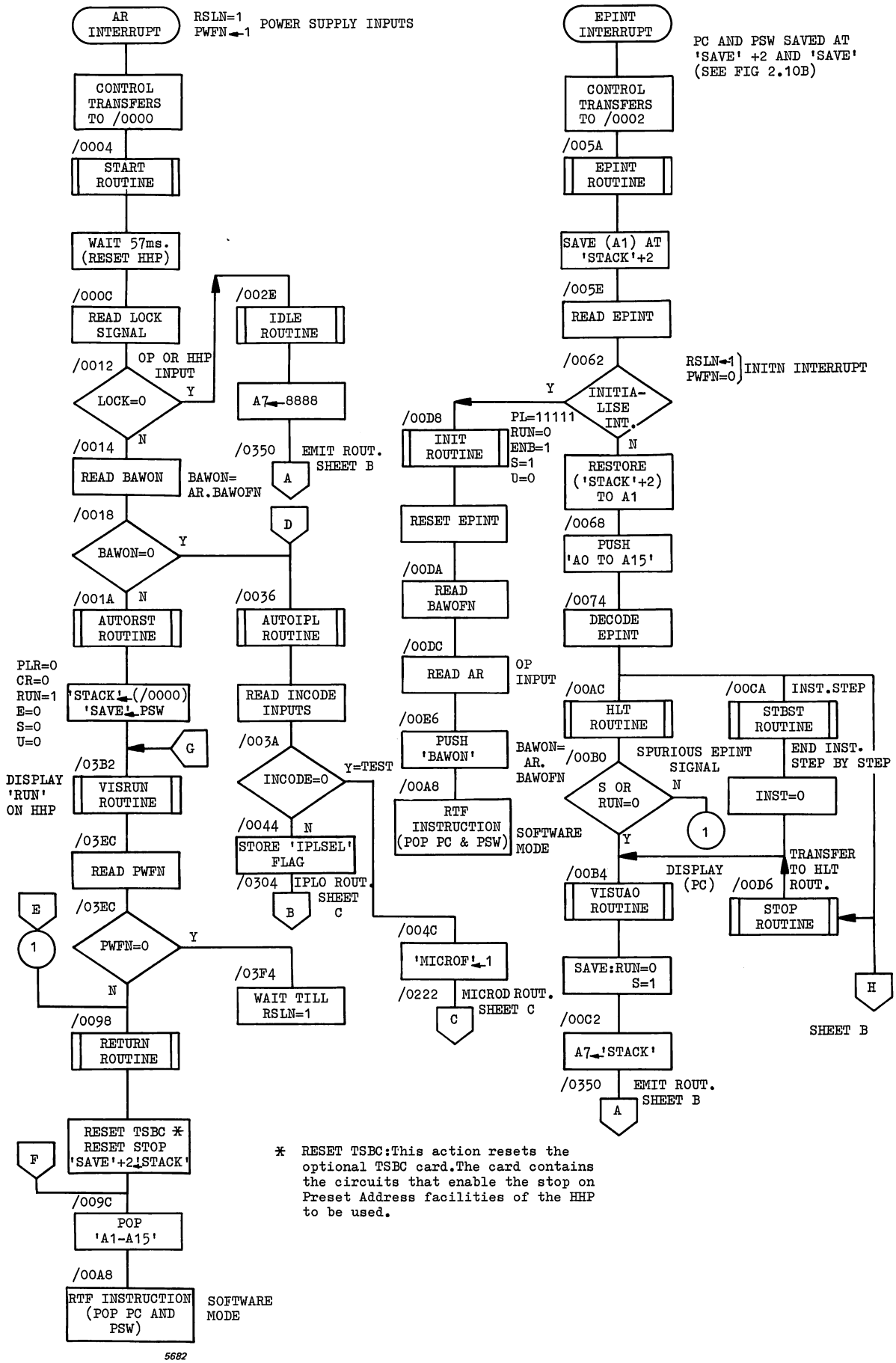


Figure 2.10 (A) FIRMWARE FLOWCHART

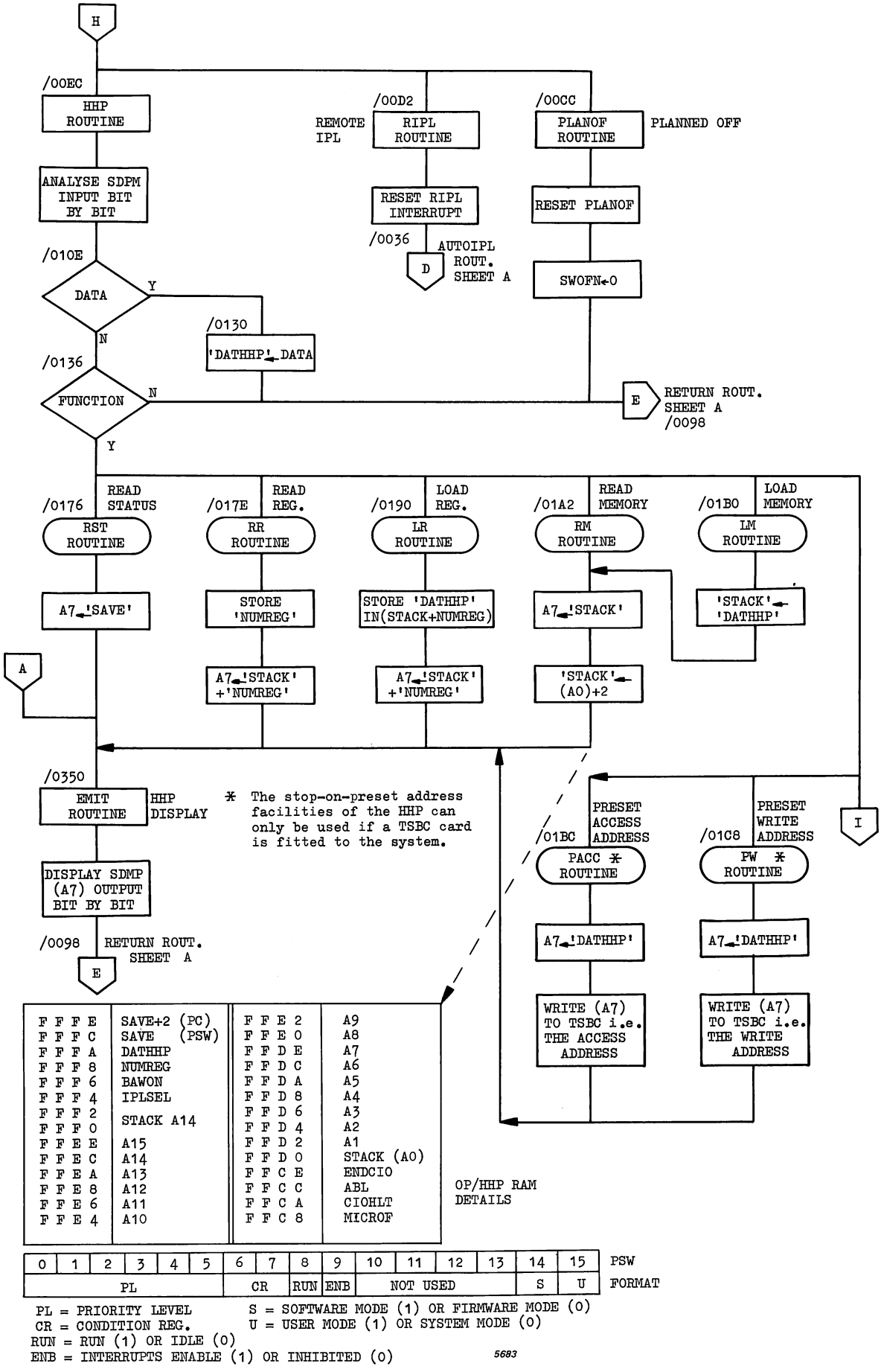


Figure 2.10 (B) FIRMWARE FLOWCHART

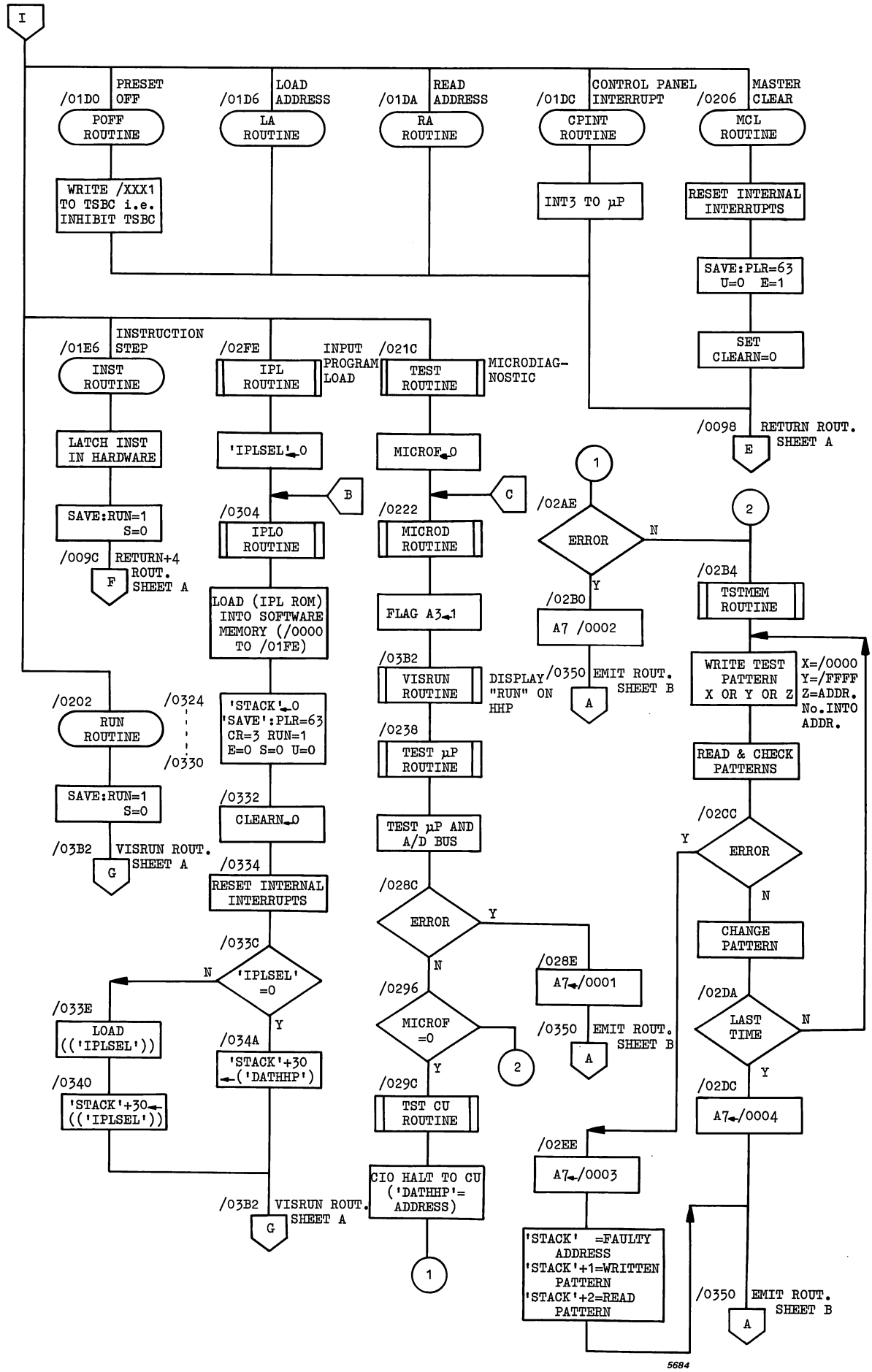


Figure 2.10 (C) FIRMWARE FLOWCHART

3 DETAILED DESCRIPTION

LIST OF ILLUSTRATIONS

LIST OF TABLES

3.1 INTRODUCTION

In this chapter references to circuit diagrams are by sheet number, e.g. reference ED3-4 means Fig. 4.1E, chip D3, pin number 4. References to Firmware and IPL Program Assembly Listings are by F and I titles and addresses, e.g. reference F/0098 means Firmware Assembly Listing, hexadecimal address /0098. Mode ROM decoding lists are shown in Tables 3.3 and 3.4.

Timing details are provided only for CP1A operations that are normally cyclic or which can be rendered cyclic by running simple programs.

3.2 POWER CONTROL (FIGURE 3.1 AND 4.1A)

Power is supplied to the CP1A in one of two ways:

a. By a power supply that has a battery back-up circuit. In this case the contents of the dynamic MOS Software Memory are preserved for up to two hours after a power failure.
b. By a power supply that does not have a battery back-up circuit. In this case the contents of the dynamic MOS Software Memory are destroyed by a power failure.

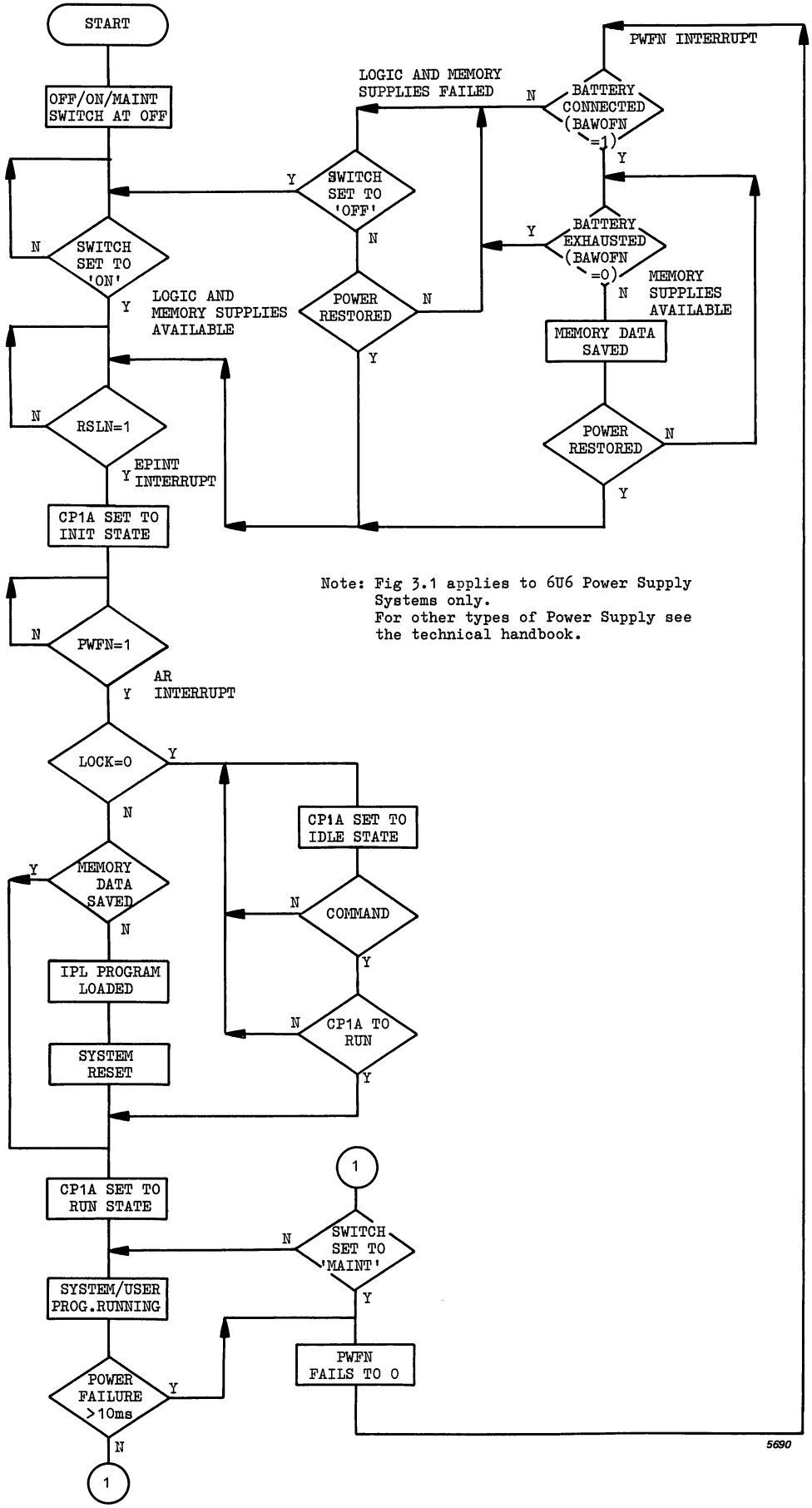
When a battery is fitted the +12VL, +5VL (logic) and +12VM, +5VM (memory) supplies are provided by independant circuits. In the event of a power failure the battery back-up circuits continue to provide the CP1A with +12VM and +5VM supplies. When a battery back-up circuit is not fitted the +12VL and +12VM supplies are provided by the same +12V source and the +5VL and +5VM supplies are provided by the same +5V source, i.e. a link connects the +12VL line to the +12VM line and another connects the +5VL line to the +5VM line. Note that the -5VM supply is generated on the CP1A card (Figure 4.1C).
Power control signals RSLN, PWFN and BAWOFN provide power status information which is used by the CP1A card for initialization, power monitoring, etc.

Note: This is true for systems that are fitted with 6U6 Power Supplies. For systems fitted with another type of power supply consult the appropriate technical manual.

3.2.1 POWER SUPPLIES SWITCHED ON (FIGURE 4.1A)

Supplies available:
When the 6U6 power control switch is set to ON there is a short delay while the switching controller of the power supply establishes control over the 6U6 circuits and then the +12V, +5V and -12V supplies rise to their nominal values. At this time control signals RSLN and PWFN are both at logical 0 (Figure 2.4).

Oscillator and frequency divider:
When the +5V supply is available to the CP1A, crystal oscillator Q2, Y1 generates clock signals. The nominal 10.52632 MHz signal is buffered in AT5 and is then divided by four in AT6. The outputs AT5-3 and AT5-6 are complementary 95ns clock signals that are fed to the RAM Control Logic. The outputs of AT6-13 provide a 380ns clock signal for the µP, Interrupt Handlers, Time-Out Circuit and flip-flop AM6-11.



Note: Fig 3.1 applies to 6U6 Power Supply Systems only.
For other types of Power Supply see the technical handbook.

FIGURE 3.1 CP1A POWER CONTROL

System reset conditions:
When the power supplies rise to their nominal values signal RSLN remains reset at true-earth potential (via relay contacts in the power supply). In the CP1A, signal RSLN at EL0-13 is inverted and then slugged by R33, C67. The slugged signal is inverted at EL0-12 and holds the following chips preset or reset: EL5, EC5, EB5, AK5, AM6, CR6, FK6. Signal RSLAN is inverted at EL0-9 and, via EN6-13 and EA4-7, signal RSL holds CLEARN lo. This signal holds the external system reset. Signal RSL holds AB2-15 reset and also, via FL6-3, the HHP (if connected). Note that the HHP is powered by the CP1A power supplies. The output of EN6-13 presets EE4-10 and is inverted at EL0-14. The CLEAR signal holds G4-16, H4-16 and K4-16 reset. The CLIRN signal holds FE4-4 preset lo.

Initialization sequence:
Approximately 1 sec. after the 6U6 power supplies have attained their nominal values RSLN goes hi. On the CP1A, RSLAN at ED3-3 goes hi. PWFN at ED3-2 is still lo so ED3-5 is clocked lo. This signal sets ED5-8 hi and EH5-6 lo. Signal EPINT interrupts the µP at AK3-30 and the µP switches to Firmware Mode (AK3-4 is set lo).

The µP then saves the contents of the PC and the PSW on the Firmware RAM as follows. On Figure 4.1A the µP sets WRITE hi, AMA lo and AMB hi (write memory access). It produces an ASTRO pulse and address /FFFE. On Figure 4.1B the trailing edge of the pulse strobes address /FFFE into the Address Latch. On Figure 4.1F the address is available at the OP/HHP RAM address inputs IMAD05-14. (Remember that bit 15 is reserved for selecting word or character operation of the Software Memory and that only ten bits are required for an addressing range of 1k word.)

In the next µP clock period the µP sets REQN lo. This signal enables Mode ROM AM4-13 and the input combination of the Mode ROMs sets CSRAMN lo. This signal enables AJ6-13 so that AJ6-11 (WRAMN) is set lo. On Figure 4.1F the OP/HHP RAM is enabled. The contents of the PC (Register A0) are placed on the A/D Bus and are written into address /FFFE of the OP/HHP RAM. The REQN signal is reset without requiring a RDY input. A congruent operation writes the PSW into OP/HHP RAM address /FFFC.

The µP then places address /0002 on the A/D Bus, sets WRITE lo, FETCHN lo and generates an ASTRO pulse, whereby address /0002 is strobed into the Address Latch. When REQN is set lo the input combination of the Mode ROMs sets AL4-7 (CSROMN) lo. On Figure 4.1F the contents of OP/HHP ROM address /0002 are placed on the A/D Bus and are supplied to the µP. In this instance the contents are the number /005A and this number is loaded into the PC so that control branches to Firmware Memory address /005A i.e. to the EPINT routine (see Figure 2.10A).

EPINT routine:
The µP reads and decodes instruction F/005A and then writes the contents of Register A1 into OP/HHP RAM address /FFD2 (this operation is not significant during a power-on sequence). In order to discover the source of the EPINT instruction F/005E is an RER /0080 instruction. On Figure 4.1B address /0080 (0000 0000 1000 0000 in binary) is strobed into the Address Latch. On Figure 4.1E the input of EN4-1 (IMAD 08) is set hi, but EN4-2, 3 and 4 are lo. When REQN at EN4-5 goes lo EN4-14 (RN) goes lo. At ED4-1,19 this signal enables the Status Buffer, whereby A/D Bus line AD 09 is set lo (INITN is lo). This zero is loaded into bit position 9 of Register A1. Instruction F/006A ANDs constant /0040 with bit position 9. When bit 9 is a zero the result is zero in Register A1. Instruction F/0062 causes control to branch to the Initialization routine (F/00D8).

Initialization routine:
Instruction F/00D8 is a WER /000D instruction which resets the EPINT interrupt. On Figure 4.1E EN4-1 and 2 are set lo and EN4-3 is set hi. Thus EN4-11 (WN) is set lo. On Figure 4.1F this signal enables FN6-6, so the next HI clock pulse clocks FE4-3 whence SDMP is reset. On figure 4.1E signal WN enables EE3-19 (EE3-1 is enabled because DMANSN is hi at this time). Pins EE3-11 and 13 are lo and pins EE3-15 and 17 are hi. Thus IMADA 11 and IMADA 14 are set lo. These signals preset ED3-5 and ED3-9 hi and the EPINT interrupt is reset. IMADA 14 presets EE5-5 hi.

Instruction F/00DA is an RER /0080 instruction that transfers the data at the input of the Status Buffer to Register A1. Instruction F/00DC is an RER /00F6 instruction that transfers Incode Data (Figure 4.1F) to Register A2. (Enable signal EINCODN is generated via the Mode ROMs.) The μP ANDs the contents of Register A1 with constant /0002 to discover the state of BAWOF (see ED4-15). If signal BAWOFN is lo (as it should be at this stage of a power-on sequence) then BAWOF is hi and instruction F/00DE results in Register A1 containing /0002. In this case instructions F/00E0 and F/00E2 are executed and Register A2 is loaded with zero. Instruction F/00E4 ANDs the Incode Data with /0080 to test if signal AR from the OP is hi (this is not significant during the power-on sequence). BAWOFN is ANDed with AR and the result is stored as BAWON. Control then branches to the RTF instruction at F/00A8. This instruction restores the saved values of the PC and PSW and a Halt interrupt (see section 3.6) sets the μP to Idle mode. During a power-on sequence nothing further should happen until the PWFN signal from the power supply goes hi.

AR interrupt:
About 1.5 mS after RSLN goes hi PWFN goes hi. On Figure 4.1E signal PWFN is inverted and slugged by R10 and C11. The slugged signal is again inverted at EA5-3 and PWFAN is supplied to the Status Buffer at ED4-17. On Figure 4.1A it provides an AR interrupt at AK3-28. The μP switches to Firmware Mode and places address /0000 in the PC. The μP reads the contents of Firmware Memory address /0002 and places this number (/0004) in the PC. Thus control branches to Firmware Memory address /0004 i.e. to the Start routine.

Start routine:
Instruction F/0004 loads register A6 with number 10,000 (decimal). Instruction F/0008 repeatedly subtracts 1 from the contents of Register A6 until Register A6 contains a negative number. This count loop provides a delay of about 57mS to allow the HHP to initialize (if connected). Then instruction F/000C reads Incode Data (Figure 4.1F) to discover the state of the LOCK signal from the OP or the HHP. If LOCK is hi (indicating that either the OP REMOTE switch or the HHP LOCK switch is operated) then the routine reads BAWON to decide whether to initiate an Automatic Restart or an Automatic IPL routine. In this case, where the power supply has been switched ON from the OFF state, it is necessary to load the IPL Program into Software Memory. BAWON is lo and control branches to the Automatic IPL routine. When LOCK is lo control must be given to the OP or HHP, so control branches to the IDLE routine (F/002E). This routine loads /8888 into Register A7 and then control branches to the EMIT routine (F/0350). The EMIT routine transfers number /8888 to the HHP display (if the HHP is connected). How this is done is described is section HHP INTERFACE. At the end of the routine control branches to the RETURN routine (F/0098).

Return routine:
Instruction F/0098 is an RER /00F4 command that resets the TSBC card (see the note on Figure 2.10A). On Figure 4.1B address /00F4 is loaded into the Address Latch. On Figure 4.1E EN4-11 is set lo to enable EE3-19, whose output at EE3-18 (BRQA) is hi due to signal AMA from the μP being hi. On Figure 4.1A the inputs to AB2-3 and 2 are both hi. Thus an external register access is selected. The output of AM4-10 is set lo so the next HI clock pulse sets AM6-8 hi, which in turn clocks AM6-5 hi (the BM signals are shown in Figure 2.2). Address /00F4 is supplied to the system bus MAD lines and is decoded by the TSBC card which resets itself. The operations of the BM and System Bus are described in detail in later sections.

Instruction F/009A resets the STOP input (if it was set). On Figure 4.1E instruction WER /001D sets EE3-7 lo and this signal presets EE5-5 hi (if it was already set lo).

The rest of the Return routine reloads the scratchpad registers and then executes an RTF instruction.

AutoIPL routine:
When LOCK = 1 and "BAWON" = 0, instruction F/0036 reads the Incode Data into Register A1 where it is ANDed with /003F. If the result is zero, i.e. the Incode Data is zero, control branches to the TEST routine. When the result is not zero, i.e. neither the OP thumbwheel switch nor the straps are set to call up the TEST routine, then the Incode Data set the device parameter index for the IPL Program. Similarly, if the OP is not connected but the DCCU input is used, then the Incode Data set the device parameter index for that device. Full details of the IPL Program loading options are given in section IPL PROGRAM.

Instruction F/0038 eliminates the two irrelevant high-order bits of the Incode Data. Instruction F/003A checks for the value zero. Instruction F/003C eliminates all but the four low-order bits of Register A1 (four bits provide sixteen possible device parameter codes). Instruction F/0040 inverts the device code and it is then shifted left by one place. The result is the device parameter address of the IPL Program, which is then stored in address /FFF4 of the OP/HHP RAM ("IPLSEL" - see Figure 2.10B). Control then branches to the IPL0 routine.

IPL0 routine:
This routine loads (bootstraps) the contents of the IPL ROM into the first 256 locations of the Software Memory. Once it has been loaded the IPL Program automatically loads a system/user program(s) from the device specified by the "IPLSEL" code stored in OP/HHP ROM address /FFF4. (It is useful to remember that the IPL Program occupies 256 Software Memory locations but is stored as 1024x4-bit half-characters in the IPL ROM. The bootstrap must assemble each 16-bit word before it writes it into Software Memory).

Instruction F/0304 loads zero into Register A3 (the RAM address counter), F/0306 loads number /2000 into Register A4 (first address of the IPL ROM) and F/030A loads Register A5 with number /0004 (half-character counter). Instruction F/030C loads the contents of the contents of Register A4 into Register A1, i.e. the contents of IPL ROM address /2000. F/030E ANDs /000F with the contents of Register A1 to eliminate all but the l.s. half-character, F/0310 left shifts the contents of Register A2 four places (irrelevant at this time) and F/0312 loads the first IPL ROM half-character into Register A2. Instruction F/0314 increases the IPL ROM address count by 2 (to /2002) and F/0316 subtracts 1 from the half-character count (which now contains 3). Since the half-character count is not zero, control branches to F/030C. Another half-character is loaded from IPL ROM to Register A1, the contents of Register A2 are left shifted to make room for the new half-character, which is then loaded, and so on until four half-characters have been loaded into Register A2.

Instruction F/031A then loads the contents of Register A2 into the address specified by the contents of Register A3 i.e. the first IPL Program word is loaded into Software Memory address /0000. Instruction F/031C increments the Software Memory address count in Register A3 by 2 (to /0002) and F/031E counts how many words have been loaded.

The two program loops are repeated until the complete IPL Program has been stored in Software Memory. Instruction F/0324 loads /0000 into Register A1. Instruction F/0326 stores the new PC value of /0000 into OP/HHP RAM address /FFD0 ("STACK" - see Figure 2.10B) and F/032A stores the new PSW value of /FF80 (PLR = 63, CR = 3, RUN = 1, ENB = 0, S = 0 and U = 0) in address /FFFC ("SAVE"). Note that these values are not used until the end of the RETURN routine. Instruction F/0332 is WER /00F8. On Figure 4.1A the inputs to the Mode ROMs set ENRAZN lo (AM4-9). On Figure 4.1E this signal triggers EL5-9 (EL5-10 is lo at this time) and, via EN6-13 and EA4-7, a 20µS CLEARN pulse is generated to reset the system. The next instruction reads the number /20D3 into the µP. This number is decoded to reset the internal interrupts. Register A3 is then reset to /0000 and the value of "IPLSEL" (IPL Program device parameter address) is loaded into Register A1. If "IPLSEL" is /0000 control branches to the PANEL routine (F/0346). This is relevant when the IPL Program is loaded by the HHP. The contents of Register A2 are placed in OP/HHP address /FFEE ("STACK"+30) to give a new value to A15 and then control branches to the VISRUN routine (/03B2).

If "IPLSEL" is not /0000 then "IPLSEL" is loaded from Register A1 to Register A2 and the contents of Register A2 are stored in OP/HHP address /FFEE to provide the device parameter address of the IPL Program.

The VISRUN routine is covered in the HHP INTERFACE section. At the end of this routine control branches to the RETURN routine (F/0098). This has already been described but when the contents of Registers A1 to A15 are restored and the RTF instruction restores the PC and the PSW, control automatically branches to the start address of the IPL Program (address /0000). In a normal situation this routine will load an initial program from the specified device into Software Memory.

3.2.2 POWER FAILURE

Power failure interrupt:
When a power failure of longer than 10mS occurs the power supplies are maintained for a further 5mS or so before falling to zero. About 10mS after a power failure, signal PWFN from the power supply goes lo (see Figure 2.4). On Figure 4.1E signal PWFAN at EA5-3 goes lo and on Figure 4.1A a level 1 interrupt occurs at the AK3-28 input of the µP. The µP waits until the current instruction has been completed and then initiates an internal power-fail routine. This routine saves the PC and PSW on the Software Memory stack and then branches to the start address of the power failure interrupt handling routine. Note that this routine is a software program whose composition will depend upon the requirements of the system.

The internal power-fail routine works as follows. The µP sets WRITE hi, AMA lo and AMB hi but FIRMN remains lo (write into Software Memory). It places the contents of the SP (next available stack address) on the A/D Bus and the address is clocked into the Address Latch by an ASTRON pulse.

The input combination of the Mode ROMs sets AM4-10 lo and the next HI pulse sets AM6-9 lo and AM6-8 hi. The positive-going output of AM6-8 clocks AM6-13 so that AM6-5 (BRQSI) is set hi.

This signal strobes the states of BRQA and BRQB into the BM. In this case BRQA is lo and BRQB is hi so the BM is set up for a memory access. The BM sets RDY lo and sets BSY lo to inform the system that the System Bus is busy. It then sets EMADN and EBON lo and WRITE hi. When EMADN goes lo it resets AM6 to that BRQSI is reset lo; it sets the µP input DMARQN lo to request use of the bus (the µP will grant the request and set DMANSN lo after the bus cycle); it enables EA5-1 so that its inputs can be accepted; and on Figure 4.1B it gates the address through the Address Buffer and onto the System MAD lines. The address is also present at the Row/Column Address Selector (Figure 4.1C). A detailed description of the RAM Control Logic and Software Memory operation is given in section SOFTWARE MEMORY. On Figure 4.1B the EBON signal enables the Data Latch so that when the µP places the contents of the PC on the A/D Bus it is latched into G1, H1, J1 and K1 (signal ENRN remains lo during a write operation). The WRITE signal of the BM is supplied to the RAM Control Logic to select a write operation. On Figure 4.1E, the inverse output of A5-16 is lo to set word operation. The setting of MAD 15 is irrelevant during word operation.

The BM then sets TMRN lo, which initiates a write sequence in the RAM Control Logic (Figure 4.1C) and also triggers the Time-Out Circuit (Figure 4.1A). On Figure 4.1A pin AC3-8 is set hi and triggers monostable AB5- whose output at AB5-5 goes hi for a nominal 6.8µS (the time-out period). If this period elapses and no TSMN signal has been received from the RAM Control Logic, monostable AL5 is triggered and produces a nominal 0.92µS pulse that provides a TSMN signal to free the Bus. The output pulse of L5-4 is supplied to the µP and is interpreted as an Address Recognition Error. On Figure 4.1C the RAM Control Logic strobes the access conditions into the RAM Function Latch and multiplexes the row and column co-ordinates to the RAM (Figure 4.1D). When the contents of the PC have been written into the selected address a TSMN signal is generated (Figure 4.1C). The timing of this signal depends upon the type of System Bus (UPL Bus or GPBS). On Figure 4.1A signal TSMN resets RDY hi and soon afterwards TMRN is reset hi. When the TSMN signal reverts hi EMADN, EBON and WRITE are reset and, finally, BSY is reset hi.

A congruent operation saves the PSW in the next available stack address of the Software Memory. The PC is then loaded with /0000. This address is placed on the A/D Bus, is latched into the Address Latch, and is passed via the Address Buffer to the Software Memory address inputs. The WRITE output of the µP is lo so the RAM Control Logic is set up to perform a read access. The contents of Software Memory address /0000 (the start address of the power failure interrupt handling routine) are loaded into the PC and control branches to the start address of the routine. Note that the routine is a software program whose composition will depend upon the requirements of the system.

Software memory contents preserved:
If a battery back-up circuit is fitted to the 6U6 Power Supply and provided the battery is connected and is not exhausted, the battery will provide the CP1A with +12VM and +5VM power supplies during a power failure and the contents of the Software Memory will be preserved. In this case BAWOFN will remain hi throughout the power failure and will be hi when the power supplies are restored.

Software memory contents destroyed:
If a battery back-up circuit is not fitted or if the battery is disconnected during a power failure or if the battery becomes exhausted during a power failure, the contents of the Software Memory are destroyed. In this case BAWOFN will be lo when the power supplies are restored.

3.2.3 POWER RESTORATION

The operations of the CP1A are similar to the operations during a power-on sequence, except that BAWOFN may be hi or lo depending upon whether the Software Memory contents were preserved or destroyed. If the Software Memory contents were preserved then BAWON will be hi (assuming that the OP RESTART button was operated - if the OP is not connected a resistor pulls the AR input hi). In this case there is no need to reload the Software Memory. If, however, the BAWON signal is lo due to the contents of the Software Memory having been destroyed, the Software Memory will have to be reloaded with the IPL Program and the system/user programs. The details of the alternative courses of action are shown in Figure 2.10 and the Firmware Assembly Listing.

The PWFN test on Figure 2.10A is to detect the condition PWFN lo/RSLN hi i.e. after the trailing edge of PWFN. When this condition is detected the CP1A must wait for a positive-going edge of RSLN.

3.3 IPL PROGRAM

The device parameters required by the IPL Program are loaded into Register A15 in two ways:

(a) Via the Incode Data lines - this method is used for automatic IPL operation at power-on and power-restoration, for IPL operation from the OP, and for IPL operation from a DCCU.
(b) From the HHP keyboard.

Case (a):
Referring to Figure 2.10(a), the instructions F/0036 to F/0044 read the Incode Data, convert it to a specified IPL Program address in the range /01FE to /01E0, and store the specified address at OP/HHP RAM address /FFF4 ("IPLSEL"). For an OP, the Incode Data has the form xxxxxx (as set by the OP thumbwheel switch). For an automatic or DCCU input, the Incode Data has the form 11xxxx, where the m.s. bits are set to ones by pull-up resistors and xxxx is set by the Incode Data straps. When the IPL Program has been loaded, the specified IPL Program address contains the required device parameters. Near the end of the IPL routine (Figure 2.10(c)), an "IPLSEL" flag test causes instructions F/033E and F/0340 to store the contents of the contents of "IPLSEL" (the device parameters) in OP/HHP RAM address /FFEE ("STACK" +30). After the VISRUN routine, the RETURN routine loads the contents of "STACK"+30 into Register A15.

Case (b):
Referring to Figure 2.10(a), the instruction at F/0130 stores the HHP keyboard data (device parameters) in OP/HHP RAM address /FFFA ("DATHHP"). Near the end of the IPL0 routine (Figure 2.10(c)) an "IPLSEL" flag test causes the contents of "DATHHP" to be stored in OP/HHP RAM address /FFEE ("STACK"+30). After the VISRUN routine, the RETURN routine loads the contents of "STACK"+30 into Register A15. The format of the device parameters is shown in Table 3.1.

BITS:	SIGNIFICANCE:
0=1	C.U. reads 16-bit words when on progr. channel (ex floppy disk)
1=1	Disk
ALSO 3=1	Programmed Channel
3=0	IOP Channel
2=1	Moving Heads
2=0	Fixed Heads
1=0	Others
ALSO 2=1	ROM IPL or DMA
ALSO 3=1	ROM IPL
3=0	DMA
2=0	Sequential Devices or CDC Disk
ALSO 3=1	Programmed Channel
3=0	IOP Channel
4 - 7	BIO Bits
8=1	Multi-device Controller
8=0	Single-device Controller
9	Must be set for moving head disk with absolute seek
10 - 15	C.U./Device Address

Table 3.1 FORMAT OF DEVICE PARAMETERS

3.3.1 AUTOMATIC LOADING

This occurs during a power-on sequence if LOCK =1, during a power-restoration sequence in which the contents of the Software Memory were destroyed (BAWON = 0) and LOCK = 1. The operations that load the IPL Program are described in section POWER CONTROL.

3.3.2 HHP LOADING

Provided that the HHP is unlocked (LOCK = 0), the IPL Program can be loaded under the control of the HHP. The device parameters are selected by operating the 0 to F key(s), and the IPL button is pressed. The device parameter data is sent to the CP1A on the SDPM line and generates an EPINT, whereby the device parameter data is stored at OP/HHP RAM address /FFFA ("DATHHP") - see Figure 2.10(a) and F/00EC. When the CP1A receives function code 44 (IPL) the EPINT is decoded and control branches to the IPL routine (Figure 2.10(c) and F/02FE). The contents of OP/HHP RAM address /FFF4 ("IPLSEL") are set to zero. The IPL Program is then loaded into the Software Memory in the same way as was described in section POWER CONTROL. At the end of the IPL0 routine "IPLSEL" is zero so "DATHHP" is stored in OP/HHP RAM address /FFEE ("A15") to provide the device parameters. The VISRUN routine sends the RUN code on the SDMP line so that "run" is displayed on the HHP. The RETURN routine switches the µP to Software Mode. The loaded IPL Program normally loads an Initial Program that, in turn, loads system/user programs from a selected peripheral device.

3.3.3 OP LOADING

In this case the device parameter data is set on the thumbwheel switch of the OP, and the RUN button is pressed. On Figure 4.1F, the RUNN signal at Conn. J4-A2 is set lo. Signal FIPLEXN goes lo to generate an EPINT which interrupts the µP. When the µP has discovered the source of the interrupt EPINT is reset and control branches to the AUTOIPL routine. This routine reads the device parameter index that is set on the Incode Data lines, converts it to an IPL Program address, and then branches to the IPL0 routine. The rest of the sequence is the same as then one previously described.

3.3.4 DCCU LOADING

The IPL Program can be loaded under the control of a DCCU. In this case the four Incode Data straps are set to one of sixteen possible device parameter indices. On Figure 4.1E, signal RIPLN is set lo and is buffered at EA4-9. This signal sets EK5-11 hi so that ED3-9 is clocked lo and generates an EPINT. When the µP has discovered the source of the interrupt the IPL Program is loaded into Software Memory as previously described.

3.3.5 EXAMPLE OF IPL PROGRAM OPERATION

A complete description of the IPL Program and all its applications is outside the scope of this manual, but an example of how it might be used with the CP1A is given. It is assumed that an Initial Program is stored on cylinder no. 0, record no. 1 (physical sector 3) of a fixed disk that is fitted to an X1215 Disk Drive Unit No. 0. The address of the C.U. is assumed to be /0002. If the Initial Program is to be loaded using the HHP, the format of the device parameters is 0110 0011 1110 0010 (/63E2). When this value is selected and the IPL button is pushed, the CP1A loads the IPL Program. When (on Figure 2.10A) the RTF instruction of the RETURN routine is executed, the device parameters are in Register A15, and control branches to Software Memory address /0000.

The first instruction of the IPL Program (instruction I/0000) causes control to branch to I/0082. Instructions I/0082 to I/00AA compute the Software Memory size and transfer a section of the IPL Program to the top end of the Software Memory. This action is required for a DMA UPL disk system, but need not detain us here. Instructions I/00AC to I/00B0 load Registers A2, A3 and A4 with the addresses of INR, CIO and SST instruction codes that are used later in the program.

Instructions I/00B2 loads the device parameters from Register A15 to Register A6. The contents of Register A6 are anded with /3F to keep only the C.U. address. The address is then ored with the contents of Registers A2 and A3 to form INR and CIO instructions. The C.U. address is also stored in location I/0072 (HIO).

Instruction I/00BE loads the device parameters into Register A7, whereby shift and test instructions discover that a multiple D.U. controller is to be used. An AND instruction then saves the C.U. address in Register A6.
Instruction I/00C6 forms a complete SST instruction in address I/007A, i.e. an SST instruction having the required C.U. address. The four l.s. bits of Register A6 (the C.U. address) are shifted left one place to form the IOP and IOP Subchannel addresses. Two ORS instructions then form WER codes in addresses I/0042 and I/0044, respectively. These codes are for when the IOP is initialized.

The shifted device parameters that are in Register A7 are loaded into Register A1 by instruction I/00D2. This action places the sector no. bits into the correct positions for a read CIO command. Instructions I/00D4 and I/00D6 load Registers A5 and A6 with the data length (/0050) and disk program load address (/0080) data. Note that the data length for an X1215 operation is 205 words, so instruction I/00D4 is superfluous. Register A8 is then loaded with the contents of Register A6, to which 4 is added (/0084). The new number is the start address of the loaded program. Instruction I/00E2 saves the loading address (/0080) in Register A14.

Instruction I/004E shifts right the contents of Register A7 (shifted device parameters) to align Bit 1 with the Bit 0 position. A bit test determines that a disk operation is required so control branches to I/0030. Instruction I/0030 aligns Bit 2 with the Bit 0 position, and a bit test determines that a moving-head disk is to be used. Register A1 is loaded with the Seek-to-Zero code (BIO 14 + 15 set to 1), and a CIO instruction causes the selected C.U. to seek to cylinder no. 0.

Instruction I/0038 loads Register A1 with the device parameters, which are then shifted to align the physical sector code at bit positions 10 to 13. An AND instruction eliminates bits that are not code bits, and Register A5 is loaded with the number of words that are to be transferred (205).

Instructions I/0042 and I/0044 write the data length and start address to the IOP to initialize the unit. Instruction I/0046 sends an SST instruction to the C.U. to set it to the Inactive State, and instruction I/0048 reads successive words from the disk into addresses /0080 to /0080+ /00CD. If the read command is not accepted, the program loops on address I/004A. The contents of Register A7 are shifted to align the IOP bit (Bit 3) with the sign bit position. Since the contents of A7 are positive (Bit 3 = 0), control branches to I/007A.

Instruction I/007A performs an SST command to the C.U. to reset it to the Inactive State, and also to read the Status Word into Register A7. If the command is not accepted, the program loops on I/007C. When the command is accepted, control branches to I/0006. Instruction I/0006 checks that none of the Data Fault, Throughput Error, or Not Operable bits are set and, if none are, control branches to the start address of the loaded program. Note that the Enable bit of the PSW is set to zero before the IPL Program is executed (see Figure 2.10C /0342 to /0330), so the CP1A interrupt system is inoperative during the program.

Note: To calculate the values of the device parameter index strap settings:
1. Shift the least significant bits of the required IPL device parameter address one place to the right.
2. Subtract the result from /FF.
3. The four least significant bits of the answer give the values of the strap settings.

(Only the last sixteen device parameter addresses of the IPL program are valid for use in this calculation.)

3.4 HHP INTERFACE

3.4.1 RTCE INPUT

When the RTC switch of the HHP is operated the Real Time Clock Enable (RTCE) signal at Conn. J3-A2 is set hi. On Figure 4.1E the Real Time Clock Not (RTCN) signal at Conn. J1-B8 is buffered and inverted to RTC at EA5-9. On figure 4.1A the output of AJ5-3 goes lo each time that RTC goes lo and, provided ENB = 1 and no higher level interrupt is being serviced, the µP is interrupted at AK3-26 (INT2N). The µP completes the current instruction and then loads the PC with address /0004. The µP places address /0004 on the A/D Bus and reads in the start address of the Real Time Interrupt handling routine. Note that this routine is a software program whose composition will depend upon the requirements of the system. In some systems the RTC is not used.

3.4.2 PANEL INTERRUPT (INT)

When the INT button of the HHP is pressed the HHP sends function code 46 to the CP1A. This code generates an EPINT in the usual way and the fact that the interrupt was generated by the HHP is decoded at address F/0136. The HHP routine then tests for Panel Interrupt at F/0104 and branches to /01DC. After a delay the routine produces instruction WER /0040 which, on Figure 4.1E, sets the output of EN4-9 (INTN3N) lo. On Figure 4.1A this signal interrupts the µP at AK3-27. The µP completes the current instruction and, provided that ENB = 1 and no higher priority interrupt is being serviced, control branches to Software Memory address /0006 i.e. to the start address of the Panel Interrupt handling routine. Again, the composition of the routine will depend upon the requirements of the system.

3.4.3 INSTRUCTION STEP COMMAND (INST)

When the INST button of the HHP is pressed and the HHP is not locked, function code 49 generates an EPINT (via the SDPM line). The interrupt is decoded and control branches to Firmware Memory address F/01E6. On Figure 4.1E instruction F/01E6 (WER /001B) sets IMAD08 and IMAD09 lo and WRITE A hi. Thus EN4-11 is set lo to enable EE3-19. IMAD13 is set lo, so IMADA13 is lo and this signal sets EE4-12 lo. The output of EN4-11 (WN) is lo and on Figure 4.1F this signal enables FN6-6. The next HI clock pulse results in a W3 signal which, on Figure 4.1E, clocks EE4-11 so that EE4-9 (INSTN) is latched lo and EE4-8 (INST) is latched hi. At the end of the INST routine control branches to the software program (if running). The next software instruction is executed but when, on Figure 4.1E, FETCHN reverts hi at the end of the instruction, EE5-9 is clocked hi. When FETCHN is set lo at the beginning of the next instruction cycle, the output of EH5-10 goes hi and EC5-6 (FINSTN) is clocked lo. This signal generates an EPINT which switches the µP to Firmware Mode (the software instruction is not executed). When the interrupt is decoded control branches to the STBST routine at F/00CA. This instruction vectors control to address F/00B4 (VISUA0) which sets the RUN bit of the PSW to zero and the S bit to one and saves the new PSW at OP/HHP RAM address /FFFC ("SAVE"). The contents of the PC are placed in Register A7 and control branches to the EMIT routine, which sends the new value of the PC to the HHP on the SDMP line.

3.4.4 OTHER COMMANDS

The selection of any other HHP command results in an EPINT which is decoded and then control branches to the appropriate HHP routine. These routines are detailed in Figure 2.10B and the Firmware Assembly Listing. The IPL routine is described in section IPL PROGRAM and the Microdiagnostics are described in section MICRODIAGNOSTIC PROGRAM.

3.4.5 HHP ROUTINE

On Figure 4.1F the leading edge of an SDPM message is slugged by R5, C8 and inverted at FG5-8 (RDIN). On Figure 4.1E this signal generates an EPINT at H5-6 which interrupts the µP. The EPINT routine (starting at F/005A) includes an RER /0080 instruction which reads the Status Buffer to allow the µP to discover the source of the interrupt. When the source is the HHP, control branches to the HHP routine at F/00EC. This routine employs shift instructions, count loops, etc. to read in the rest of the SDPM message. After the message has been analised and data (if any) has been stored in F/FFFA ("DATHHP"), the function is decoded and control branches to the appropriate function routine.

3.4.6 LOCK INPUT

When the LOCK switch of the HHP is operated the HHP functions are inhibited and, on Figure 4.1F signal LOCK at Conn. J3-B1 is set hi. This signal is significant only during a power-on sequence and after a power failure. In these cases the state of the LOCK signal is read by the µP, via the Incode Data lines. Complete details are given in section POWER CONTROL.

3.4.7 VISRUN ROUTINE

This routine is used to set "run" on the HHP display, via the SDMP line, whenever the CP1A is set to the RUN mode. The "run" code is 41 so the form of the SDMP data is 0100000111 (the start bit is 0, the two stop bits are 1, and the l.s. bit of code 41 is transmitted first). The VISRUN routine starts at address F/03B2. Note that a CF instruction is used to save the PC and PSW on the Firmware stack (SP = Register A14) each time the WAIT routine is used to generate a bit delay (F/0170). An RTN instruction restores the PC and PSW.

3.4.8 EMIT ROUTINE

This routine is used to transmit data from the CP1A to the HHP on the SDMP line. The first instruction at F/0350 loads the stack pointer (Register A14) with address /FFF2 (the first of two locations that are used to store the PC and the PSW during a CF instruction). The next instruction (WER /001E) generates the leading edge of the start bit. On Figure 4.1E signal EN4-11 (WN) is set lo (IMAD09 is lo, WRITE A is hi, and IMAD08 is lo), whereby EE3-19 is enabled. Because IMAD15 is lo signal EE3-3 (IMADA15) is set lo. On Figure 4.1F signal WN enables FN6-6 and FE4-2 is lo, so the next HI pulse clocks FE4-3 lo and SDMP is set hi. The next four instructions generate the required period (208nS) of the start bit then the half-character and bit counters are loaded with their initial values. The data to be transmitted are in Register A7 (see Figure 2.10B) and they are now copied into Register A2. By successive shifts, delays and WER instructions the first half-character of data is sent to the HHP on the SDMP line followed by the data code half-character ("3"). The two stop bits are appended and control branches to F/0098 (Return Routine).

3.5 OP INTERFACE

3.5.1 POWER SWITCH

When the OP is connected to the CP1A, the OP power supply switch controls the CP1A power supplies as follows:

(a) Switch set at MEMORY OFF: No power supplies
(b) Switch set at MEMORY ON : +5VM and +12VM Software Memory supplies only
(c) Switch set at MASTER ON : +5VL, +12VL, -12VL, +5VM + -12VM supplies.

3.5.2 REMOTE SWITCH OPERATED

On Figure 4.1F the LOCK input at Conn. J4-A8 is set hi. During a power-on sequence and after a power failure, the state of this signal is measured to determine whether the CP1A will be set to the RUN state or to the IDLE state. More details are given in section POWER CONTROL (see also Figure 2.4).

3.5.3 RESTART SWITCH OPERATED

On Figure 4.1F the Automatic Restart Enable signal (ARE) at Conn. J4-A6 is set hi. After a power failure, and when RSLN goes hi while PWFN is still lo, an EPINT is generated. The EPINT routine detects that the EPINT was caused by an INITN signal (see Figure 2.10A) and branches to the INIT routine. This routine tests the state of the ARE singal by reading Incode Data (Figure 4.1F) with an RER/00F6 instruction. Provided the contents of the Software Memory were preserved "BAWON" = 1. When PWFN goes hi, the START routine checks that "BAWON" = 1 and control branches to the AUTORST routine. More details are given in section POWER CONTROL (see also Figure 2.4).

3.5.4 TIMER SWITCH OPERATED

On Figure 4.1F, signal RTCE at Conn. J4-B1 is hi. On Figure 4.1E the RTCN input at Conn. J1-B8 is inverted to RTC at EA5-9. On Figure 4.1A the Real Time Clock (RTC) is gated via AJ5-3 to AK3-26 (INT2N). Provided ENB = 1 and a higher-priority interrupt is not being serviced, the INT2N interrupt causes control to branch to Software Memory address /0004. This address contains the start address of the RTC interrupt handling routine. The composition of the routine depends upon the requirements of the system. In some systems the RTC is not used.

3.5.5 RUN SWITCH OPERATED

The RUN switch is biased, and when it is operated a negative-going pulse (RUNN) appears at Figure 4.1F Conn. J4-A2. On Figure 4.1E, the leading edge of the RUNN pulse clocks ED3-9 lo. The FIPLEXN signal causes an EPINT, which interrupts the µP at AK3-30. The µP switches to Firmware Mode and the EPINT routine decodes the source of the interrupt. Control then branches to F/00D2 (the RIPL routine). On Figure 4.1E the WER /000F instruction sets EN4-11 lo to enable EE3-19. The IMAD11 input of EE3-11 is lo so IMADA11 is lo, and this signal presets the interrupt latch at ED3-10 lo. Thus the interrupt is reset. Instruction F/00D4 causes control to branch to the AUTOIPL routine. On Figure 4.1F this routine reads the Incode Data with an RER /00F6 instruction. The data code is set by the OP thumbwheel switch, and before the RUN button is pushed the thumbwheel switch should be set for the required device parameters. The data code is converted to the IPL Program device parameter address, which is stored in OP/HHP address /FFF4 ("IPLSEL") and control branches to the IPL0 routine. This routine loads the IPL Program into the Software Memory. Full details are given in section POWER CONTROL and section IPL PROGRAM.

3.5.6 ON SWITCH OPERATED

When this biased switch is operated a running system is shut down, but the contents of the Software Memory are preserved. The system can be restarted at the point where it was stopped by first setting the OP power switch to MEMORY ON and then setting it back to MASTER ON. On Figure 4.1F a negative-going pulse appears at Conn. J4-A4, and the trailing edge of the pulse latches ED3-9 lo. The FIPLEXN signal causes an EPINT which is decoded so that control branches to F/00D2. A WER /000F instruction sets the SIRN output of the Mode ROMs lo (Figure 4.1A). On Figure 4.1F the SIRN signal at FJ5-5 presets FK6-6 hi (IR). On Figure 4.1E the inverted IR signal at EL0-18 is passed via the PONN/EX strap (strapped for PONN operation) to the level-4 input of Interrupt Handler EG4-1. The IH produces BCI code 000010011111111 (see Figure 2.5) and, provided no higher-priority code eliminates the level-4 code, the level-4 code is supplied to EK4-19 (clocked in by INCLK).

In EK4 the BCI code is compared to the current Program Level, and if the level-4 interrupt has a higher priority, the EXTIN output at EK4-7 is set lo. This signal is supplied to AK3-25 and, if ENB = 1 and the CP1A is in the RUN state, the µP is interrupted. It responds by producing an RER /00FF instruction which, on Figure 4.1A sets the CSINTN output of the Mode ROMs lo. On Figure 4.1E the CSINTN signal at EK4-13 triggers the IH, which places the level-4 code on the AD00 to AD05 lines. The code is fed to the µP on the A/D Bus. The µP then produces a WER /00FF instruction. This instruction sets CSINTN hi but also sets the µP WRITE output hi, so the level-4 code is written into the Program Level Register of EK4 and becomes the new Program Level. The PC of the µP is loaded with an address that contains the start address of the level-4 interrupt handling routine (in the case of a level-4 interrupt the PC is loaded with address /0008). The µP then loads the PC with the start address of the level-4 interrupt handling routine and control branches to that address. The composition of the level-4 interrupt handling routine will depend upon the requirements of the system, but it should always include an instruction which will reset the interrupt. This can be accomplished by programming an I/O instruction. The interrupt handling routine may also include a WER /F7 instruction that sets the CP1A power supply to the Maintain Mode by generating a SWOFAN pulse at AL4-4. From EC5-11 this pulse sets SWOFN lo. SWOFN is fed to the OP from Conn. J4-B3.

Note: The Maintain Mode is not programmable on 6U6 Power Supplies.

When the CP1A is in the IDLE state a level-4 interrupt is not accepted. In this case the CP1A hardware operates in association with the firmware to generate an independant SWOFN signal. On Figure 4.1E the IRN signal at EJ6-5 finds the FIRMN signal at EJ6-4 set lo. Thus signal PLOFN goes lo and an EPINT is generated. The EPINT routine decodes the source of the interrupt and control branches to F/00CC (see also Figure 2.10A). The µP produces an RER /00F7 instruction and, on Figure 4.1A, the SIRN output of the Mode ROMs is set lo. On Figure 4.1F signal SIRN presets FK6-5 hi and FK6-6 lo. The µP then produces a WER /00F7 instruction. On Figure 4.1A the SWOFN output of the Mode ROMs is set lo and on Figure 4.1E the output of EK5-3 is set lo (SWOFN). This signal sets the power supply to Maintain Mode.

3.5.7 THUMBWHEEL SWITCH

The 10-position switch is used to set Incode Data (including device parameter codes and the CP1A self-test code). The Incode Data is read into the µP by executing an RER /00F6 instruction.

3.5.3 RESTART SWITCH OPERATED

On Figure 4.1F the Automatic Restart Enable signal (ARE) at Conn. J4-A6 is set hi. After a power failure, and when RSLN goes hi while PWFN is still lo, an EPINT is generated. The EPINT routine detects that the EPINT was caused by an INITN signal (see Figure 2.10A) and branches to the INIT routine. This routine tests the state of the ARE singal by reading Incode Data (Figure 4.1F) with an RER/00F6 instruction. Provided the contents of the Software Memory were preserved "BAWON" = 1. When PWFN goes hi, the START routine checks that "BAWON" = 1 and control branches to the AUTORST routine. More details are given in section POWER CONTROL (see also Figure 2.4).

3.5.4 TIMER SWITCH OPERATED

On Figure 4.1F, signal RTCE at Conn. J4-B1 is hi. On Figure 4.1E the RTCN input at Conn. J1-B8 is inverted to RTC at EA5-9. On Figure 4.1A the Real Time Clock (RTC) is gated via AJ5-3 to AK3-26 (INT2N). Provided ENB = 1 and a higher-priority interrupt is not being serviced, the INT2N interrupt causes control to branch to Software Memory address /0004. This address contains the start address of the RTC interrupt handling routine. The composition of the routine depends upon the requirements of the system. In some systems the RTC is not used.

3.5.5 RUN SWITCH OPERATED

The RUN switch is biased, and when it is operated a negative-going pulse (RUNN) appears at Figure 4.1F Conn. J4-A2. On Figure 4.1E, the leading edge of the RUNN pulse clocks ED3-9 lo. The FIPLEXN signal causes an EPINT, which interrupts the µP at AK3-30. The µP switches to Firmware Mode and the EPINT routine decodes the source of the interrupt. Control then branches to F/00D2 (the RIPL routine). On Figure 4.1E the WER /000F instruction sets EN4-11 lo to enable EE3-19. The IMAD11 input of EE3-11 is lo so IMADA11 is lo, and this signal presets the interrupt latch at ED3-10 lo. Thus the interrupt is reset. Instruction F/00D4 causes control to branch to the AUTOIPL routine. On Figure 4.1F this routine reads the Incode Data with an RER /00F6 instruction. The data code is set by the OP thumbwheel switch, and before the RUN button is pushed the thumbwheel switch should be set for the required device parameters. The data code is converted to the IPL Program device parameter address, which is stored in OP/HHP address /FFF4 ("IPLSEL") and control branches to the IPL0 routine. This routine loads the IPL Program into the Software Memory. Full details are given in section POWER CONTROL and section IPL PROGRAM.

3.5.6 ON SWITCH OPERATED

When this biased switch is operated a running system is shut down, but the contents of the Software Memory are preserved. The system can be restarted at the point where it was stopped by first setting the OP power switch to MEMORY ON and then setting it back to MASTER ON. On Figure 4.1F a negative-going pulse appears at Conn. J4-A4, and the trailing edge of the pulse latches ED3-9 lo. The FIPLEXN signal causes an EPINT which is decoded so that control branches to F/00D2. A WER /000F instruction sets the SIRN output of the Mode ROMs lo (Figure 4.1A). On Figure 4.1F the SIRN signal at FJ5-5 presets FK6-6 hi (IR). On Figure 4.1E the inverted IR signal at EL0-18 is passed via the PONN/EX strap (strapped for PONN operation) to the level-4 input of Interrupt Handler EG4-1. The IH produces BCI code 0000100111111111 (see Figure 2.5) and, provided no higher-priority code eliminates the level-4 code, the level-4 code is supplied to EK4-19 (clocked in by INCLK).

In EK4 the BCI code is compared to the current Program Level, and if the level-4 interrupt has a higher priority, the EXTIN output at EK4-7 is set lo. This signal is supplied to AK3-25 and, if ENB = 1 and the CP1A is in the RUN state, the µP is interrupted. It responds by producing an RER /00FF instruction which, on Figure 4.1A sets the CSINTN output of the Mode ROMs lo. On Figure 4.1E the CSINTN signal at EK4-13 triggers the IH, which places the level-4 code on the AD00 to AD05 lines. The code is fed to the µP on the A/D Bus. The µP then produces a WER /00FF instruction. This instruction sets CSINTN hi but also sets the µP WRITE output hi, so the level-4 code is written into the Program Level Register of EK4 and becomes the new Program Level. The PC of the µP is loaded with an address that contains the start address of the level-4 interrupt handling routine (in the case of a level-4 interrupt the PC is loaded with address /0008). The µP then loads the PC with the start address of the level-4 interrupt handling routine and control branches to that address. The composition of the level-4 interrupt handling routine will depend upon the requirements of the system, but it should always include an instruction which will reset the interrupt. This can be accomplished by programming an I/O instruction. The interrupt handling routine may also include a WER /F7 instruction that sets the CP1A power supply to the Maintain Mode by generating a SWOFAN pulse at AL4-4. From EC5-11 this pulse sets SWOFN lo. SWOFN is fed to the OP from Conn. J4-B3.

Note: The Maintain Mode is not programmable on 6U6 Power Supplies.

When the CP1A is in the IDLE state a level-4 interrupt is not accepted. In this case the CP1A hardware operates in association with the firmware to generate an independant SWOFN signal. On Figure 4.1E the IRN signal at EJ6-5 finds the FIRMN signal at EJ6-4 set lo. Thus signal PLOFN goes lo and an EPINT is generated. The EPINT routine decodes the source of the interrupt and control branches to F/00CC (see also Figure 2.10A). The µP produces an RER /00F7 instruction and, on Figure 4.1A, the SIRN output of the Mode ROMs is set lo. On Figure 4.1F signal SIRN presets FK6-5 hi and FK6-6 lo. The µP then produces a WER /00F7 instruction. On Figure 4.1A the SWOFN output of the Mode ROMs is set lo and on Figure 4.1E the output of EK5-3 is set lo (SWOFN). This signal sets the power supply to Maintain Mode.

3.5.7 THUMBWHEEL SWITCH

The 10-position switch is used to set Incode Data (including device parameter codes and the CP1A self-test code). The Incode Data is read into the µP by executing an RER /00F6 instruction.

3.5.8 INDICATORS

The indicators are driven via the CP1A Outcode Data lines. On Figure 4.1F the outcode data are released onto the lines by executing a WER /00F6 instruction. A data strobe (SHEXN) is generated by setting output OUTN of the Mode ROMs (Figure 4.1A) lo and gating it with an HIN clock pulse.

3.6 CP1A RUN/IDLE STATE SWITCHING

When the CP1A is executing system/user programs it is set to the RUN state in Software Mode i.e. the RUN and S bits of the PSW are set to 1. If the program stops due to the execution of a Halt instruction the µP is switched to Idle mode, but the HHP continues to display "run". The discrepancy is rectified by detecting the Halt condition and updating the HHP display. On Figure 4.1E signal FIRMN at EC3-2 is hi. A stream of FETCHN pulses at EB5-2 have positive-going trailing edges which repeatedly retrigger monostable EB5 so that EB5-4 is held lo. Thus EC3-12 remains hi. (The maximum interval between FETCHN trailing edges is normally less than 80 µs.) If the program stops on a Halt instruction, EB5 is not retriggered and EB5-4 goes hi. The output of EC3-12 goes lo and an EPINT is generated. The EPINT routine decodes the source of the interrupt and control branches to the HALT routine at F/00AC. The PSW is loaded into Register A1 and the S bit is tested. If the S bit = 1, i.e. the µP is in Software Mode, the firmware program sequence continues with the VISUAO routine at F/00B4. This routine generates a new PSW in which RUN = 0 and S = 1 and stores it at OP/HHP RAM address /FFFC ("SAVE"). The contents of OP/HHP RAM address /FFDO ("STACK" i.e. the PC) are loaded into Register A7 and control branches to the EMIT routine. This routine writes the PC to the HHP display. At the end of the subsequent RETURN routine the contents of the registers are restored with the RUN bit of the PSW set to 0. Thus the CP1A is set to the IDLE state and waits for an HHP or OP command.

When the S bit test shows that S = 0, i.e. the µP is in Firmware Mode, the interrupt is meaningless and was probably caused by spurious noise - typically caused by disconnecting the HHP. In this case control branches to the RETURN routine (with the RUN bit of the PSW still set to 1) so that operations can continue.

Another condition that must be detected is that of an external bus operation that occupies the bus for more than 80 µs. When this occurs - typically because of a DMA operation between a FIOP unit and Software Memory - the bus is occupied for about 100 µs. During this period no FETCHN pulses are generated and an EPINT signal is generated which is not valid. To detect this condition, instruction F/00B2 also tests the RUN bit. When the RUN bit is 0 it means that the program was stopped by a Halt instruction, so the HHP display must be updated. When the RUN bit is 1 it means that the bus has been occupied for longer than 80 µs, so the HHP need not be updated and operations can continue.

3.7 STOP COMMAND

When the System Bus STOPN signal goes lo at Conn. J1-B10 (Figure 4.1E) the output of EL0-3 goes hi and clocks EE5-5 lo. The FSTOPN signal generates an EPINT. The EPINT routine decodes the source of the interrupt and control branches to F/00D6. This address contains an instruction which vectors to the VISUAO routine (described in section 3.6).

3.8 SOFTWARE MEMORY INTERFACE

3.8.1 READ ACCESS (FIGURE 3.3 AND 4.1)

The following description assumes that the one-instruction program shown in Figure 3.2A is loaded and running.
On Figure 4.1A, the ASTRO output of the µP is set hi. About 50nS later address /0000 is placed on the A/D Bus (AD00 to AD15) and about 50nS after that the AMA, WRITE and FETCHN outputs are set lo and the AMB output is set hi. On Figure 4.1B, the trailing edge of the ASTRON pulse clocks the address into the Address Latch.

When µP output REQN goes lo the Mode ROMs are enabled at Figure 4.1A, AM4-13. The output of AM4-10 goes lo, whereby the next H1 pulse clocks AM6-9 lo and AM6-8 hi. Because the WRITE input at AJ6-10 is lo, the output of AJ6-8 (ENRN) goes lo. On Figure 4.1B this signal enables the Data Latch receiver outputs, but at this time there is no significant data on the BION lines. On Figure 4.1A, the hi output of AM6-8 clocks AM6-3, so AM6-5 (BRQSI) goes hi. The Bus Request Strobe Input (BRQSI) latches the states of BRQA (AB2-3) and BRQB (AB2-2) into the BM to select the type of System Bus access. On Figure 4.1E, EE3-1 is lo, so EE3-2 is enabled. Because AMA at EE3-2 is lo, EE3-18 (BRQA) is lo. On Figure 4.1A, AB2-3 is lo. AMB is hi so AB2-2 is hi. Provided that BM signals BUSRN, MSN and BSYN are all hi (i.e. no other master unit has the use of the System Bus, nor is requesting use of the System Bus) the BM is set up to access the Software Memory in read mode.

The BM sets RDY (AB2-26) lo and the µP samples this signal at AK3-34 until it goes hi. On Figure 4.1B, RDY is fed to the Data Latch, which is set to receive data when data is available from the Software Memory. On Figure 4.1A, the BM sets outputs EMADN and WRITE lo. EMADN resets BRQSI lo (via AJ5-11) and sets µP input DMARQN lo. In the example we are considering, the µP sets DMANSN lo after the bus cycle. On Figure 4.1E, DMANSN inhibits EE3-1 so that BRQA is 3-stated (Note: BM chips of some master units use a second BRQA sample to set the type of bus access termination.) On Figure 4.1B, EMADN gates address /0000 through the Address Buffer to the System Bus MAD lines.

On Figure 4.1C, the MAD00 bit is fed to CM5-12 and the MAD15 bit to CM5-13. On Figure 4.1E, the CHAR output of EA5-16 is held lo by pull-up resistor R7 and the inverter, and on Figure 4.1C, input CM5-4 is held lo, i.e. the CP1A can access the Software Memory in word mode only. MAD01 to 14 bits are supplied to the input of Row/Column Address Selector A1/B1. On Figure 4.1B, EMADN enables BE1 so that MADE0 to MADE7 bits are set lo, and the output of BF3-8 (ENEM) is set lo. If any of MADE0 to 7 bits is set hi (by an external unit or a fault) ENEM goes hi. On Figure 4.1C, the output of CN6-1 goes lo, whereby the output of CQ6-12 goes lo to inhibit the operation of the Stack RAM Control Logic. Thus the CP1A is restricted to an addressing range of 32K words. On Figure 4.1E, EMADN sets EL0-16 hi. However, because EL5-9 is hi at this time, nothing further happens. On Figure 4.1C, the WRITE signal from AB2-20 is supplied, via the System Bus, to CM5-5. At CA1/B1-1 (STAD) is lo so bits MAD01 to MAD07 (Row Address) are passed, via CA1/B1, to Refresh/Access Selector CR5/S5. Assuming that a refresh cycle is not in progress, FREF at CR5/S5-1 is lo and the Row Address is passed, via the Refresh/Access Selector, to the Stack RAM.

On Figure 4.1A, TMRN at AB2-7 is set lo, and on Figure 4.1C, TMRN is inverted at CL0-5 and sets CR6-12 hi. The next HON pulse at CR6-11 clocks CR6-9 (FTMR) hi and CR6-8 lo. At CM5-9 signal FTMR clocks the RAM function bits into the RAM Function Latch. At CP6, FTMR removes the clear input from the flip-flops. The output of CR6-8 sets CQ5-8 hi and removes the clear input from shift register CW6. FTMR is also fed to CR6-2, where the next HO pulse clocks CR6-5 (CYCLE) hi and CR6-6 lo. CYCLE is fed to CN3-10 and 5 to enable the gates, but N3-11 and 3 are lo at this time so the gate outputs do not change state. The lo output of CR6-6 holds CV6-2 lo so that a refresh cycle cannot start until the access cycle has finished. The lo output of CV6-15 holds CQ5-6 hi, and the lo output of CV6-14 holds CN6-2 lo. Because CN6-3 is lo, CN6-1 is hi, thus all three inputs at CQ6-1,2 and 13 are hi and CQ6-12 is hi. Thus CR6 is not cleared. The output of CR6-6 also sets CW6-10 lo, whereby the next HON pulse at CQ6-11 loads bit combination 1000 into CW6.

The RAS output at CW6-15 is set hi. At CP5-10 and 4, RAS is gated with FREF and the MAD00 bit. Because MAD00 is lo, CM5-11 is hi, whereby CN5-6 is hi and RASON is set lo. On Figure 4.1D, RASON latches the Row Address bits into the chips that comprise the l.s. half of the Stack RAM. On Figure 4.1C, the next HON pulse at CW6-11 shifts the one in the register one place rightward, and also places a one in the l.s. position of the register. STAD is set lo and this signal at CA1/B1-1 sets CA1 and CB1 to pass MAD08 to MAD14 bits (Column Address) to the Refresh/Access Selector. Because a refresh cycle is not in progress, the Column Address is fed, via CR5/CS5, to the address inputs of the Stack RAM. The next HON pulse shifts the two ones in the register one place rightward and loads a one into the l.s. position. Thus CAS at CW6-13 is set hi and it is gated with the outputs of CM5-14, 3 and 15. Because only word operation is possible, CM5-3 is hi and, regardless of the value of the MAD15 bit, the outputs of CN5-11 and CN5-3 are hi. Outputs CP5-3 and CP5-1 are lo and, on Figure 4.1D, the CASLN and CASRN signals latch the Column Address bits into the l.s. half of the Stack RAM. On Figure 4.1C, WRITE at CM5-5 is lo, therefore CM5-7 is lo and CM5-6 is hi. The outputs of CQ5-3 and CQ5-11 are hi and, on Figure 4.1D, FWLN and FWRN are set hi for a read word operation.

During the CAS period, Stack RAM address /0000 is read and the contents of address /0000 (/0F00) are placed at the inputs of data Tx/Rxs DL1/DM1. On Figure 4.1C, the next HON pulse sets CW6-12 hi. The next HON pulse clocks CP6-11 so that CP6-8 is set lo. Because CM5-3 is hi, CN3-9 is hi. CYCLE at CN3-10 is hi, so BEMSCN and BELSCN are both set lo. WRITE is lo so the output of CM5-6 (FWN) is hi. On Figure 4.1D, FWN sets DL1/DM1 to transmit data. The inputs at DL1-9 and DM1-9 (BEMSCN and BELSCN) allow the read data to pass to the BION lines. (Note that the data is inverted.) On Figure 4.1C, the next HON pulse at CP6-3 clocks CP6-5 hi. In the case of a UPL Bus System, this output is gated with TMR at CL6-4 to set TSMN lo. In the case of a GPBS System, the earlier output of CP6-9 is gated with TMR to set TSMN lo.

On Figure 4.1A, signal TSMN at AB2-6 (from the Time-Out circuit if there is no reply to a TMRN signal, within a nominal 6.4µS) is accepted by the BM, which then sets RDY at AB2-26 hi. In the µP, RDY prepares the µP to receive data. On Figure 4.1B, the input at BG1/H1/J1/K1-11 (ENRN) is lo, the Data Latch data is available on the A/D Bus, but it is not yet latched by the µP. Note that the inversion of data through the Data Latch sets true data on the A/D Bus. When RDY goes hi, this condition is detected by the next +ve-going edge of the H1 clock to the µP. The next -ve-going edge of H1 latches the A/D Bus data into the µP. The -vegoing edge of H1 also resets REQN lo. On Figure 4.1A, the next +ve-going edge of H1 at AM6-11 clocks CM6-9 hi and ENRN at CJ6-9 is reset hi. In the next clock period the µP outputs AMA, AMB, WRITE and FETCHN are reset. After a delay (RDYDLY), TMRN of the BM is reset hi. On Figure 4.1C, the next HON pulse at CR6-11 resets CR6-9 lo and CR6-8 hi. The hi output of CR6-8 is gated with the hi input of CQ5-9 so that CQ5-8 goes lo.

This signal holds shift register CW6 cleared. The next HO clock pulse resets CR6-5 (FTMR) lo and CR6-6 hi. When FTMR goes lo, it resets CP6 at CP6-13 and 1. On Figure 4.1B, RDY going hi blocks the Data Latch.

Figure 3.2B shows another simple program loop. This program accesses the Software Memory twice: firstly to fetch the instruction, and secondly to fetch the long constant. During the first access MAD bits 00 to 13 are set hi, and during the second MAD bits 00 to 14. In both cases the m.s. half of the memory is used.

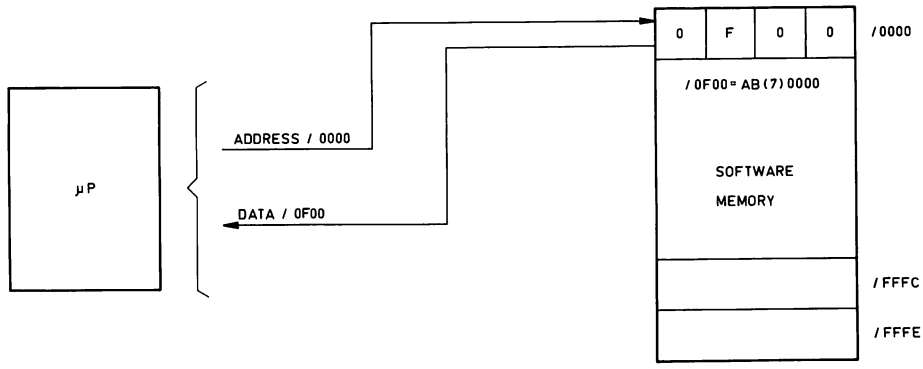


Figure 3.2A BRANCH TO ADDRESS /0000: INSTRUCTION /0F00 LOCATED IN MEMORY ADDRESS /0000

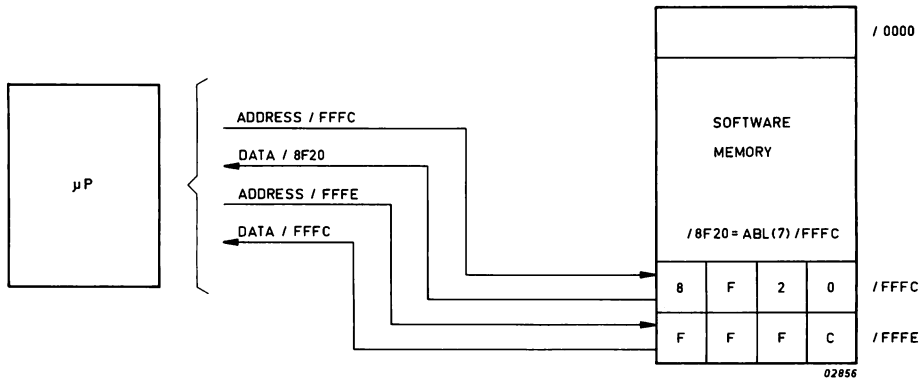


Figure 3.2B BRANCH TO ADDRESS /FFFC: INSTRUCTION /8F20 LOCATED IN MEMORY ADDRESS /FFFC

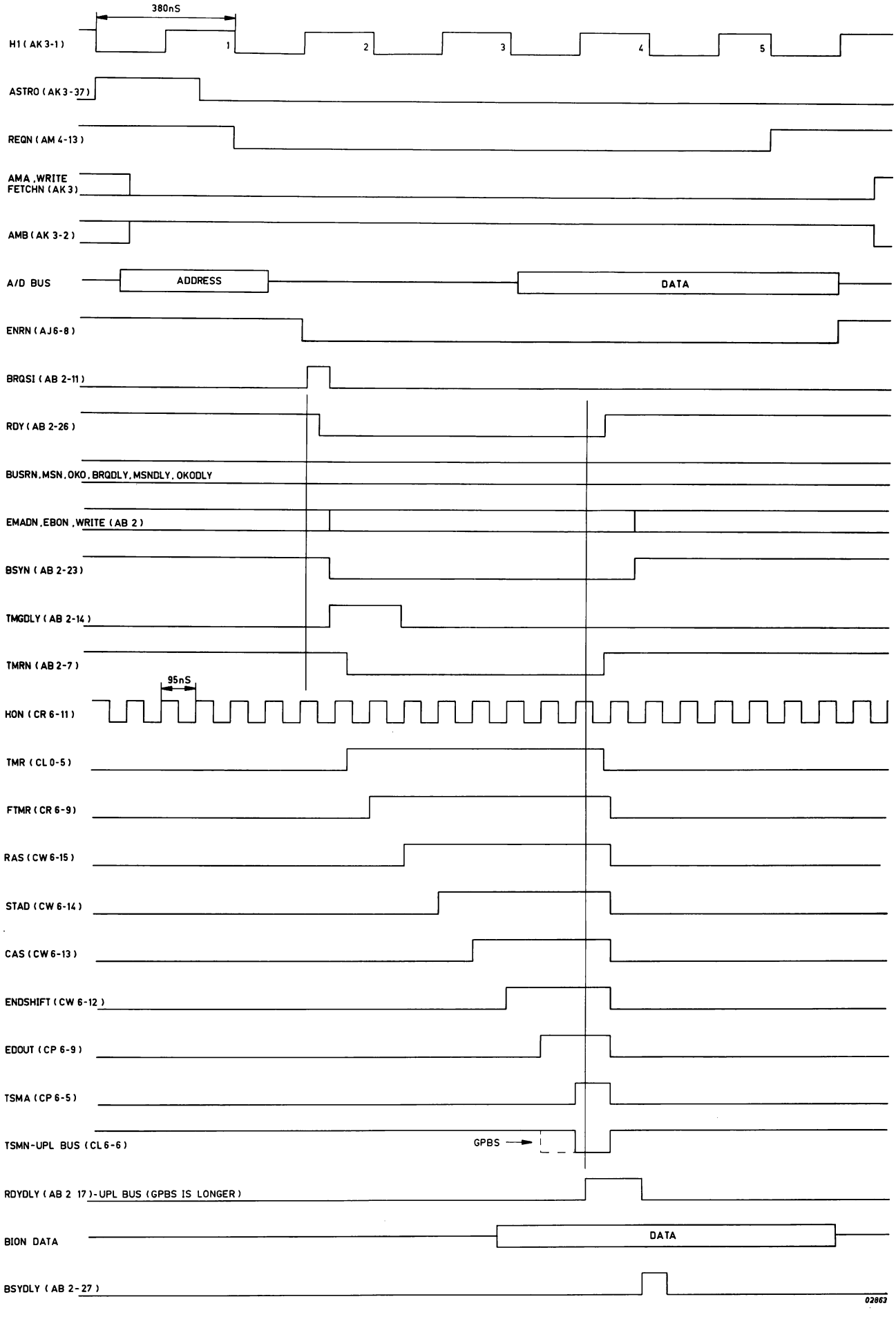


Figure 3.3 SOFTWARE MEMORY READ ACCESS

3.8.2 WRITE ACCESS (FIGURE 3.4 AND 4.1)

A write access is similar to a read access except that the WRITE output of the µP is set hi instead of lo. The µP places the data that is to be written on the A/D Bus. When BRQSI is set hi the DRCP input of the Data Latch (Figure 4.1B, BG1/H1/J1/K1-19) goes hi to latch the data. When the BM sets its WRITE output hi it also sets its EBON output lo. On Figure 4.1B, the BEN input of BG1/H1/J1/K1-9 enables the data onto the BION lines. The data is written into the Software Memory during the CAS period.

3.8.3 REFRESH CYCLE (FIGURE 3.5 AND 4.1C)

The Stack RAM is periodically refreshed in groups of 128 addresses by a Refresh Address Counter and the RAM Access Timing logic. The Refresh Address Counter consists of cascaded counters CT6/U6 and S6 which generate successive address inputs for the Stack RAM. The output of CS6 is supplied to the Refresh/Access Selector CR5/S5.

When a memory access is not in progress, the output of CR6-6 is reset hi and the shift right input of shift register CV6-2 is enabled. When the output of CU6-12 is set hi the CLEAR input of CV6-1 is set hi to remove the inhibit from the shift register. Initially, inputs CV6-9 and 10 are set at one and zero, so the next HON pulse at CV6-11 clocks a one into the l.s. position of the register. Thus CV6-15 (FREF) is set hi. This signal is supplied to the Refresh/Access Selector and sets the selector to pass the Refresh Row Address to the address inputs of the Stack RAM. The FREF signal also sets CQ5-6 lo, whereby CQ6-12 is set lo and flip-flops R6 are inhibited. Thus, once a refresh cycle has started, a read or write access cannot start until the refresh cycle is completed. The output of CV6-15 also sets CQ5-6 lo, whereby CQ5-8 is set hi and shift register CW6 is enabled.

The next HON pulse at CV6-11 shifts the one in the l.s. position of the register into the second l.s. position. When CV6-14 goes hi it sets the input of CW6-3 hi.

The next HON pulse at CW6-11 clocks a one into the l.s. position of the register and RAS at CW6-15 is set hi. The same HON pulse at CV6-11 shifts the contents of CV6 one place rightward and also shifts a one into the l.s. position.

The next HON pulse at CV6-11 shifts the contents of the register one place rightward and a one into the l.s. position. Thus the output of CV6-12 is set hi and this signal alters the operating conditions of the register by setting CV6-10 hi. The next HON pulse at CV6-11 loads te parallel inputs at CV6-3,4,5 and 6 into the register. (Bit combination 1101.)

The next HON pulse at CV6-11 finds CV6-13 lo so a zero is loaded into the l.s. position, and the register then contains bit combination 0101. Signal FREF is set lo, which resets CQ5-6 hi. The output CQ5-8 is set lo and clears register CW6 to reset RAS lo.

The RAS pulse is gated with FREF so that CP5-8 (RASON) and CP5-6 (RASIN) are both set lo. On Figure 4.1B, 128 column addresses are refreshed during the RAS-only period. Before the next group of 128 column addresses are refreshed the Refresh Address (Row Address) output of CS6-3 is incremented.

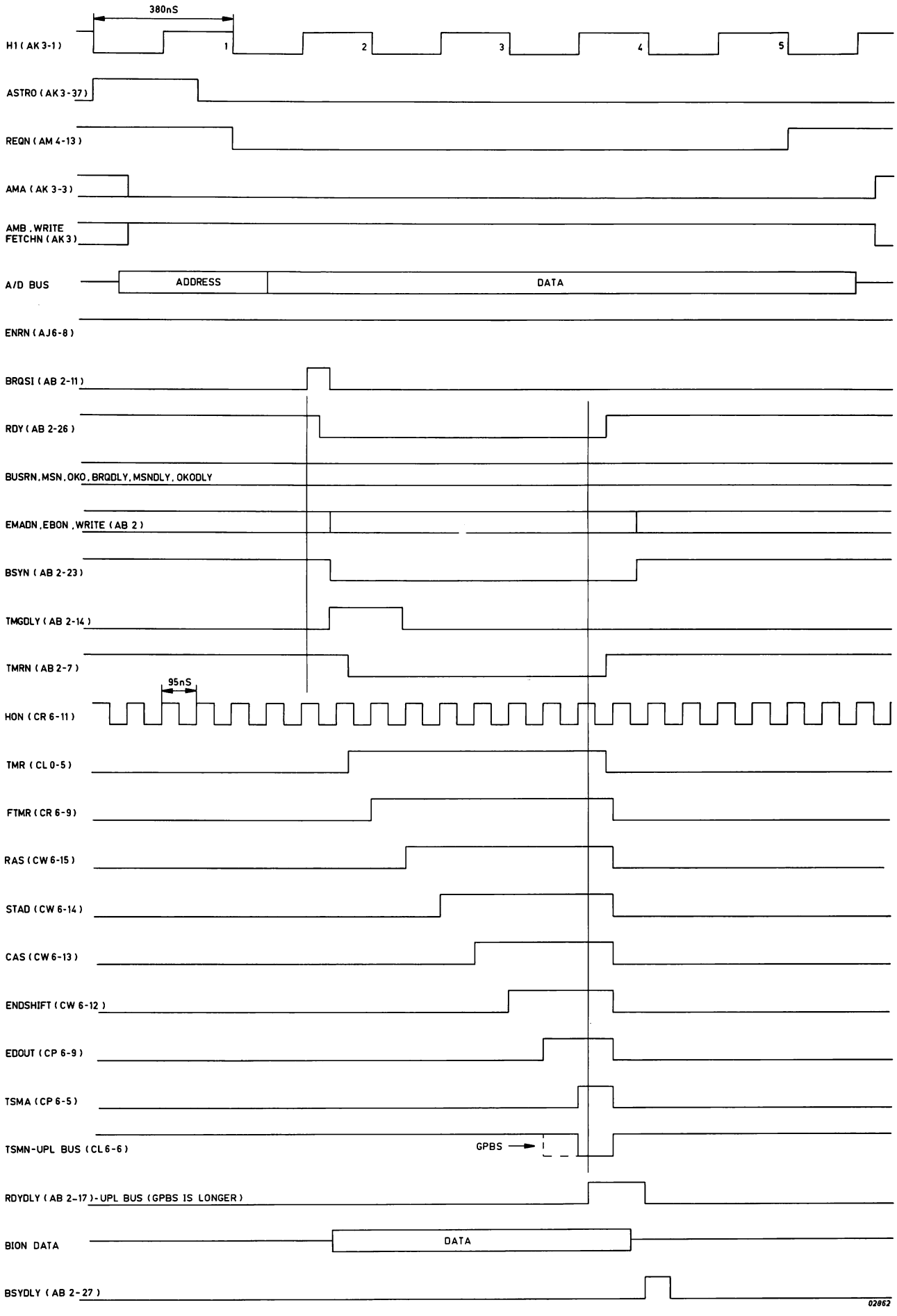


Figure 3.4 SOFTWARE MEMORY WRITE ACCESS

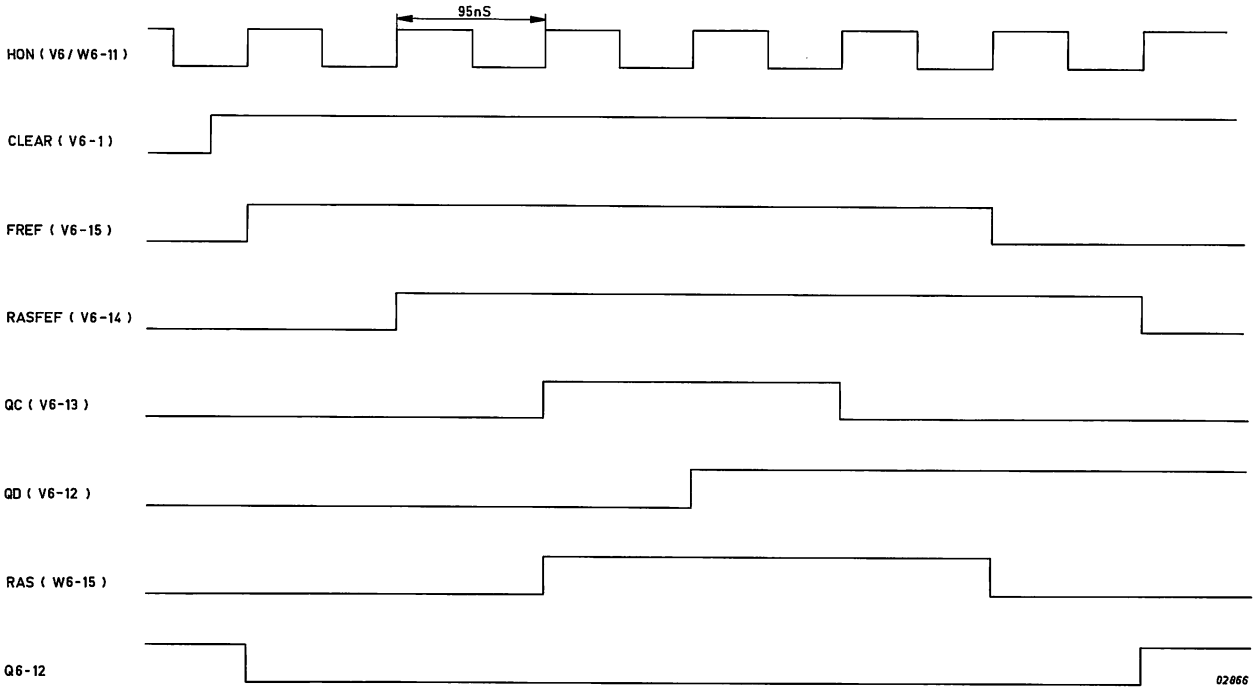


Figure 3.5 REFRESH CYCLE

3.8.4 -5VM POWER SUPPLY

The output of CU6-11 is supplied, via current-limiting resistor R2, to the base of Q1. When Q1 is switched off, C12 charges toward +12VM via R1 and D1. When Q1 is switched on, the potential at the junction of R1 and C12 is about 0V. The negative voltage at the junction of C12 and D2 is passed, via D2, to C13 and the capacitor charges up towards the maximum value of the negative voltage. Zener diode D3 clamps the voltage at the terminal of D3 to -5.1V. On Figure 4.1D, this voltage (-5VM) is supplied to pin 1 of every memory chip.

3.9 SYSTEM INTERFACE

The CP1A card communicates with the rest of the system across the System Bus, and in one of the following modes:

(a) Programmed Channel (Inhibit Mode)
(b) Programmed Channel (Interrupt Mode)
(c) Multiplexed Channel (Input-Output Processor Mode)
(d) Direct Memory Access Channel (DMA Mode).

Mode (a) is seldom used, but mode (b) is often used to program the control units of slow peripherals such as Paper Tape Readers and Paper Tape Punches. Mode (c) is used to program the control units of medium-fast and fast peripherals such as disk drives. Mode (d) is used to program the control units of very fast peripherals such as high-volume disk drives that incorporate data buffers.
In the following description of the System Interface it is assumed that the program shown in Table 3.2 is running. The hardware configuration is assumed to be as is shown in Figure 3.10, and a flowchart for the program is shown in Figure 3.11. Note that CP1A operations that are described in detail elsewhere in the manual are alluded to in outline only in this section.

3.9.1 LOADING AND RUNNING THE PROGRAM

The HHP is normally used to hand-load simple, stand alone programs. The PC (Register A0) is loaded with the start address (/1000) and the MCL (Master Clear) button is used to reset the system before the RUN button is pushed.

3.9.2 INITIAL OPERATIONS

The first three instructions of the program load the interrupt address vector (/1036) into the level 6 interrupt address (/000C), and load the Stack Pointer (Register A15) with the first address of the stack.

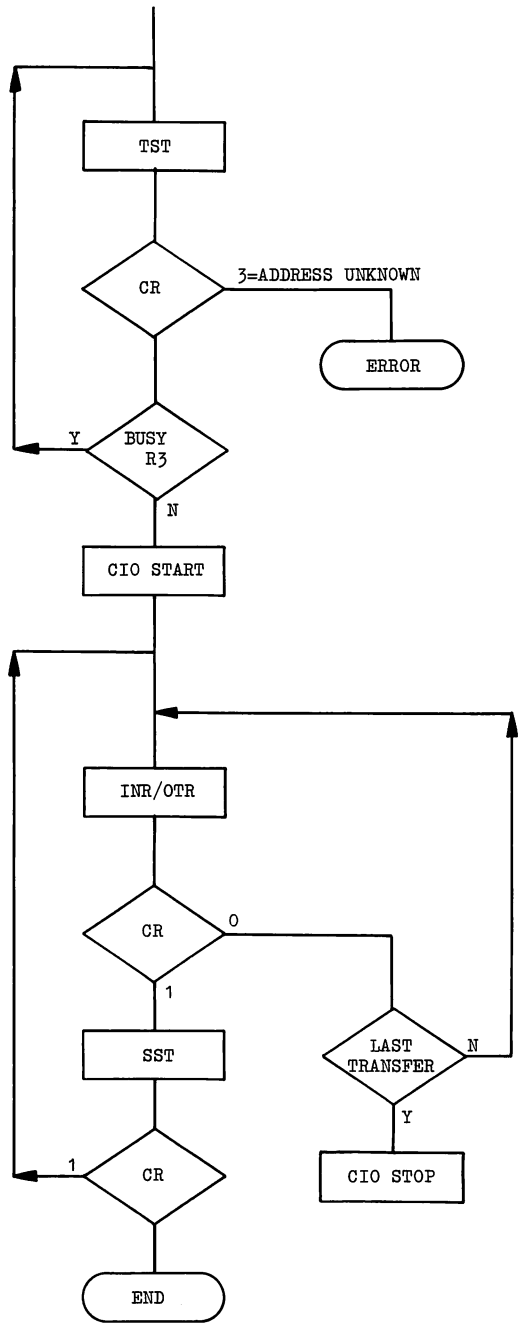


Figure 3.6 PROGRAMMED CHANNEL (INHIBIT MODE)

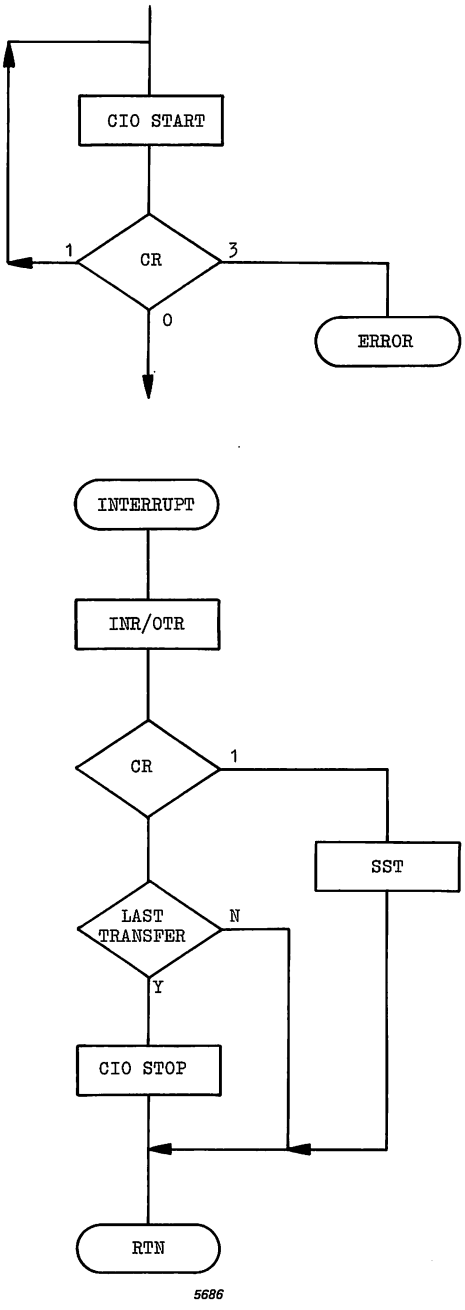


Figure 3.7 PROGRAMMED CHANNEL (INTERRUPT MODE)

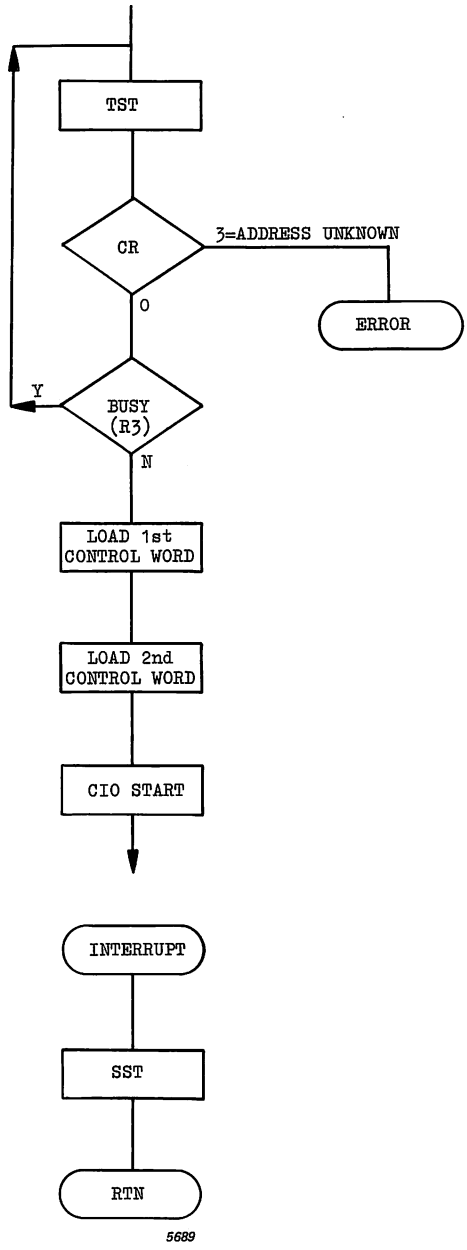


Figure 3.8 MULTIPLEXED CHANNEL (INPUT-OUTPUT PROCESSOR MODE)

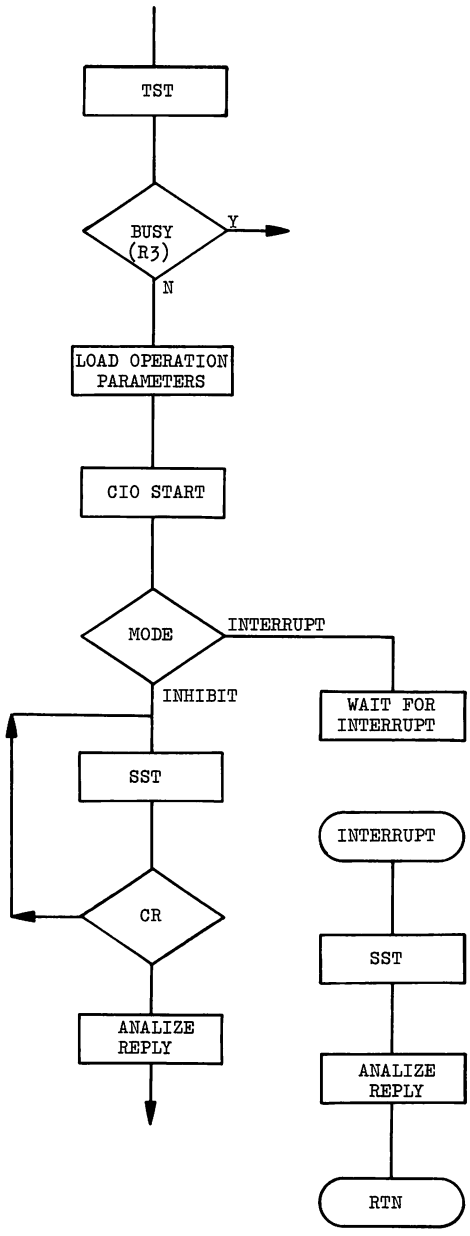


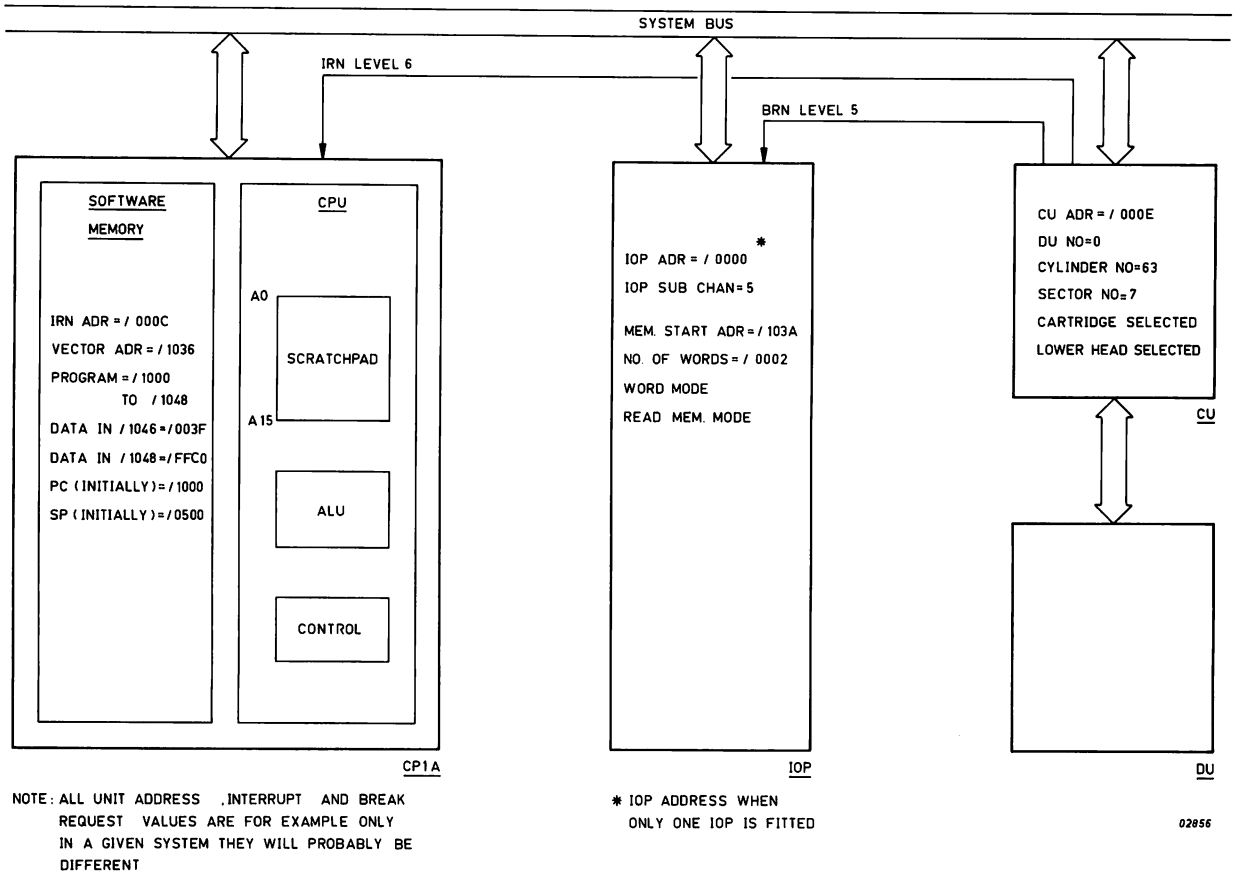
Figure 3.9 DIRECT MEMORY ACCESS CHANNEL (DMA MODE)

3.9.3 SEEK COMMAND (FIGURE 3.12)

The instruction at /100A loads cylinder number 63 into Register A2. The next instruction works as follows. On Figure 4.1A, the μP sets its ASTRO output hi. About 95μS later it sets AMA and WRITE hi and AMB and FETCHN lo. It also sets address /002E on the A/D Bus. On Figure 4.1B, the trailing edge of the ASTRON pulse at BC2/D2-11 clocks address /002E into the Address Latch.

Memory Address	Address Contents	Assembly Mnemonic			Additional Comments
1000	8120	LDKL	A1	/1036	Load interrupt vector
1002	1036				
1004	8141	ST	A1	/0C	Store interrupt vector
1006	87A0	LDKL	A15	/500	Load stack pointer
1008	0500				
100A	8220	LDKL	A2	/1FA	Load cylinder number
100C	01FA				
100E	42CE	CIO	A2,1,	/2E	Seek command to C.U.
1020	5F02	RB(7)	*		Wait for interrupt from C.U.
1022	8320	LDKL	A3	/0002	Load 1st IOP word
1024	C002				
1026	730A	WER	A3	/0A	Send 1st IOP word
1028	8420	LDKL	A4	/1046	Load 2nd IOP word
102A	1046				
102C	740B	WER	A4	/0B	Send 2nd IOP word
102E	055D	LDK	A5	/5D	Load write parameters
1030	45CE	CIO	A5,1,	/2E	Write Command to C.U.
1032	5F02	RB(7)	*		Wait for interrupt from C.U.
1034	5F26	RB(7)	*	-38	Branch to start of program
1036	4ECE	SST	A6	/0E	Reset C.U. to Inactive State
1038	9E20	ADLK	A15	4	Set SP to saved PC address
103A	0004				
103C	903E	IMR	A15		Increment saved PC
103E	903E	IMR	A15		Increment saved PC
1040	9F30	SUKL	A15	4	Set SP to next stack address
1042	0004				
1044	F03E	RTN	A15		Return
1046	003F				Cylinder number 63
1048	FFC0				Complement of cylinder no. 63

Table 3.2 SEEK AND WRITE PROGRAM



NOTE: ALL UNIT ADDRESS ,INTERRUPT AND BREAK REQUEST VALUES ARE FOR EXAMPLE ONLY IN A GIVEN SYSTEM THEY WILL PROBABLY BE DIFFERENT

* IOP ADDRESS WHEN ONLY ONE IOP IS FITTED

Figure 3.10 EXAMPLE OF PART OF A SYSTEM CONFIGURATION

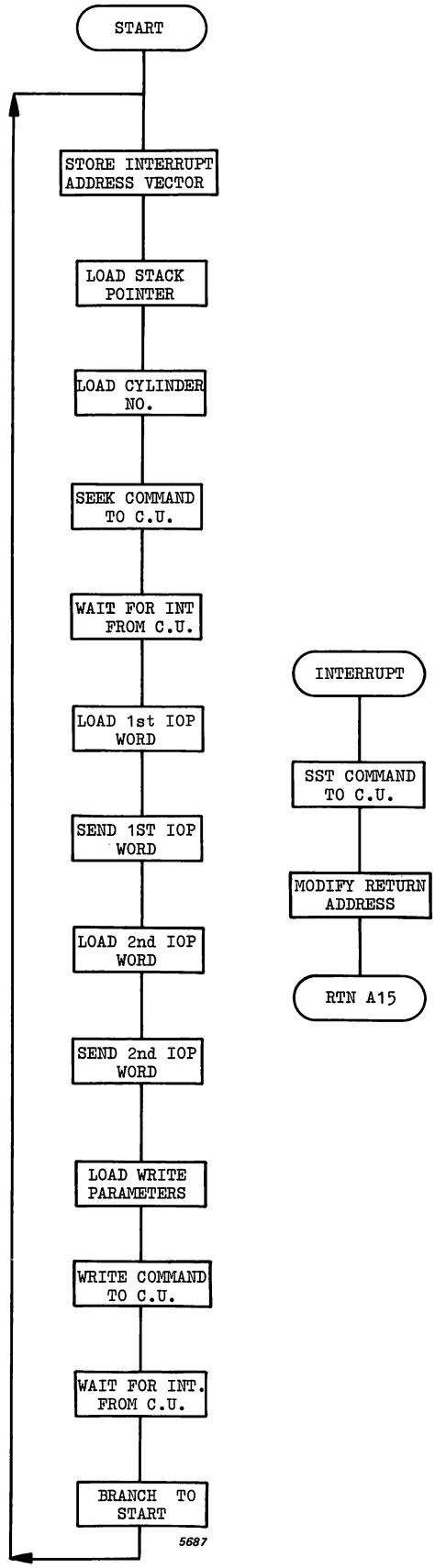


Figure 3.11 SEEK AND WRITE FLOWCHART

On Figure 4.1E, the input at EE3-1 is lo, so the hi input at EE3-2 drives EE3-18 (BRQA) hi. On Figure 4.1A, the input at AB2-3 (BRQA) is hi, the input at AB2-2 (BRQB) is lo, and the input at AB2-12 (WRC) is hi. About one clock period after the µP sets its ASTRO output hi, it sets its REQN output lo. The REQN signal removes address /002E from the A/D Bus, and replaces it with the data /01FA (cylinder no. 63). The REQN signal also sets output AM4-10 of the Mode ROMs lo. The next H1 pulse at AM6-11 clocks AM6-9 lo, but the output of AJ6-8 (ENRN) remains hi because the input at AJ6-10 is hi. The output at AM6-8 is clocked hi, and this signal clocks the output at AM6-5 hi. Signal BRQSI latches AMA, AMB and WRC into the BM, which is, therefore, set up to access the System Bus in TMPN mode. On Figure 4.1B, signal BRQSI at BG1/H1/J1/K1-19 latches the A/D Bus data into the Data Latch.

Provided that signals BUSRN, MSN and BSYN are all hi (i.e. no other master unit has requested or is using the System Bus), the BM allocates the System Bus to the CP1A and sets the RDY output of the BM lo. At AK3-34, the µP samples this signal and does nothing more until it is reset hi. A short time later the BM sets its EMADN and EBON outputs lo, and its WRITE output hi. On Figure 4.1A, the input at AJ5-13 sets AJ5-11 lo and signal BRQSI is reset lo. On Figure 4.1B, the input at BC1/D1-1 gates address /002E onto the System MAD lines. On Figure 4.1E, the input at EA5-2 gates power control inputs and the Real Time Clock into the CP1A. This action is significant only if there is a Power Failure or Real Time Clock interrupt, and here it is assumed that no such interrupt occurs. On Figure 4.1A, the EMADN input at AK3-33 (DMARQN) causes the µP to set DMANSN lo after the current bus cycle. On Figure 4.1E, the DMANSN input at EH5-9 drives EH5-8 hi so that the output at EE3-18 (BRQA) is 3-stated.

The input at EL0-4 sets EL0-16 hi, but ENRAZN at EL5-9 is hi, so the monostable is not triggered.

When the EBON output of the BM is set lo, this signal at BG1/H1/J1/K1-9 enables the cylinder no. onto the System Bus BION lines.
The BM also sets its BSY output lo to signify that the System Bus has been allocated and is not available to other units. The BM OKO output remains lo.
After an interval (TMGDLY), the BM sets its TMPN output lo. In the C.U. this signal: enables the C.U. Address Decoder; clocks in the function bits; clocks the BION data into the BION buffer. About 190nS (UPL Bus) or 115nS (GPBS) later the C.U. generates an ACN signal, and this signal is supplied to CP1A Conn. J1-A8 (Figure 4.1A).

About 300nS (UPL Bus) or 225nS (GPBS) after TMPN goes lo, and provided that the C.U. has decoded the address that is set on the MAD lines, the TSMN output of the C.U. is set lo. This signal is supplied to Conn. J1-A10 (Figure 4.1A), and it informs the BM that the data transfer has been effected. If this signal is not received within a nominal period of 6.4µS, the output at AL5-4 is set lo. The AREN input of the µP at AK3-24 causes the µP to set the contents of the Condition Register to 11, i.e. the address unknown condition.

After an interval (RDYDLY), the RDY output of the BM is reset hi. At AK6-11 this signal clocks AK6-8 hi, and at AK3-23 (CACK) the signal causes the µP to set the contents of the Condition Register to 00, i.e. the I/O Command was accepted condition. If an ACN signal has not been received when the RDY signal is reset hi, the contents of the Condition Register are set to 01, i.e. the I/O Command was refused condition.

Soon after RDY is reset hi, signal TMPN is reset hi, and then signal TSMN is reset hi. The trailing edge of the TSMN pulse is used to reset signals EMADN and EBON hi and to reset signal WRITE lo. It is also used to reset BSYN hi. Thus the System Bus is freed and is ready to be used again.

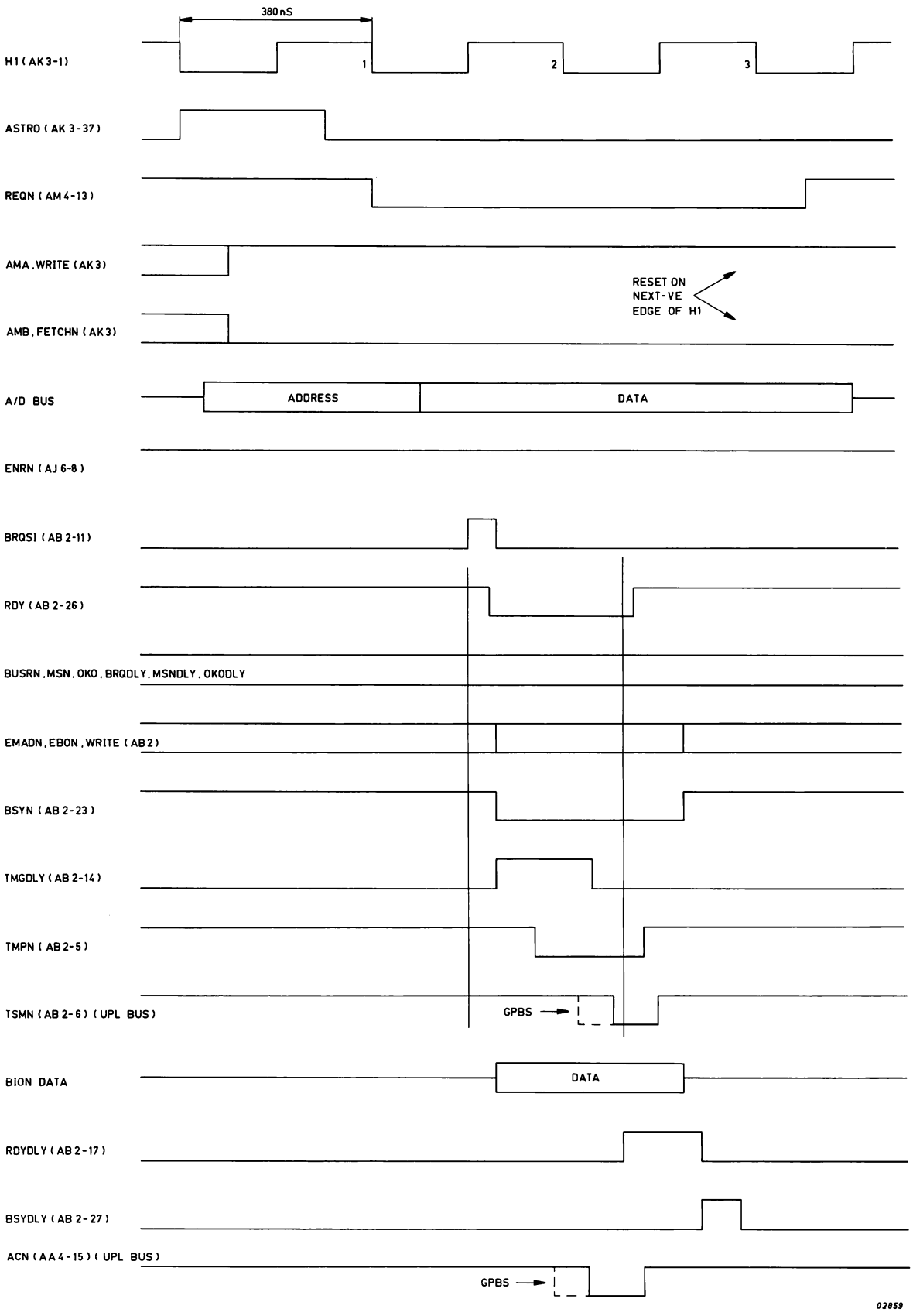


Figure 3.12 C.U. ACCESS

3.9.4 SUMMARY OF SEEK OPERATION IN C.U.

The Seek command switches the C.U. from its Inactive State to its Execute State. The C.U. Processor selects Disk Unit 0 and sends the cylinder no. to the D.U. It then initiates a seek to the required cylinder, and switches the C.U. to its Inactive Seek State (in which it can accept a second command on the other D.U. if a second D.U. is fitted).

When the seek is finished, the C.U. Processor switches the C.U. to the Wait State, where it generates an interrupt (INR) that is supplied to the CP1A at Conn. J1-B24 (Figure 4.1E). Note that this interrupt input (Level 6) was chosen for this example, but that a different level may be used in a specified system.

3.9.5 CP1A INTERRUPT ROUTINE

BCI code generation:
On Figure 4.1E, the lo input at EG4-21 triggers EG4 so that it generates BCI code 000011011111111 (see Figure 2.5). This code is clocked into EK4 by INCL clock (380nS). Provided that the Level 6 BCI code was not eliminated by a code of higher priority, it is compared with the contents of the Priority Level Register (PLR) in EK4. In our example the contents of the PLR are 63 at this time, so the incoming BCI code has higher priority, and EK4 sets EK4-7 (EXTIN) hi. On Figure 4.1A, this signal interrupts the µP at EK3-25.

CP1A interrupt:
When the µP has completed the current instruction (and provided that the ENB bit is set to logical 1), it executes an RER /FF instruction. Output AL4-5 (CSINTN) is set lo, and on Figure 4.1E, the input at EK4-13 is set lo. The IH places the Level 6 code on the AD00 to AD05 lines, and the code is acquired by the µP. The µP then executes a WER /FF instruction, which again sets CSINTN lo and also sets the WRITE input at EK4-10 hi. This time, the Level 6 code on the AD00 to AD05 lines is copied into the PLR to provide the program level. The RDY output of AK4-12 goes lo about 15nS after CSINTN goes lo and it is reset hi when the IH has finished operating.

Saving the PC and PSW:
The µP then accesses the Software Memory and writes the value of the PC (contents of Register A0) into location /0500 (the first location of the stack), and also decrements the SP (contents of Register A15) by 2. It again accesses the Software Memory and writes the PSW into Software Memory address /0500 - /0002, and again decrements the SP. The µP then loads the PC with address /000C. When the µP accesses this Software Memory address, the contents of the address (/1036) are placed in the PC and control branches to the specified address.

Interrupt routine:
In our example the interrupt routine consists of an SST Command that must be performed in order to reset the C.U. to its Inactive State, and also to cause it to send the C.U. Status Word to the specified CP1A register. The instruction results in a sequence of operations that are identical in form to the operations that were described in section 3.9.3. The following instructions increment the saved value of the PC by 2 so that control returns to a new value of PC after the interrupt. A return results in the µP executing a WER /FF instruction which restores the old value of program level to the PLR in the IH. (In our example this value is 63.)

3.9.6 INITIALIZING THE IOP

The instruction in address /1022 loads the number of words that are to be transferred from Software Memory to the Disk Unit into Register A3. The next instruction, at address /1026, transfers this data to the IOP. The sequence of operations required to effect the transfer is very similar to the operations described in section 3.9.3. In this case, however, the BM is set-up to access the System Bus in TMEN mode. Also note that the interval between TMEN going lo and TSMN from the IOP going lo is about 360nS. Also note that the IOP does not generate an ACN signal and that the Condition Register remains unchanged by the execution of a WER instruction. The next pair of instructions load the Software Memory start address into Register A4 and transfer the address to the IOP using a WER instruction.

3.9.7 WRITE COMMAND

The instruction in address /102E loads the write parameters (head and sector nos.) into Register A5, and the parameters are transferred to the C.U. using a CIO instruction. This operation is identical in form to the operation that is described in section 3.9.3.

3.9.8 SUMMARY OF C.U. AND IOP OPERATIONS

When the Write Command is decoded by the C.U., the C.U. switches from the Inactive State to the Execute State. The C.U. Processor then switches it to the Exchange State, where it generates a Break Request Not signal (BRN).
The BRN signal is supplied to the IOP, where, if the IOP sub-channel is available, the IOP operates as follows. Provided that System Bus signals BUSRN and MSN are hi (i.e. no other master unit has requested use of the System Bus nor has been selected to use it) and ERQN is lo (i.e. the System Bus is enabled for use), the IOP sets its BUSRN output lo. After an interval (OKODLY), the BM in the CP1A sets its OKO output at AB2-25 hi. This signal is daisy-chained through the master units, and is trapped in that unit which is both requesting use of the System Bus and which has highest priority. Note: In many systems the IOP is the master unit of highest priority. The OKI input to the IOP (OKO output of CP1A) is accepted by the IOP, which sets its OKO output lo to block units of lower priority.

The IOP then sets its MSN output lo to indicate to other units that the Bus has been selected. The OKO output of the CP1A BM is then reset lo and, after a delay, the BUSRN signal is reset hi. The bus logic of the IOP then takes contol of the System Bus and sets BSYN lo. The IOP takes the Bus in LOCK mode i.e. for two consecutive cycles.

The IOP then generates synthetic Software Memory access signals (TMRN hi, WRITE lo) which result in the word at Software Memory address /1046 (/003F) being transferred and temporarily stored in the IOP. The Software Memory access signal TSMN is set lo to signify the end of the access. The IOP then generates a synthetic OTR instruction which sets TMPN lo and WRITE hi, and which transfers the word to the C.U. The C.U. sends TSMN in reply and also transfers the word to the D.U., where it is written onto the selected surface of the selected disk. The C.U. switches from the Execute State to the Exchange State for the transfer and this operation generates a new BRN signal. The IOP again accesses the Software Memory and transfers the second word to itself. Another OTR Command is performed which transfers the second word to the C.U. The C.U. operates as before to transfer the second word to the D.U. This time, however, the OTR Command is accompanied by the MAD03 bit set hi (End-of-Range), and this signal, in association with the C.U. Processor, switches the C.U., via intermediate states, to the Wait State. An interrupt (IRN) is generated which is supplied to the CP1A.

3.9.9 REPEATING THE INTERRUPT AND THE PROGRAM

The interrupt circuits of the CP1A function as previously described, and the CP1A again performs the interrupt routine. At the end of the routine, control branches to address /1034. The instruction at this address causes control to branch to the start of the program.

3.10 MICRODIAGNOSTIC PROGRAM (FIGURE 2.10, 4.1 AND FIRMWARE ASSEMBLY LISTING)

The CP1A Microdiagnostic Program is part of the Firmware Microprogram. It is used to test the CP1A.

3.10.1 TRIGGERED FROM THE HHP

With the CP1A powered up, and with the HHP connected, the HHP can be used to trigger the Microdiagnostic Routine. First, the address of the CU that will be used to check the correct recognition of a CIO Halt instruction is set up on the HHP by pushing the appropriate 0 to F keys. Then the 0 and TEST keys are pushed in quick succession and are held pushed for a second or so to trigger the Microdiagnostic Routine.

Storing CU address:
On Figure 4.1F, the leading edge of the data start pulse at Conn. J3-A1 is slugged by R5 and C8, and is then inverted to a logical 0 level at FG5-8 (RDIN). On Figure 4.1E, RDIN at ED5-4 results in an EPINT which interrupts the µP at Figure 4.1A, AK3-30. The µP switches to Firmware Mode control branches to OP/HHP ROM address F/0002. The number /005A at this address is loaded into the PC and control branches to OP/HHP ROM address F/005A. The PSW and PC are saved at OP/HHP RAM addresses "SAVE" and "SAVE+2".

EPINT routine (data):
Instruction F/005A saves the contents of Register A1 at OP/HHP RAM address "STACK+2". This action is necessary because the following RER /0080 instruction will change the contents of Register A1. The RER /0080 instruction reads the Status Buffer data into Register A1. This data is then anded with /0040 to test if the interrupt is an INIT interrupt. Since, in the case of a Microdiagnostic trigger, it is not control continued with a load instruction that restores the contents of Register A1. A multiple store instruction then saves the contents of Register A1 to A15 on the OP/HHP RAM. Load and store instructions save the PC at OP/HHP RAM address /FFD0 ("STACK"). Test and shift instructions then discover the source of the interrupt and, in this case, control branches to the HHP routine at F/00EC.

This routine loads the OP/HPP RAM stack pointer into Register A14 then employs SDPM-bit periods, delays, counters and shift instructions to assemble the selected CU address in Register A1. It then tests if the information is a data code or a function code. In this case, the information is data, so it is stored at OP/HHP RAM address /FFFA ("DATHHP"). Control then branches to the RETURN routine at F/0098.

RETURN routine:
After resetting the TSBC card and the STOP circuit (neither of which are normally relevant to a Microdiagnostic Routine) the RETURN routine loads the PC into Register A1 and saves the new PC at OP/HHP RAM address /FFFE ("STACK+2"). It then restores the contents of Registers A1 to A15, and a Return-from-Firmware instruction returns control to the software address that is specified by the PC. After a delay, a Halt interrupt will switch the CP1A to the IDLE state (see section 3.6), where it waits for another command.

EPINT routine (function):
When the test code is sent from the HHP to the CP1A, the EPINT interrupt and the EPINT routine function as previously described, and control branches to F/00EC (HHP routine).

HHP routine (function):
This time the HHP routine detects function code TEST and control branches to F/021C (TEST routine).

TEST routine:
The first two instructions of this routine load Register A1 with /0000 and store /0000 in OP/HHP RAM address /FFC8 ("MICROF"). This is a flag which marks that the Microdiagnostic Routine was triggered by the HHP, i.e. that the CIO Halt instruction can be executed.

MICROD routine:
Register A3 is loaded with /0001 to serve as a flag that marks this point in the routine. Control then branches to the VISRUN routine at F/03B2.

VISRUN routine:
This routine assembles the "run" code and sends it to the HHP so that the HHP displays "run". Towards the end of this routine instruction F/03E8 tests the contents of Register A3. If the contents are not /0000 (in this case the contents are /0001) control branches to F/0228.

MICROD routine continued:
Instruction F/0228 loads Register A1 with /8F20 (an ABL instruction) and F/022C stores the instruction at OP/HHP RAM address /FFFC ("CIO+2"). Instruction F/0230 loads Register A1 with /02AE (the long constant for the ABL instruction), and instruction /0234 stores the long constant at OP/HHP RAM address /FFCE ("CIO+4"). The above pair of numbers is used to exit from the CIO instruction. (This action is described later).

TEST CP1A routine:
This routine starts at F/0238. Register A1 is loaded with /1111 and then the contents of A1, together with the contents of A2, are shifted rightward 15 places so that A2 then contains /2222. Then the contents of A2 are loaded into A4 and shifted leftward one place so that A4 contains /4444. The contents of A4 are loaded into A6, whose contents are added to the contents of A4 so that A6 contains /6666. The contents of A6 are then loaded into A1 and shifted leftward one place to cause an overflow. If the overflow is not detected (CR of the PSW is not 11) control branches to an ERROR routine. This is described later. If the overflow is detected (CR of the PSW is 11), the contents of A1 are loaded into A12, which then contains /CCCC. The next instruction takes the complement of the contents of A12 and loads it into A3, which should then contain /3333. The contents of A2 are then loaded into A1, whose contents are shifted rightward circular two places. The result is loaded into A8, which should then contain /8888. Next, the complement of the contents of A8 is loaded into A7, which should then contain /7777. The contents of A7 are loaded into A5. The contents of A5 are shifted leftward one place, and A5 should contain /EEEE. The contents of A5 are then loaded into A14, which should then contain /EEEE. The contents of A5 are exclusive-ored with the contents of A7, and the result is loaded into A9. A9 should then contain /9999. Next, the contents of A14 are ored with the contents of A5, and the result is loaded into A13. A13 should then contain /DDDD. The contents of A7 are then anded with the contents of A5, and the result is loaded into A10. A10 should then contain /5555. The contents of A10 are added to the contents of A10, and the result is loaded into A10, which should then contain /AAAA. The contents of A7 are loaded into A1, from whose contents the contents of A6 are subtracted. The result is loaded into A1, whose contents should then be /1111. The contents of A1 are loaded into A11, to whose contents are added the contents of A10. The result in A11 should be /BBBB. The contents of A11 are loaded into A15, to whose contents the contents of A3 are added. Then the contents of A1 are added to the contents of A15, whose contents should then be /FFFF. A multiple store instruction then stores the contents of A1 to A15 in OP/HHP RAM addresses /FFD2 to /FFEE. Register A1 is loaded with /0000 and this number is stored in OP/HHP RAM address /FFDO ("STACK"). Number /0001 is added to the contents of A15 and, if the result is /0000, control branches to the TEST CU routine at F/0296. If the result is not /0000 control continues with the ERROR routine. An operator can examine the contents of A0 to A15 by using the HHP.

ERROR routine:
When there is an error during the TEST CP1A routine, /0001 is loaded into Register A7. A WER /00F6 instruction writes /0001 on the Outcode Data lines for displaying on the OP, then control branches to the EMIT routine at F/0350.

EMIT routine:
This routine assembles error code /0001 and sends it to the HHP for display. At the end of the routine, control branches to the RETURN routine at F/0098.

RETURN routine:
This routine switches the CP1A to IDLE mode, where it waits for a command i.e. another TEST command or some other command.

TEST CU routine:
Provided that the TEST CP1A routine is successfully concluded, control continues with instruction F/0296. The "MICROF" flag is tested and, because in this case it is /0000, control continues with instruction F/029C. The contents of OP/HHP RAM address "DATHHP", i.e. the selected CU address, are loaded into Register A2. The CU address is then anded with /003F to keep only the l.s. six digits of the address (an address code in the range 000000 to 111111). The result is added to /4180 to generate the CIO Halt instruction code. The instruction is stored in OP/HHP RAM address /FFCA ("CIO HALT"). The branch instruction at F/02AA causes control to branch to OP/HHP RAM address /FFCA (CIO HALT instruction). The instruction is executed and, if the instruction was accepted by the addressed CU, the CR bits of the PSW are set to 00. If this in fact did happen, control branches to F/02B4 (TEST MEMORY routine). If it did not, Register A7 is loaded with /0002 and control branches to F/0209 (ERROR routine). The ERROR, EMIT and RETURN routines are then executed in sequence (as previously described).

TEST MEMORY routine:
Initially, Registers A1 to A4 are cleared so that they can be used as counters and holding registers. Instructions F/02BC to F/02C2 write data pattern /0000 into every location of the Software Memory. Register A3 is reset to contain /0000. Instructions F/02C6 to F/02D0 read the data from every location of the Software Memory, and if any location does not contain /0000 control branches to the ERROR+3 routine. (The ERROR+3 routine is described later.) Register A3 is reset and the next instruction sets the condition code (CR) of the PSW. Provided that CR=00, control branches to F/02E2. Here /0001 is subtracted from the contents of Register A2, which should then contain /FFFF. This number is loaded into Register A3 and control branches to F/02BC. The write and read loops are repeated, but now the program writes pattern /FFFF into every memory location and checks that /FFFF is read from every location: if it was not, control branches to the ERROR 3 routine; if it was, control continues at F/02D2. Register A3 is reset and the condition register is set. This time CR should not =00, so control continues at F/02D8. /0001 is added to the contents of Register A2, which should then contain /0000. If it does, control branches to F/02E8. Here Register A1 is loaded with /0002 and /0002 is subtracted from the contents of Register A2. Control then branches to F/02BC. The write loop is repeated, but now the address reference of each location is written into the referenced location. The read loop then checks that each location contains the correct address reference.

ERROR+3 routine:
/0003 is loaded into Register A7. The faulty address reference is stored in OP/HHP RAM address "STACK"; the written pattern is stored in "STACK+2"; and the read pattern is stored in "STACK+4". Control then branches to the ERROR routine.

The ERROR, EMIT and RETURN routines function as previously described. An operator can read the contents of "STACK", "STACK+2" and "STACK+4" (Registers A0, A1 and A2) by using the HHP.

When the TEST MEMORY routine is successfully concluded, instruction F/02DA causes control to continue at F/02DC. Register A7 is loaded with /0004, and a WER /00F6 instruction writes /0004 on the OUTCODE DATA lines for display on the OP. Control then branches to the EMIT routine, and then to the RETURN routine.

3.10.2 TRIGGERED FROM THE OP

With the CP1A powered up, and with the OP connected, setting the thumbwheel switch of the OP to 0 and then pushing the RUN button triggers the Microdiagnostic Routine.

On Figure 4.1F, the RUNN signal at Conn. J4-A2 is set lo, and the INCODE DATA line inputs at Conn. J4-A6 to A15 are set to xx000000. On Figure 4.1E, the RUNN input at EK5-13 sets EK5-11 hi. This signal clocks ED3-9 lo, whereby an EPINT is generated.

EPINT routine:
This routine functions as previously described, but in this case control branches to F/00D2 (RIPL routine).

RIPL routine:
A WER /000F instruction resets the interrupt. (On Figure 4.1E, the output of EE3-9 (IMADA11) is set lo, and this signal presets ED3-9 lo.) Control then branches to F/0036 (AUTOIPL routine).

AUTOIPL routine:
A RER /00F6 instruction loads INCODE DATA into Register A1. The contents of Register A1 are anded with /003F to eliminate the AR and LOCK bits. If the Contents of the register are then /0000 (and in this case they should be), control branches to F/004C. Instruction /004C loads Register A1 with /0001, and then stores the contents of the register at OP/HHP RAM address /FFF8 ("MICROF"). In this way the program marks that the Microdiagnostic Routine was triggered by the OP. The contents of Register A1 are also stored in OP/HHP RAM address /FFF4 ("IPLSEL"), but this information has no significance during a Microdiagnostic Routine. Control then branches to F/0222 (MICROD routine).

The rest of the microdiagnostic sequence is nearly the same as the one that was previously described, with the following exception: on Figure 2.10C, the test at F/0296 finds that the value of "MICROF" is not /0000, so control bypasses the TEST CU routine and continues with the TEST MEMORY routine.

	M4-15 FIRMN	M4-1 AMA	M4-2 AMB	M4-3 IMAD8 TO IMAD11	M4-4 IMAD 12	M4-7 IMAD 13	M4-6 IMAD 14	M4-5 IMAD 15	M4-9 ENRAZN	M4-10 REQBUSN	M4-11 SEL1N	M4-12 SEL2N	ROM O/P (HEX)	ROM ADDR	FUNCTION
	0	0	X	X	X	X	X	X	1	1	0	0	C	0 TO 63	ROM IPL/ ROM/RAM/ FIRMWARE
	0	1	0	0	X	X	X	X	1	0	1	1	B	64 TO 79	TEST (CIO HALT)
	0	1	0	1	X	X	X	X	1	1	1	1	F	80 TO 95	I/O
	0	1	1	0	X	X	X	X	1	1	1	1	F	96 TO 111	WER/nn*
	0	1	1	1	0	0	0	0	1	1	1	1	F	112	WER/RER/ F0
	0	1	1	1	0	0	0	1	1	0	1	1	B	113	WER/F1
	0	1	1	1	0	0	1	0	1	0	1	1	B	114	WER/F2
	0	1	1	1	0	0	1	1	1	0	1	1	B	115	WER/F3
	0	1	1	1	0	1	0	0	1	0	1	1	B	116	RER/F4
FIRM-WARE	0	1	1	1	0	1	0	1	1	1	1	1	F	117	WER/RER/ F5
	0	1	1	1	0	1	1	0	1	1	1	0	E	118	WER/RER/ F6
	0	1	1	1	0	1	1	1	1	1	0	1	D	119	WER/RER/ F7
	0	1	1	1	1	0	0	0	0	0	1	1	3	120	WER/F8
	0	1	1	1	1	0	0	1	1	1	1	1	F	121	/F9
	0	1	1	1	1	0	1	0	1	1	1	1	F	122	WER/RER/ FA
	0	1	1	1	1	0	1	1	1	1	1	1	F	123	WER/RER/ FB

X = Don't care

* See L4 ROM DECODE

Table 3.3 MODE ROM M4 DECODE

	M4-15 FIRMN	M4-1 AMA	M4-2 AMB	M4-3 IMAD8 TO IMAD11	M4-4 IMAD 12	M4-7 IMAD 13	M4-6 IMAD 14	M4-5 IMAD 15	M4-9 ENRAZN	M4-10 REQBUSN	M4-11 SEL1N	M4-12 SEL2N	ROM O/P (HEX)	ROM ADDR	FUNCTION
	0	1	1	1	1	1	0	0	1	1	1	1	F	124	WER/RER/ FC
	0	1	1	1	1	1	0	1	1	1	1	1	F	125	WER/RER/ FD
	0	1	1	1	1	1	1	0	1	1	1	1	F	126	WER/RER/ FE
	0	1	1	1	1	1	1	1	1	1	0	1	D	127	WER/RER/ FF
	1	0	X	X	X	X	X	X	1	0	1	1	B	128 TO 191	Software RAM
	1	1	0	X	X	X	X	X	1	0	1	1	B	192 TO 223	I/O
	1	1	1	0	X	X	X	X	1	0	1	1	B	224 TO 239	RER/WER/ = /Fn
	1	1	1	1	0	0	0	0	1	1	1	1	F	240	WER/RER/ F0
	1	1	1	1	0	0	0	1	1	1	1	1	F	241	WER/RER/ F1
	1	1	1	1	0	0	1	0	1	1	1	1	F	242	WER/RER/ F2
SOFT-WARE	1	1	1	1	0	0	1	1	1	1	1	1	F	243	WER/RER/ F3
	1	1	1	1	0	1	0	0	1	1	1	1	F	244	WER/RER/ F4
	1	1	1	1	0	1	0	1	1	1	1	1	F	245	WER/RER F5
	1	1	1	1	0	1	1	0	1	1	1	0	E	246	WER/RER/ F6
	1	1	1	1	0	1	1	1	1	1	0	1	D	247	WER/RER/ F7
	1	1	1	1	1	X	X	X	1	1	1	1	F	248 TO 254	WER/RER/ Fn
	1	1	1	1	1	1	1	1	1	1	0	1	D	255	/FF

X = Don't care

Table 3.3 MODE ROM M4 DECODE (CONT.D)

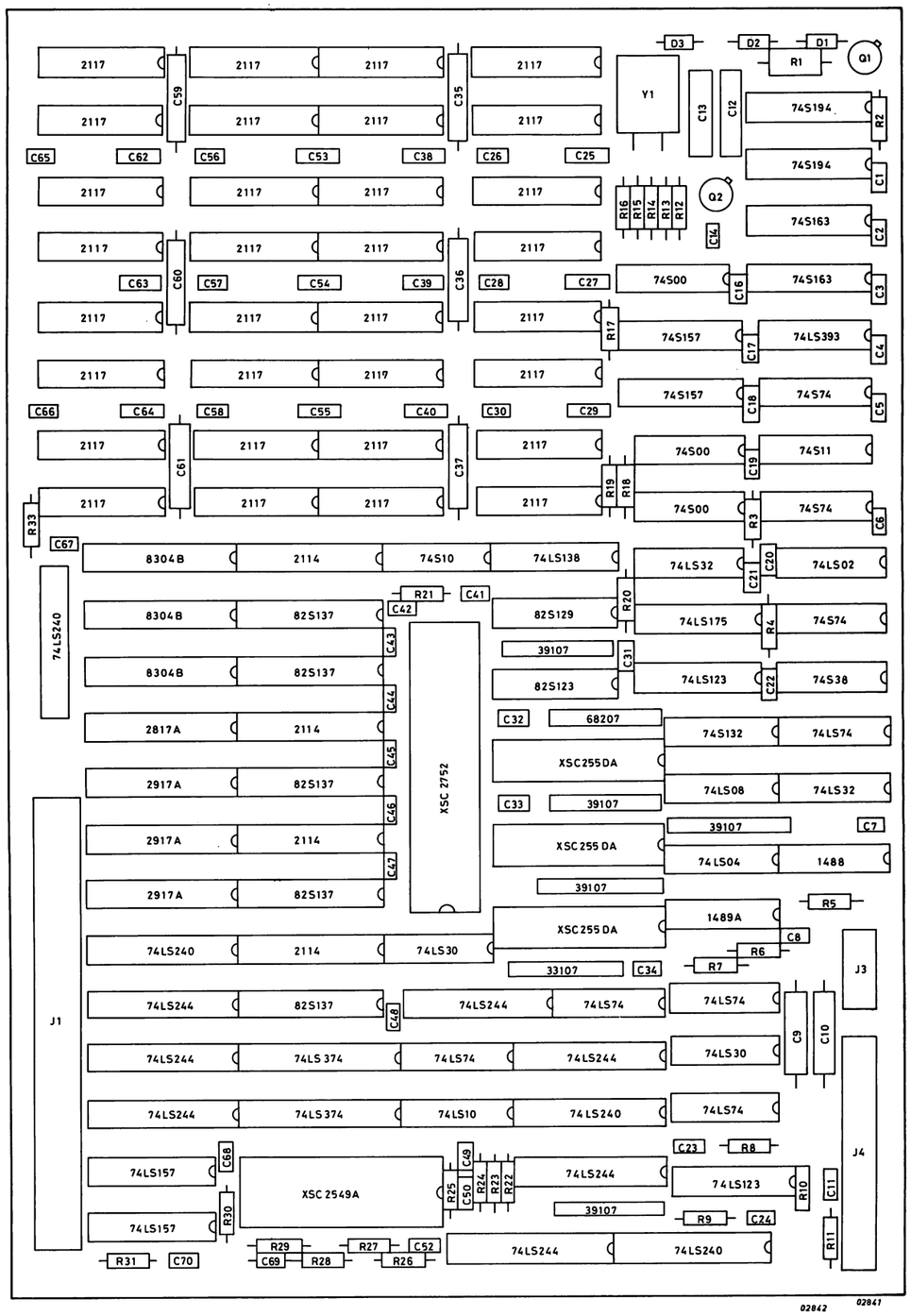
L4-14 SEL1N	L4-13 SEL2N	L4-12 IMAD 01	L4-11 IMAD 02	L4-10 WRITEA	L4-9 CS RAMN	L4-7 CS ROMN	L4-6 CS IPLN	L4-5 CS INTN	L4-4 SWOFAN	L4-3 OUTN	L4-2 EIN-CODN	L4-1 SIRN	ROM ADDR	FUNCTION
0	0	0	0	0	1	0	1	1	1	1	1	1	0	READ ROM
0	0	0	0	1	1	1	1	1	1	1	1	1	1	N.U.
0	0	0	1	0	1	1	0	1	1	1	1	1	2	READ IPL
0	0	0	1	1	1	1	1	1	1	1	1	1	3	N.U.
0	0	1	0	X	1	1	1	1	1	1	1	1	4+5	N.U.
0	0	1	1	X	0	1	1	1	1	1	1	1	6+7	R/W RAM
0	1	0	0	X	1	1	1	0	1	1	1	1	8+9	R/W IHC
0	1	0	1	X	1	1	1	1	1	1	1	1	10 +11	N.U.
0	1	1	0	X	1	1	1	1	1	1	1	1	12 +13	N.U.
0	1	1	1	0	1	1	1	1	1	1	1	0	14	RER/F7
0	1	1	1	1	1	1	1	1	0	1	1	1	15	WER/F7
1	0	0	X	X	1	1	1	1	1	1	1	1	16 TO 19	N.U.
1	0	1	0	X	1	1	1	1	1	1	1	1	20 +21	N.U.
1	0	1	1	0	1	1	1	1	1	1	1	0	22	RER/F6
1	0	1	1	1	1	1	1	1	1	0	1	1	23	WER/F6
1	1	X	X	X	1	1	1	1	1	1	1	1	24 TO 31	N.U.

X = Don't care

N.U. = Not used

Table 3.4 MODE ROM L4 DECODE

4 DIAGRAMS


2117
C59
C35
C65
C62
C56
C53
C38
C26
C25
C60
C36
C63
C57
C54
C39
C28
C27
C61
C37
C66
C64
C58
C55
C40
C30
C29
R33
C67
74LS240
8304B
2114
74S10
74LS138
82S137
82S129
2817A
2917A
74LS30
74LS244
74LS374
74LS10
74LS157
XSC 2549A
XSC 2752
XSC255DA
XSC 255 DA
39107
68207
33107
74S132
74LS74
74LS08
74LS32
74LS04
1488
1489A
74LS123
74S38
74LS175
74S74
74LS02
74S11
74S00
74S157
74S163
74LS393
74S194
74LS163
Y1
Q1
Q2
R1
D1
D2
D3
C13
C12
R16
R15
R14
R13
R12
C44
R2
C1
C2
C16
C3
R17
C17
C4
C18
C5
R19
R18
C19
R3
C6
C20
C21
R20
R4
C31
C22
C32
C33
C7
C8
R5
R6
R7
C34
J1
J3
J4
C9
C10
C11
C23
R8
R9
C24
R10
R11
C68
R30
C49
R25
C50
R24
R23
R22
C52
R29
C69
R28
R27
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C70
C48
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C46
C47
C63
C44
R21
C41
C42
02842
02841

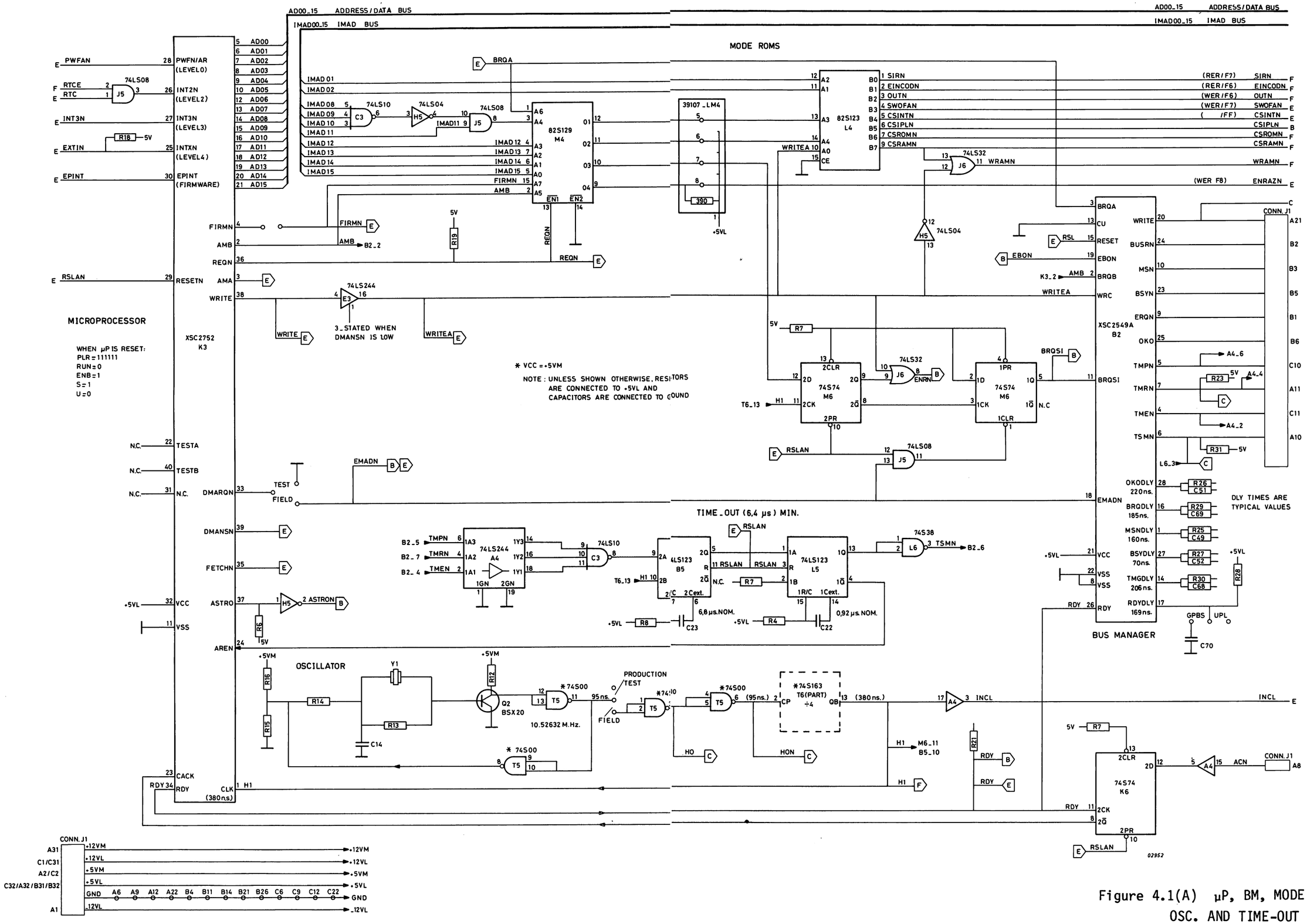


Figure 4.1(A) µP, BM, MODE ROMS, OSC. AND TIME-OUT LOGIC

AD 00_15 ADDRESS/DATA BUS

ADDRESS/DATA BUS AD00_15

68207 KL4 AD00 01 02 03 04 05 7 6 5 4 3 2 6K8 1 +5VL

IPL ROM

IMAD05 15 06 16 07 17 08 1 09 2 10 3 11 4 12 7 13 6 14 5 — 82S137 M2 — 04 11 AD12, 03 12 13, 02 13 14, 01 14 15, CE1, CE2 10 — A CSIPLN

74LS244 E1: 2 4 6 8 17 15 13 11 — 1A1 1A2 1A3 1A4 2A4 2A3 2A2 2A1 — 1Y1 1Y2 1Y3 1Y4 2Y4 2Y3 2Y2 2Y1 — 18 16 14 12 3 5 7 9 MADE0 — 1G 2G 1 19 — A EMADN

74LS240 F1: 2 4 6 8 17 15 13 11 — 1A1 1A2 1A3 1A4 2A4 2A3 2A2 2A1 — 1Y1 1Y2 1Y3 1Y4 2Y4 2Y3 2Y2 2Y1 — 18 16 14 12 3 5 7 9 — 1G 2G 1 19

74LS30 F3: 1 11 12 2 6 5 4 3 — 8 ENEM C

CONN. J1

MADE00 01 02 03 04 05 06 07 — B12 B13 B15 B16 B17 B18 B19 B20

MAD00 01 02 03 04 05 06 07 — C13 A13 C14 A14 C15 A15 C16 A16

MAD08 09 10 11 12 13 14 15 — C17 A17 C18 A18 C19 A19 C20 A20

MAD00_15 C

ADDRESS LATCH

74LS374 C2: AD00 8 01 18 02 3 03 17 04 7 05 14 06 4 07 13 — 4D 8D 1D 7D 3D 6D 2D 5D — 4Q 8Q 1Q 7Q 3Q 6Q 2Q 5Q — 9 19 2 16 6 15 5 12 IMAD00 01 02 03 04 05 06 07 — CLK 11 — OUTPUT CONTROL 1 — A ASTRON

74LS374 D2: AD08 3 09 18 10 4 11 17 12 7 13 13 14 8 15 14 — 1D 8D 2D 7D 3D 5D 4D 6D — 1Q 8Q 2Q 7Q 3Q 5Q 4Q 6Q — 2 19 5 16 6 12 9 15 IMAD08 09 10 11 12 13 14 15 — CLK 11 — CONTR. 1

ADDRESS BUFFER

74LS244 C1: IMAD00 8 01 11 02 6 03 13 04 4 05 15 06 2 07 17 — 1A1 2A1 1A2 2A2 1A3 2A3 1A4 2A4 — 1Y4 2Y1 1Y3 2Y2 1Y2 2Y3 1Y1 2Y4 — 12 9 14 7 16 5 18 3 MAD00 01 02 03 04 05 06 07 — 1G 2G 1 19 — A EMADN

74LS244 D1: IMAD08 8 09 11 10 6 11 13 12 4 13 15 14 2 15 17 — 1A1 2A1 1A2 2A2 1A3 2A3 1A4 2A4 — 1Y4 2Y1 1Y3 2Y2 1Y2 2Y3 1Y1 2Y4 — 12 9 14 7 16 5 18 3 MAD08 09 10 11 12 13 14 15 — 1G 2G 1 19

IMAD00_15 IMAD BUS

IMAD BUS IMAD00_15

BIO 00N_15N D

A RDY — N.C. 10 1

2917A G1: AD00 13 01 17 02 3 03 7 00 12 01 18 02 2 03 8 — A2 A3 A0 A1 R2 R3 R0 R1 — ODD RLE — BUS2 BUS3 BUS0 BUS1 — 14 16 4 6 BIO00N 01N 02N 03N — OE 11 BE 9 DRCP 19 — A ENRN A EBON A BRQSI

2917A H1: AD04 13 05 17 06 3 07 7 04 12 05 18 06 2 07 8 — A2 A3 A0 A1 R2 R3 R0 R1 — OE BE DRCP — BUS2 BUS3 BUS0 BUS1 — 14 16 4 6 BIO04N 05N 06N 07N — ODD RLE — N.C. 10 1 — A RDY

2917A J1: AD08 13 09 17 10 3 11 7 08 12 09 18 10 2 11 8 — RLE — BUS2 BUS3 BUS0 BUS1 — 14 16 4 6 BIO08N 09N 10N 11N — BE 9 DRCP 19 — ENRN EBON BRQSI

2917A K1: AD12 13 13 17 14 3 15 7 12 12 13 18 14 2 15 8 — BE DRCP — BUS2 BUS3 BUS0 BUS1 — 14 16 4 6 BIO12N 13N 14N 15N — DD RLE — N.C. 1 19 — RDY

CONN. J1

BIO 00N 01N 02N 03N 04N 05N 06N 07N 08N 09N 10N 11N 12N 13N 14N 15N — A23 A24 A25 A26 A27 A28 A29 A30 C23 C24 C25 C26 C27 C28 C29 C30

02900

DATA LATCH

Figure 4.1(B) ADDRESS AND DATA LATCHES AND IPL ROM

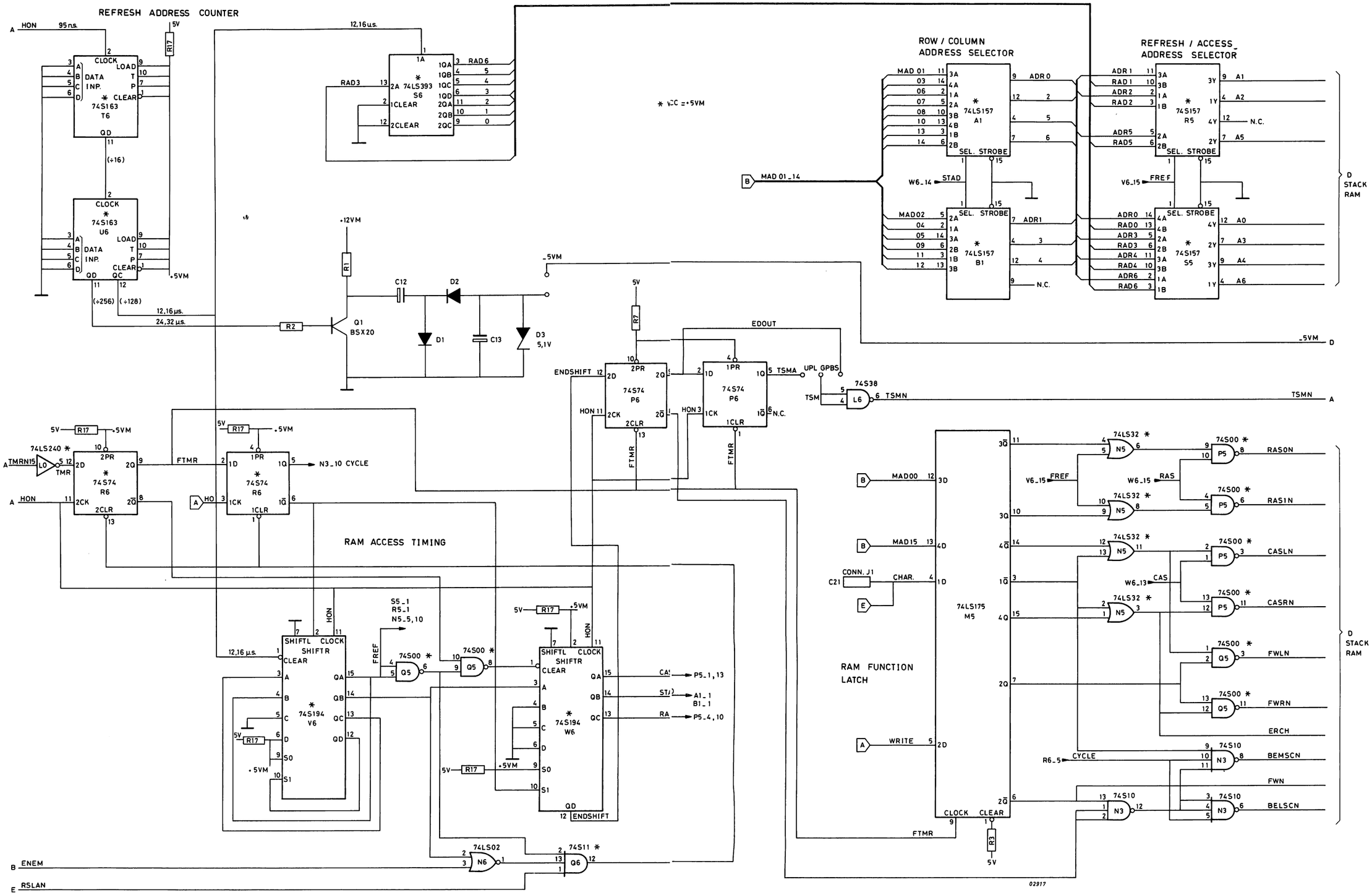


Figure 4.1(C) STACK RAM CONTROL LOGIC

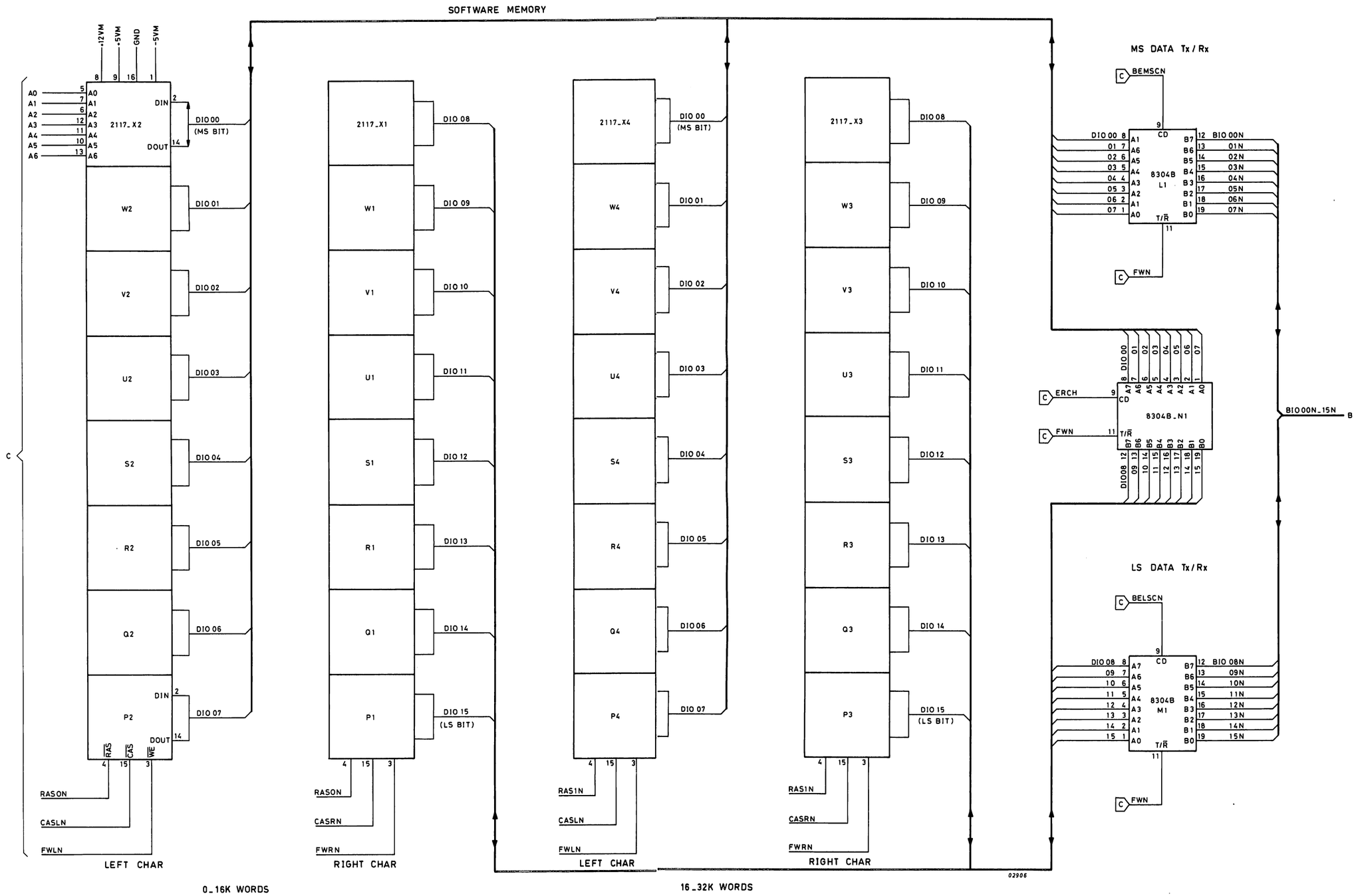


Figure 4.1(D) STACK RAM

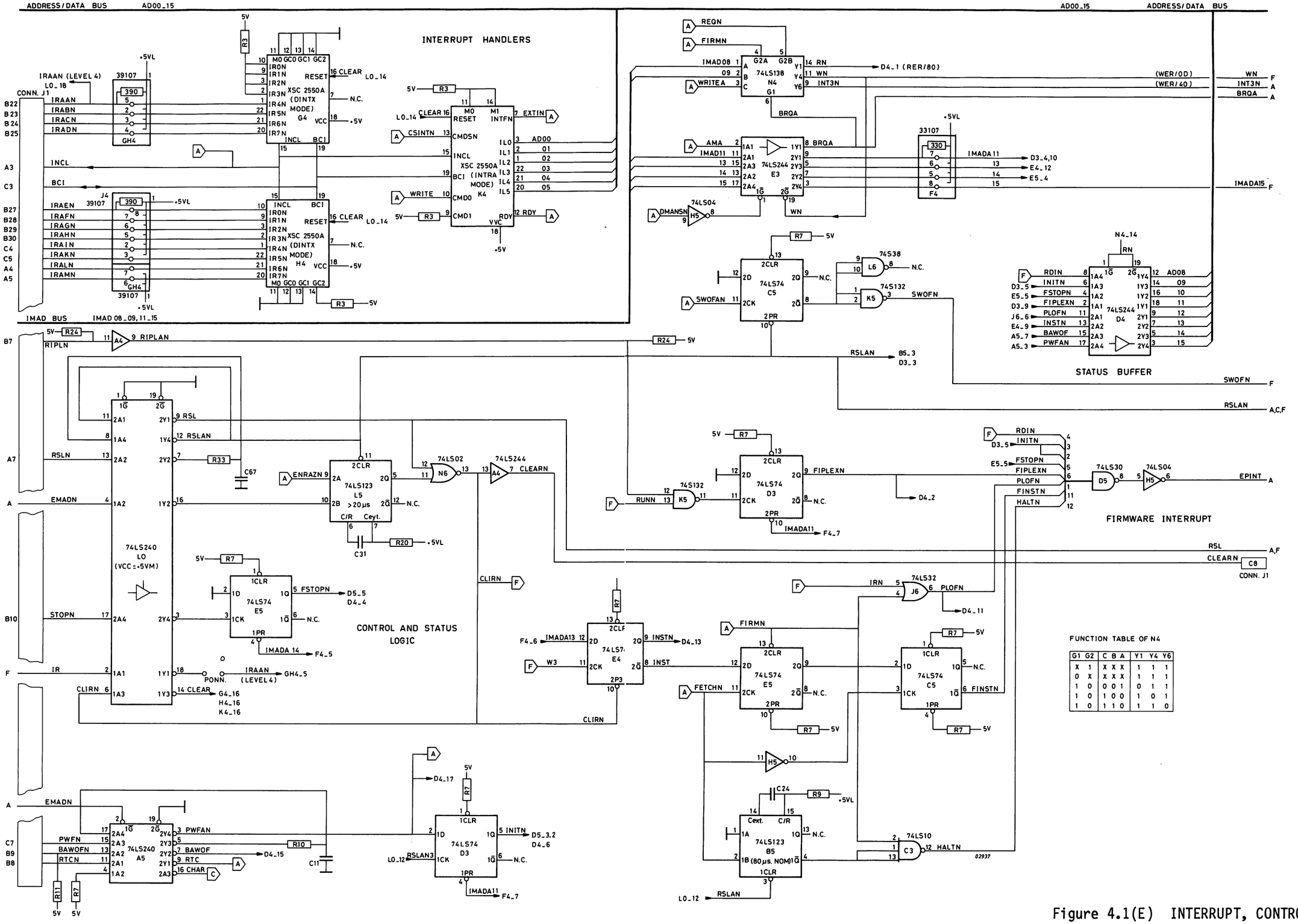


Figure 4.1(E) INTERRUPT, CONTROL AND STATUS LOGIC

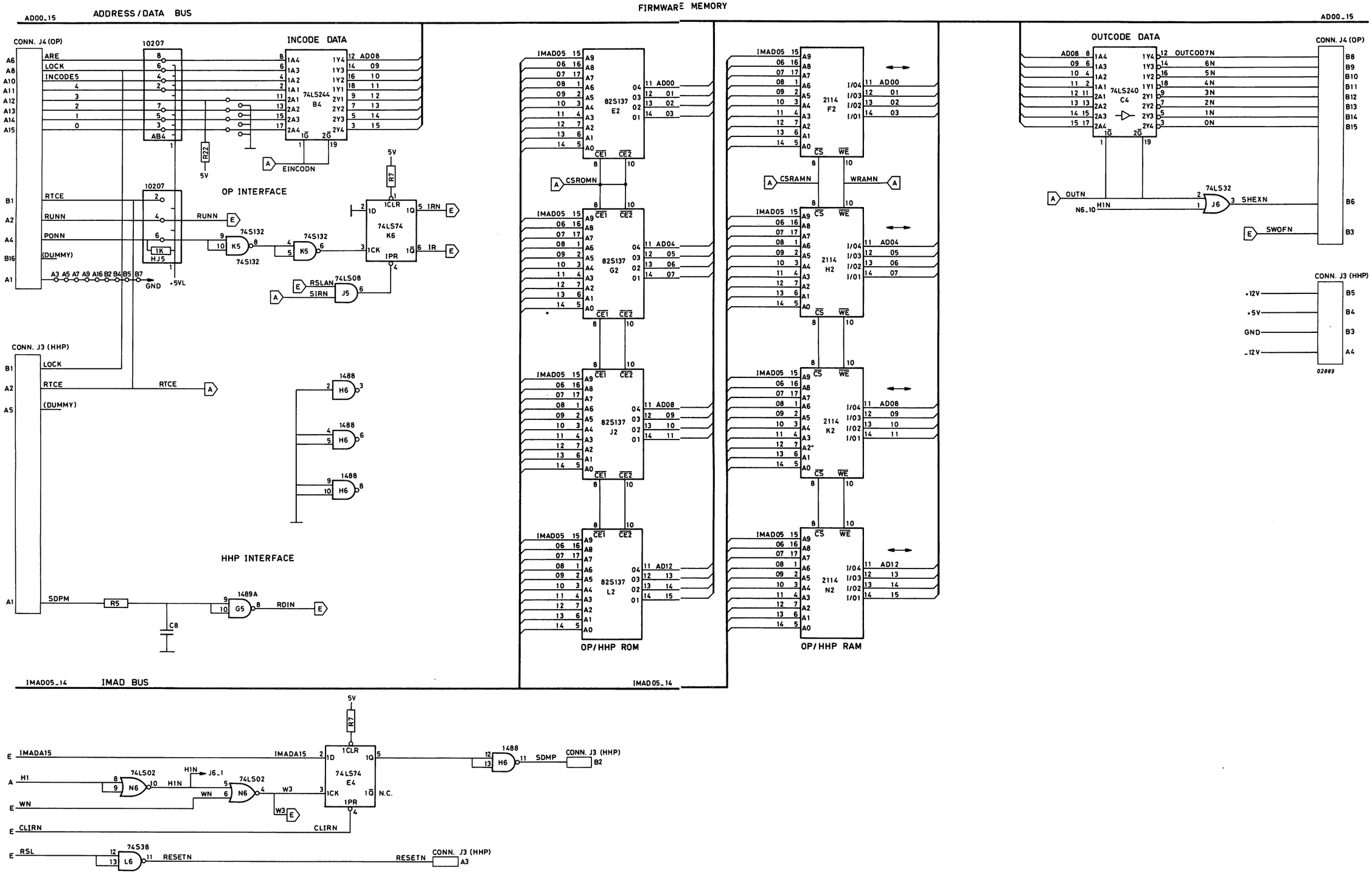
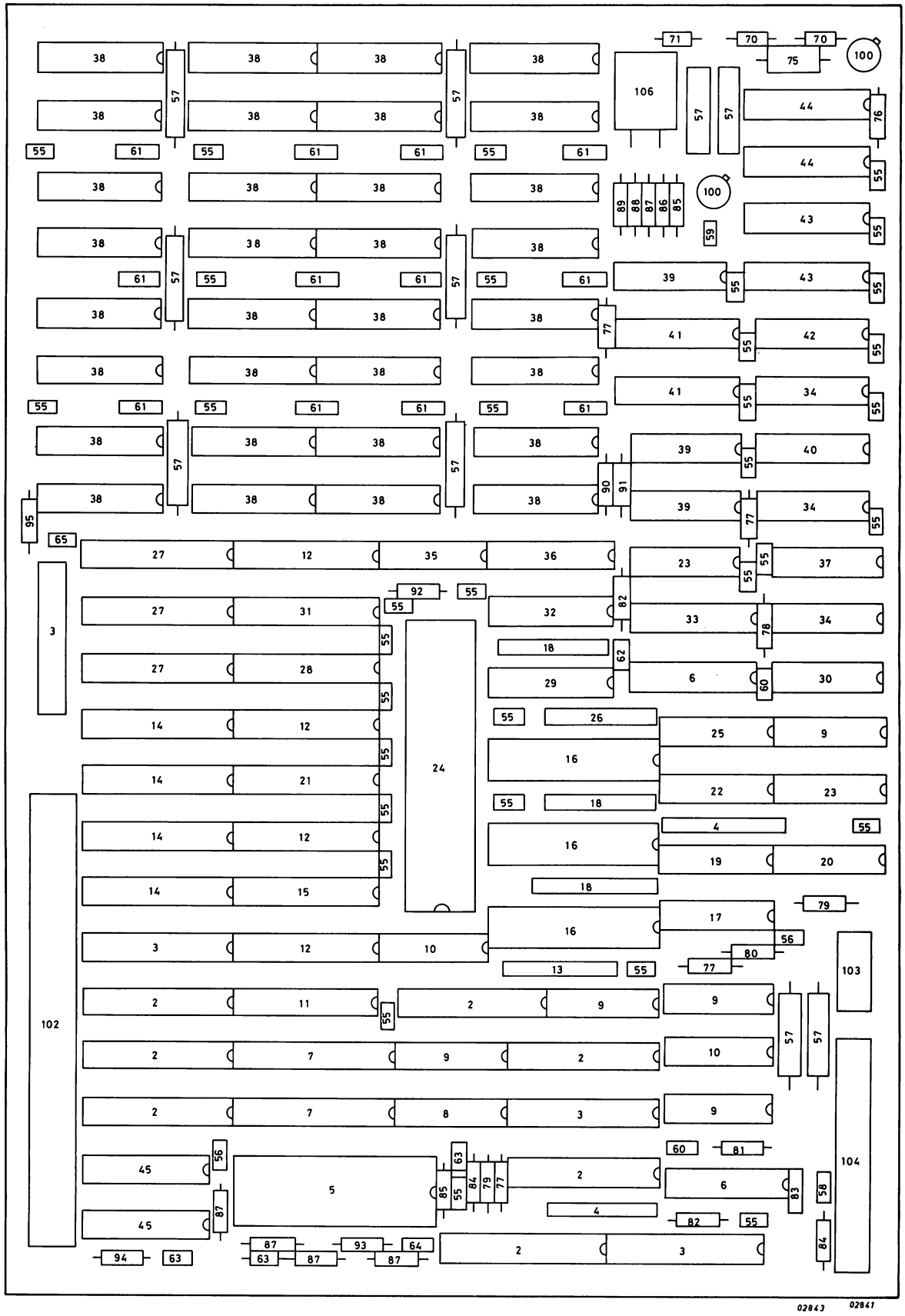


Figure 4.1(F) OP/HHP INTERFACES AND FIRMWARE

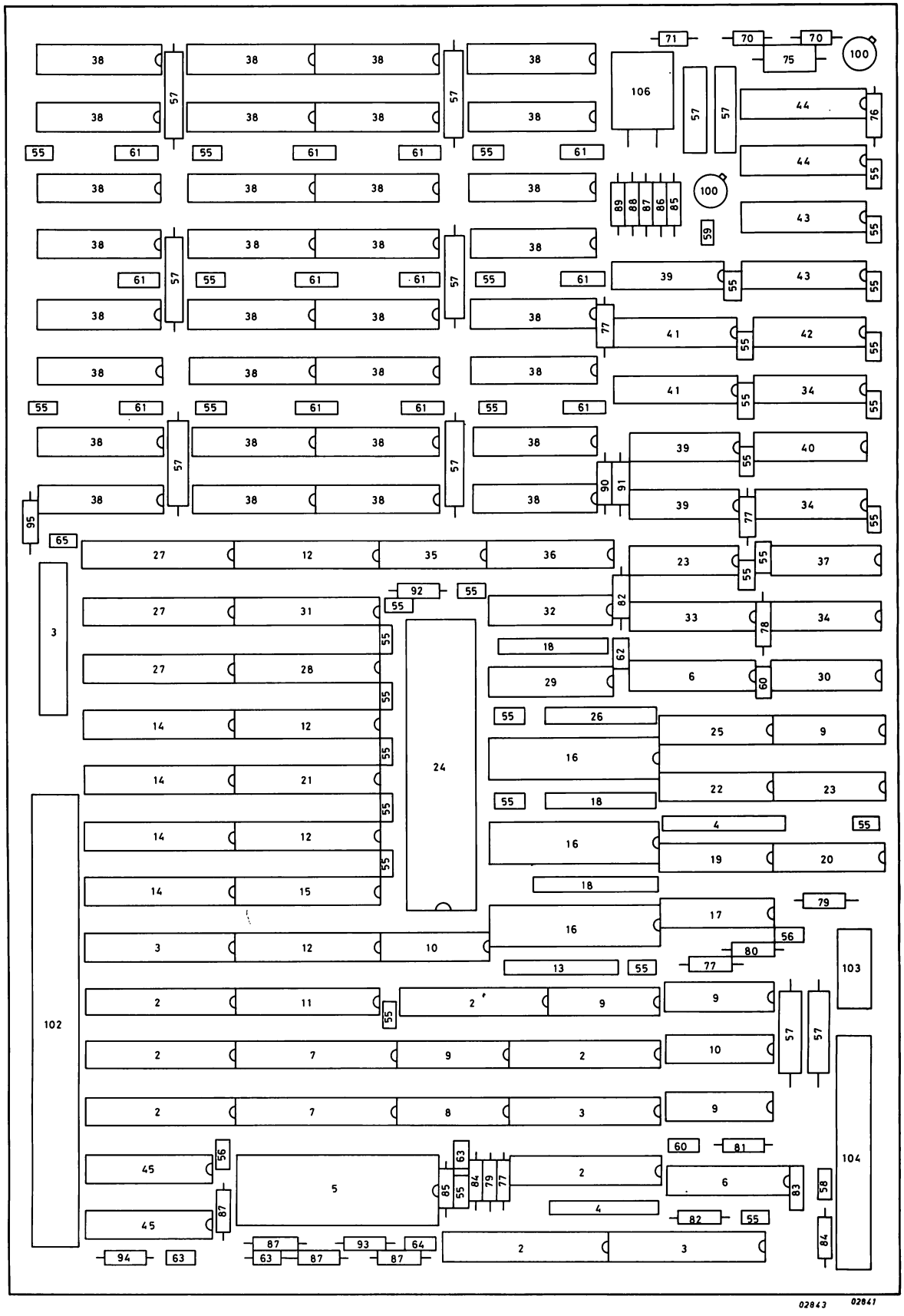
5 LISTINGS

Listings are not included in this document because of their limited usefullness, their bulk and related cost.
One copy of the listings will be made available to the LMO's upon receipt of a written request by an authorized official.

6 PARTS LIST


02843
02841

Pos.	Code Number	Description
1	5111 199 66810	PCBCP1A
2	5111 000 04261	IC 74LS244
3	5111 000 04091	IC 74LS240
4	5111 000 04191	IC 102-07
5	5111 000 04911	IC XSC 2449A
6	5111 000 03801	IC 74LS123
7	5111 000 03941	IC 74LS374
8	5111 000 03641	IC 74LS10
9	5111 000 02831	IC 74LS74
10	5111 000 02801	IC 74LS30
11	5111 010 05331	IC 82S137
12	5111 000 04201	IC 2114
13	5111 000 05521	IC 331-07
14	5111 000 04251	IC 2917A
15	5111 010 05341	IC 82S137
16	5111 011 30761	IC XSC 2550A
17	5111 000 01881	IC 1489A
18	5111 000 04241	IC 391-07
19	5111 000 02661	IC 74LS04
20	5111 000 01871	IC 1488
21	5111 010 05351	IC 82S137 (PROM 5351)
22	5111 000 02701	IC 74LS08
23	5111 000 02721	IC 74LS32
24	5111 010 04861	IC XSC 2752
25	5111 000 04071	IC 74S132
26	5111 000 05531	IC 682-07
27	5111 000 04371	IC 8304D
28	5111 010 05361	IC 82S137 (PROM 5361)
29	5111 010 05311	IC 82S123 (PROM 5311)
30	5111 000 04291	IC 74S38
31	5111 010 04601	IC 82S137 (IPL 4601)
32	5111 010 05321	IC 82S129 (PROM 5321)
33	5111 000 02891	IC 74LS175
34	5111 000 00791	IC 74S74
35	5111 000 00921	IC 74S10
36	5111 000 02511	IC 74LS138
37	5111 000 02711	IC 74LS02
38	5111 000 05501	IC 2117
39	5111 000 00481	IC 74S00
40	5111 000 00801	IC 74S11
41	5111 000 02451	IC 74S157
42	5111 000 03871	IC 74LS393
43	5111 000 03761	IC 74S163
44	5111 000 02551	IC 74S194
45	5111 000 02691	IC 74LS157


02843
02841

Pos.	Code Number	Description
55	2222 629 01103	Capacitor 10nF
56	2222 631 58221	Capacitor 220pF
57	2222 015 16109	Capacitor 10µF
58	2222 630 01332	Capacitor 3,3nF
59	2222 631 58331	Capacitor 330pF
60	2222 631 58101	Capacitor 100pF
61	2022 552 00977	Capacitor 1µF, 50V
62	2222 630 01392	Capacitor 3,9nF
63	2222 631 58151	Capacitor 150pF
64	2222 631 58829	Capacitor 82pF
65	2222 630 01472	Capacitor 4,7nF
70	9330 228 60112	Diode BAX13
71	9331 177 20112	Diode BZX79,5.1V
75	2322 212 13471	Resistor 470E, 0.5W, 5%
76	2322 211 13152	Resistor 1K5, 0,125W, 1%
77	2322 211 13102	Resistor 1K, 0,125W, 1%
78	2322 151 51783	Resistor 17K8, 0,125W, 1%
79	2322 211 13221	Resistor 220E, 0,25W, 5%
80	2322 211 13272	Resistor 2K7, 0,25W, 5%
81	2322 151 51474	Resistor 147K, 0,125W, 1%
82	2322 151 53163	Resistor 31K6, 0,125W, 1%
83	2322 211 13331	Resistor 330E, 0,125W, 1%
84	2322 211 13681	Resistor 680E, 0,125W, 1%
85	2322 151 51472	Resistor 1K47, 0,125W, 1%
86	2322 151 53162	Resistor 3K16, 0,125W, 1%
87	2322 151 52152	Resistor 2K15, 0,125W, 1%
88	2322 151 56811	Resistor 681E, 0,125W, 1%
89	2322 151 54641	Resistor 464E, 0,125W, 1%
90	2322 211 13751	Resistor 750E, 0,125W, 1%
91	2322 211 13302	Resistor 3K, 0,25W, 5%
92	2322 211 13162	Resistor 1K6, 0,25W, 5%
93	2322 151 51782	Resistor 1K78, 0,125W, 1%
94	2322 211 13821	Resistor 820E, 0,25W, 5%
95	2322 211 13391	Resistor 390E, 0,125W, 1%
100	9330 219 20112	Transistor BSX20
102	2411 029 08123	Connector 3x32 pins
103	5111 100 30541	Connector 2x5 pins
104	5111 100 40321	Connector 2x16 pins
106	2411 535 01525	Crystal 10.52632 MHz.

IDENTIFICATION CODE NUMBER	SERVICE CODE NUMBER	DESCRIPTION
2222 015 16109	4822 124 20697	CAP.10UF 25V
2222 629 01103	4822 122 30043	CAP.10NF
2222 630 01122	4822 122 30054	CAP.1,2NF
2222 630 01332	4822 122 30099	CA.3.3NF
2222 630 01471	4822 122 30034	CAP.470PF
2222 630 01472	4822 122 30128	CAP.4.7NF
2222 631 10339	4822 122 31067	CAP.33PF
2222 631 58101	4822 122 31081	CAP.100PF
2222 631 58121	4822 122 30093	CAP.120PF
2222 631 58221	4822 122 31173	CAP.220PF
2222 631 58331	4822 122 31353	CAP.330PF
2222 631 58829	4822 122 31078	CAP.82PF
2322 151 51212	5322 116 54557	RES.1,21K 0,125W 1%.
2322 151 51472	5322 116 50635	RES.1,47K 0,125W 1%.
2322 151 51474	5322 116 54712	RES.147K 0,125W 1%.
2322 151 51783	5322 116 54637	RES.17,8K 0,125W 1%.
2322 151 52152	5322 116 50767	RES.2',15K 0,125W 1%.
2322 151 53162	5322 116 50579	RES.3,16K 0,125W 1%.
2322 151 53163	5322 116 54657	RES.31,6K 0,125W 1%.
2322 151 54641	5322 116 50536	RES.464E 0,125W 1%.
2322 151 56811	5322 116 54534	RES.681E 0,125W 1%.
2322 211 13102	4822 110 63107	RES.1K 0,25 W 5%.
2322 211 13112	4822 110 60108	RES.1,1K 0,25 W 5%.
2322 211 13152	4822 110 63112	RES.1,5K 0,25 W 5%.
2322 211 13162	4822 110 60113	RES.1,6K 0,25 W 5%.
2322 211 13221	4822 110 63089	RES.220E 0,25 W 5%.
2322 211 13272	4822 110 63118	RES.2,7K 0,25 W 5%.
2322 211 13302	4822 110 60119	RES.3.0K 0,25 W 5%.
2322 211 13331	4822 110 63094	RES.330E 0,25 W 5%.
2322 211 13391	4822 110 63096	RES.390E 0,25 W 5%.
2322 211 13681	4822 110 63103	RES.680E 0,25 W 5%.
2322 211 13751	4822 110 60104	RES.750E 0,25 W 5%.
2322 211 13821	4822 110 63105	RES.820E 0;25W 5% .
2322 212 13471	4822 110 53098	RES.470E 0,5W 5%.
2411 011 07257	5322 268 14116	PIN QW786
2411 024 13001	5322 268 94029	JUMPER DCW06
2411 535 01525	5322 242 74376	CRYSTAL 10,52632MHZ.
5111 000 00481	5322 209 84167	IC SN74S00N-00
5111 000 00791	5322 209 84183	IC SN74S74N-00
5111 000 00801	5322 209 85604	IC N74LS11A
5111 000 00921	5322 209 84954	IC SN74S10N
5111 000 01871	5322 209 85621	IC COM1488
5111 000 01881	5322 209 85619	IC 1489A
5111 000 02451	5322 209 85669	IC SN74S157N
5111 000 02511	5322 209 85647	IC N74LS138B
5111 000 02551	5322 209 85742	IC N74S194F
5111 000 02661	5322 209 85486	IC N74LS04A
5111 000 02691	5322 209 85489	IC N74LS157B
5111 000 02701	5322 209 84995	IC SN74LS08N-00
5111 000 02711	5322 209 85312	IC N74LS02A
5111 000 02721	5322 209 85311	IC N74LS32A
5111 000 02801	5322 209 84985	IC SN74LS30N-00
5111 000 02831	5322 209 84986	IC SN74LS74N-00
5111 000 02891	5322 209 84999	IC SN74LS175N-00
5111 000 03641	5322 209 84996	IC N74LS10A
5111 000 03761	5322 209 85454	IC SN74S163N
5111 000 03801	5322 209 85266	IC SN74LS123N
5111 000 03871	4822 209 80447	IC N74LS393N
5111 000 03941	5322 209 85869	IC SN74LS37AN
5111 000 04071	5322 209 85267	IC SN74LS32N-00

IDENTIFICATION CODE NUMBER	SERVICE CODE NUMBER	DESCRIPTION
5111 000 04091	5322 209 85862	IC SN74LS240N
5111 000 04191	5322 111 94145	R.NETW.10207(7X1K) .
5111 000 04201	5322 209 14492	IC D2114
5111 000 04241	5322 111 94221	R.NETW.39107(7X390E)
5111 000 04261	5322 209 86017	IC N74LS244N
5111 000 04291	5322 209 85677	IC N74S38A
5111 000 04371	5322 209 86211	IC.8304B
5111 000 05221	5322 255 44112	IC.MOUNTING 18 PINS.
5111 199 66810	5322 216 25616	PCB CP1A
9330 219 20112	5322 130 40417	TRANSISTOR BSX20
9330 228 60112	4822 130 31011	DIODE BAX13
9331 177 20112	4822 130 34233	DIODE BZX79C5V1
9334 301 70112	5322 209 14841	IC 2117-4(250NS) .

END OF REPORT