DEC-11-HCRMA-C-D

CR11/CM11
card reader
system manual

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CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

The CR11/CM11 Card Reader System is a card handling system designed to interface with the PDP-11 family of processors and peripherals to read marked or punched Hollerith data cards at rates up to 600 cards per minute. The CR11/CM11 System consists of two distinct components: a card reader and a DEC PDP-11 interface unit, which is referred to as the CR11 Controller.

a. Card Reader — A motorized card handling device that reads information from EIA standard (Hollerith code) cards. The unit reads 12-row, 80-column cards at a nominal rate of 200 to 600 cards per minute, depending on the specific card reader used.

The CR11 System is fully compatible with Documation(TM) punched card and mark/sense readers and GDI punched card and mark/sense readers.

b. CR11 Controller — An interface between the card reader and the PDP-11 Unibus. Controls data transfers between the card reader and other devices in a PDP-11 System. Provides a 12-bit output character for standard data transfers and an 8-bit output character (one byte) when it is desired to use the proposed compressed Hollerith code. Also monitors reader operation and issues appropriate control commands.

The controller is completely plug-compatible with the above-mentioned card readers; no modifications are required.

Also referred to an "control unit", "interface", and "reader control".

1.2 SCOPE

This manual provides the user with the information needed to operate the CR11/CM11 Card Reader System and provides the theory of operation and logic diagrams necessary to understand and maintain the CR11 Controller. The CR11/CM11 Card Reader System is referred to in this manual as the CR11 Card Reader System.

This manual and the appropriate card reader manual must be used together for a complete understanding of the entire CR11 System. The prime subject of this manual is the CR11 Controller. In addition to providing complete coverage of the controller, this manual includes sections covering overall system operation and programming. Because of the number of different card readers that can be used with the CR11 Controller, this manual only covers the operation of the Documation Model M200 Card Reader. Operation of other card reader models, as well as any significant differences, are included in Appendix A.

(TM) Documation is a trademark of Documation, Incorporated, Melbourne, Florida.

The prime subject of the card reader manual is the card reader itself. The manual presents a detailed discussion of the print mechanism and electronics including installation, operation, principles of operation, maintenance, troubleshooting, and engineering drawings.

Table 1-1 lists related PDP-11 System documents that are applicable to the CR11 Card Reader System.

Table 1-1
Applicable Documents

Title	Number	Coverage
*PDP-11/20 System** (7-volume series)	DEC-11-HR1B-D through DEC-11-HR7B-D	Provides detailed theory of operation, flow, logic diagrams, operation, installation, and maintenance for components of the PDP-11 System including processor, memory, console, and power supply.
PDP-11 Processor Handbook	DEC, 1972	A two-part general handbook. The first part discusses system architecture, addressing modes, the instruction set, and programming techniques. The second part is devoted to a discussion of software.
PDP-11 Peripherals and Interfacing Handbook	DEC, 1972	A two-part handbook. The first part is devoted to a discussion of the various peripherals used with PDP-11 Systems. The second part provides detailed theory, flow, and logic descriptions of the Unibus and external device logic; methods of interface construction; and examples of typical interfaces.
Paper-Tape Software Programming Handbook	DEC-11-GGPB-D	Provides a detailed discussion of the PDP-11 software system used to load, dump, edit, assemble, and debug PDP-11 programs; input/output programming; and the floating-point and math package.

*Applicable PDP-11/05, 11/15, and 11/45 manuals provide system coverage on other PDP-11 Systems.

1.3 SPECIFICATIONS

Operating and physical specifications for the CR11 Controller are given in Table 1-2. Specifications for all Documation type card readers are given in Table 1-3, specifications for GDI (General Design, Inc.) card readers are given in Table 1-4, and Table 1-5 lists the model variations of optical card readers.

1.4 MAINTENANCE

The basic maintenance philosophy of the CR11 Card Reader System is to present the user with the information necessary to understand normal system operation. The user can utilize this information when analyzing trouble symptoms to determine necessary corrective action. It is beyond the scope of this manual to present detailed troubleshooting information.

Table 1-2
CR11 Controller Specifications

Registers:	Status Register (CRS) Data Buffer Register (CRB1) Data Buffer Register Encoded Output (CRB2)
Register Addresses:	CRS 777160 CRB1 777162 CRB2 777164
Data Outputs:	CRB1 = 12-bit character (Hollerith code) CRB2 = 8-bit character (compressed Hollerith code)
Interrupts:	Priority = BR6 (may be changed by jumper plug) Vector = location 230 Types = error, transition to on-line, column ready, and card done
Commands:	Read, eject, and interrupt enable
Status Indications:	Error conditions = error, card supply error, card reader check, timing error Operational conditions = reader ready, reader transition to on-line, busy, column ready, card done
Card Reader Compatibility:	Plug-compatible with Documation and GDI card readers. If reader handles only punched cards, two jumpers must be removed from status register; if reader handles both punched and mark sense cards, no modification needed.
Size:	The CR11 Controller consists of a single quad module (M8290) that occupies 1/4 of a DD11-A or one of two controller slots in a KA11, KC11, or other PDP-11 Processor System unit.
Power:	1.5A @ +5V (derived from H720 Power Supply in mounting box where controller is installed).

Table 1-3
Documation Card Reader Specifications

All Punched Card Models		OM200
Card Type:	Standard 80-column EIA card	Standard 80-column EIA card
Light Source:	Infrared light emitting diode	Fiber Optics, 13 Channel
Read Station:	Photo transistor, 12 bit simultaneously	Photo transistor, 12 data rows and 1 Clock row
Electronics:	7400 Series TTL integrated circuit logic	7400 Series TTL integrated circuit logic
Internal Clock	Crystal oscillator	

Variations

	Model M200 & OM200	Model M300	Model M600
Card Rate (cards/minute)	285	300	600
Hopper/Stacker Card Capacity	550	1000	1000
Power (in VA):			
Starting Load	1600	1600	1600
Running Load	600	600	600

(continued on next page)

Table 1-3 (Cont)
Documation Card Reader Specifications

Variations (cont)			
	Model M200 & OM200	Model M300	Model M600
Dimensions:			
Height	11 in.	13-9/16 in.	19-9/16 in.
Width	19-1/4 in.	23-1/16 in.	23-1/16 in.
Depth	14 in.	18 in.	18 in.
Weight	60 lb	75 lb	75 lb

Table 1-4
GDI Card Reader Specifications

Both Models (100 and 100M)	
Card Type:	Standard 80-column EIA card
Card Rate:	200 cards/minute (nominal)
Rate Control:	Frequency of pick (read) command at discretion of controller
Hopper/Stacker Card Capacity:	450 cards
Read Station:	Silicon photocells, 12 bits simultaneously
Internal Clock:	Timing disk and photocell
Electronics:	Positive logic DTuL 930 series integrated circuits
Input Power:	115 ± 10 Vac, 60 Hz, single-phase
Power Consumption:	Less than 300W
Size:	14 in. wide, 18 in. deep, 18 in. high
Variations	
Weight:	Model 100 = 47 lb Model 100M = 52 lb
Card Type:	Model 100 = Reads only 80-column punched cards Model 100M = Reads punched or marked 40-column cards with clock track

General PDP-11 maintenance information is presented in the *PDP-11 Conventions Manual,* DEC-11-HR6B-D. Detailed maintenance and troubleshooting information is normally included in each manual covering a specific card reader.

1.5 ENGINEERING DRAWINGS

A complete set of reduced engineering drawings and module circuit schematics is provided in a companion volume to this manual entitled *CR11 Card Reader System, Engineering Drawings.* A list of these drawings is presented in Table 1-6. The general logic symbols used on these drawings are described in the *DEC Logic Handbook,* 1971. Specific symbols and conventions are also included in the *PDP-11 Conventions Manual,* DEC-11-HR6B-D.

Table 1-5
Optical Card Reader Models

Option No.	Manufacturer & Model No.	Voltage	Frequency in Hz
CM11	GDI, 100M	115	60
CM11-A	GDI, 100M	230	50
CM11-FA	Documation, 0M200	115	60
CM11-FB	Documation, 0M200	230	50

Table 1-6
Master Drawing List

Drawing No.	No. of Sheets	Title
A-ML-CR11-0	2	Card Reader Control
A-PL-CR11-0-0	1	Card Reader Control Parts List
D-MU-CR11-0-01	1	CR11 Module Utilization
A-PL-CR11-0-01	1	CR11 Module Parts List
D-BS-CR11-0-02	1	Device Control
D-CS-M8290-1	4	Reader Control

1.6 TERMINOLOGY

The *PDP-11 Conventions Manual,* DEC-11-HR6B-D, contains a list of terminology and abbreviations used with the PDP-11 family of systems. A glossary of PDP-11 terms, as well as general computer and programming terms, is also included.

CHAPTER 2
GENERAL DESCRIPTION

2.1 INTRODUCTION

The CR11 Card Reader System is designed to operate on-line with the PDP-11 System and associated peripherals such as magnetic tape units, line printers, or communications terminals. The card reader is a self-contained table-top unit consisting of a motorized card deck, read electronics, local control logic, and an internal power supply. The controller, which interfaces the card reader to the Unibus(TM), consists of a single quad module mounted in 1/4 of a system unit (slots 1, 2, 3, or 4 in a DD11-A Peripheral Mounting Panel). Thus, four reader control interfaces can be mounted in the space of a single system unit. The interface is connected to the card reader by a single cable.

Various card reader models may be used in this system. This manual describes the Documation Model M200. Although other models are similar and are compatible with this system, they may differ in card reading rates, indicator panels, etc. The other card reader models are covered in Appendix A.

2.2 SYSTEM OPERATION

A read instruction from the controller moves a card from the input hopper into the read station where all 80 columns are read on a column-by-column basis beginning with column 1. The card data may be read in one of two modes. In the normal mode, data is transferred directly from the rows (zones) of the card to corresponding bit positions in a data buffer for transfer to the bus as a 12-bit character. The bits in this output character correspond directly to zones in the card column.

The second reading mode is the compressed data mode which is compatible with the proposed expansion of the Hollerith code. In this mode, card zones 12 through 08 are transferred directly to the data buffer; however, zones 01 through 07 are encoded into a 3-bit octal representation before loading into the buffer. This encoding is possible because of the lack of double punches in zones 01 through 07 of both the present and proposed Hollerith codes. As a result of this encoding, the 12-bit data from the card column is compressed into an 8-bit character that is transferred as a low-order byte to the Unibus.

Regardless of the reading mode used, a punched hole or mark is interpreted as a binary 1 and the absence of a hole or mark is a binary 0.

2.3 CARD READER

Most available card readers operate in a characteristic manner. The reader itself consists of an input hopper for loading a number of cards, a photoelectric read station for reading data from the card, an output hopper for

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stacking the cards after reading, a motorized mechanism for moving the cards, and control logic for generating command and status signals.

Operation begins when the controller issues a read command. When the card reader receives this command, it picks the first card from the hopper and feeds it into the read station. As the data holes or marks pass through the read station, they are sensed by a photoelectric device. At the same time, the reader generates a series of index or clock marks. These marks are transmitted to the controller simultaneously with the data bits read from the holes in the card. Thus, the controller receives 12 bits of parallel data on the 12 data output lines of the card reader connector.

The card reader furnishes alarm signals to warn of any error condition present in the reader. It also provides signals for certain housekeeping functions such as hopper empty, stacker full, and unit busy.

Each reader has a control panel for manual operations of the reader and for indicating various error conditions. These controls and indicators may vary from reader to reader, depending on the type and model used.

Four program flags indicate the status of the card reader. These flags are monitored by the controller and are tied to the interrupt logic so that setting any one of these flags generates an interrupt request.

The ON-LINE flag is set whenever the ready line from the card reader goes true indicating that the card reader is ready to accept commands. This feature permits the program to perform other tasks while awaiting manual intervention to clear a card reader problem such as lack of cards in the input hopper. This flag notifies the controller when the card reader is ready to resume on-line operation under program control.

The COLUMN DONE flag requests a program interrupt when a column of information has been read and is ready to be transferred to the bus. The CARD DONE flag is set when the card leaves the read station. The controller should then immediately issue a new read command to keep the card reader operating at full rated speed. The ERROR flag indicates that an error condition is present in the card reader and an interrupt request is made so that the program can branch to an error-handling routine.

2.4 CR11 CONTROLLER

The CR11 Controller provides the command and monitoring functions for the card reader, in addition to handling data transfers from the card reader to the Unibus. When the processor addresses the bus, the controller decodes the address to determine if the card reader is the selected external device and, if selected, whether it is to perform an input or output operation. For the following discussion, refer to the simplified block diagram shown in Figure 2-1.

The address selection logic decodes the incoming address and responds to one of four possible sequential addresses. The register that is selected and the type of bus data transfer operation being performed determine whether a command is being issued, status is being monitored, or data is being read from a card in one of two reading modes.

If, for example, data is to be read, the status register is first addressed so that a read command can be sent to the card reader. The card reader moves a card into the read station, detects the data from the first card column, and loads it into the buffer register. Once the buffer is loaded, the controller sets a COLUMN READY flag so that an interrupt can be generated to transfer the data to the bus.

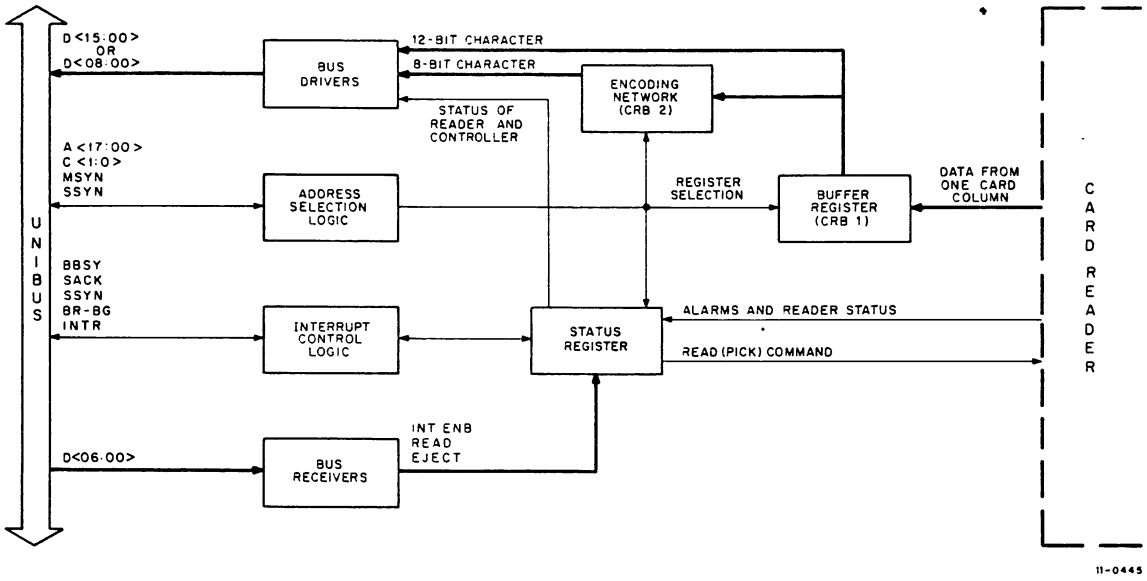


Figure 2-1 CR11 Controller – Simplified Block Diagram

At this point, either the buffer register (CRB1) or the encoding network (CRB2) would be addressed so that the data, in the form of either a 12-bit or 8-bit character, could be transferred through the bus drivers to the Unibus. When CRB1 is addressed, data from the buffer register is applied directly to the bus. When CRB2 is addressed, the 12 bits from the buffer are compressed into an 8-bit character before application to the bus.

When the status register is addressed, it can serve either as a command register to specify certain functions to be performed or as a status register to monitor operations within the controller and the card reader.

When the status register is used as a command register, it is loaded from the bus and can perform one or more of the following functions: interrupt enable, read, and eject. Interrupt enable is used to condition appropriate controller circuits so that an interrupt is initiated whenever an error occurs, the card reader goes on-line, or the reading of a card column or an entire card is completed. The read function is the only command sent to the card reader and is used to start operation of the reader. The eject function prevents the COLUMN READY flag from being set so that data from the buffer register is not transmitted to the bus. However, transfers between the card reader and the buffer register still take place. As far as the controller is concerned, the card has been ejected even though the reader continues normal operation.

When the status register is used to monitor system functions, it operates as a read-only register and its output is applied to the bus for monitoring by the program. Some of the bits in the register are set or cleared by alarm and status signals from the card reader itself; other bits are set or cleared by the controller.

Most card readers supply two status signals to the controller: READY, which indicates that the card reader is placed on-line; and BUSY or CARD IN READER (CIR), which indicates that the reader is currently processing a card. The reader normally signals an alarm simply by dropping the READY line whenever a reader error condition arises. However, in some readers, such as the Documation readers, additional alarm lines are included so that specific error signals can be sent to the controller. These alarm lines include: HOPPER CHECK (input hopper empty/output stacker full); and MOTION CHECK (card not picked or card hung up in card track).

Status and alarm signals are also generated internally by the controller. These include: ERROR, TIMING ERROR, COLUMN READY, and CARD DONE. These bits are described more fully in Chapter 4 of this manual.

CHAPTER 3
OPERATION

3.1 SCOPE

This chapter provides the information necessary for normal operation of the CR11 Card Reader System and is divided into three major parts: controls and indicators, card loading and unloading, and operating procedures. Additional procedures, such as calibration and mechanical adjustments, are beyond the scope of this manual and are covered in the appropriate card reader manual.

This chapter covers only operation of the Documation, Inc. card readers. Operating procedures for GDI card readers are described in Appendix A.

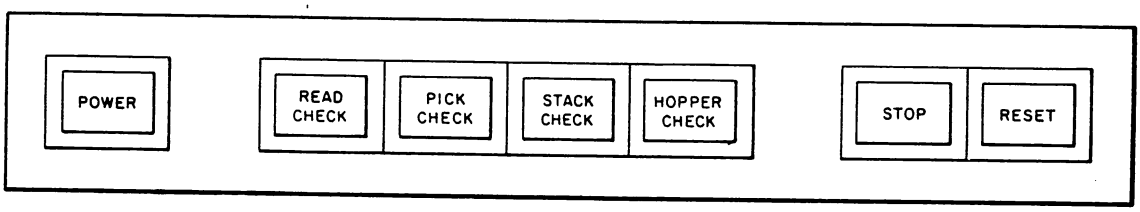
The description of the controls and indicators (Paragraph 3.2) is in tabular form and provides the user with the type and function of each operating switch and indicator on the card reader. Card handling procedures are given in Paragraph 3.3 and step-by-step operating procedures for both on-line and off-line operation are given in Paragraph 3.4.

3.2 CONTROLS AND INDICATORS

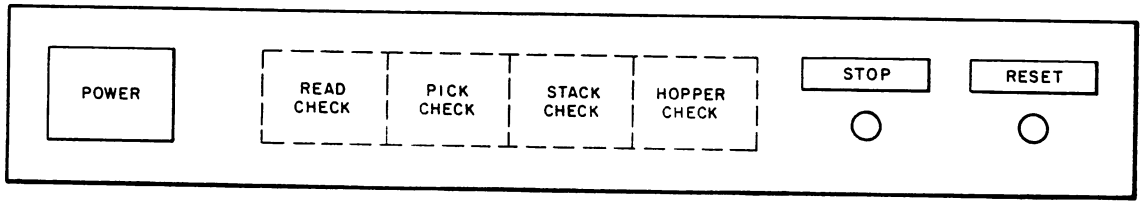
The controls and indicators used to operate the CR11 Card Reader System are shown in Figure 3-1 and listed in Tables 3-1 and 3-2. Although the front control panel is shown for both the M200/0M200 and M600 card reader models, only the M600 model is covered in the table. This particular model is described in order to provide coverage of the additional indicators. The M200/0M200 model is basically a similar version except the switches and associated indicators are mounted separately. The functions are identical with those described for the M600 model.

The items covered in each table are listed below:

Table 3-1	Front Control Panel (see Figure 3-1, a)	This control panel is located at the upper left-hand corner of the front of the reader. This panel contains the controls and indicators used for normal on-line/off-line operation of the card reader.
Table 3-2	Rear Control Panel (see Figure 3-1, c)	This panel is located at the upper right-hand corner of the back of the reader. This panel is used for initial set-up of the system and for maintenance purposes.



a. Front Control Panel (Model M600)



b. Front Control Panel (Model M200/0M200)

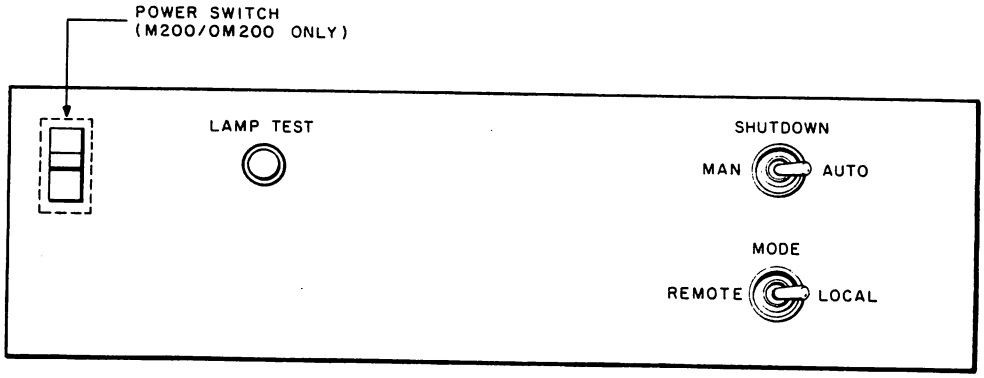


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Figure 3-1 Card Reader Controls and Indicators

Table 3-1
Front Panel Controls and Indicators

Control or Indicator	Type	Function
POWER switch	alternate-action pushbutton/indicator switch	Controls application of all power to the card reader. When indicator is off, depressing switch applies power to reader and causes associated indicator to light. When indicator is lit, depressing switch removes all power from reader and causes indicator to go out.
READ CHECK indicator	white light	When lit, this light indicates that the card just read may be torn on the leading or trailing edges, or that the card may have punches in the 0 or 81st column positions. Because READ CHECK indicates an error condition, whenever this indicator is lit, it causes the card reader to stop operation and extinguishes the RESET indicator.
PICK CHECK indicator	white light	When lit, this light indicates that the card reader failed to move a card into the read station after it received a READ COMMAND from the controller. Stops card reader operation and extinguishes RESET indicator.
STACK CHECK indicator	white light	When lit, this light indicates that the previous card was not properly seated in the output stacker and therefore may be badly mutilated. Stops card reader operation and extinguishes RESET indicator.
HOPPER CHECK indicator	white light	When lit, this light indicates that either the input hopper is empty or that the output stacker is full. In either case, the operator must manually correct the condition before card reader operation can continue.
STOP switch	momentary pushbutton/indicator switch (red light)	When depressed, immediately lights and drops the READY line, thereby extinguishing the RESET indicator. Card reader operation then stops as soon as the card currently in the read station has been read. This switch has no effect on the system power; it only stops the current operation.

(continued on next page)

Table 3-1 (Cont)
Front Panel Controls and Indicators

Control or Indicator	Type	Function
RESET switch	momentary pushbutton/indicator switch (green light)	When depressed and released, clears all error flip-flops and initializes card reader logic. Associated RESET indicator lights to indicate that the READY signal is applied to the controller. The RESET indicator goes out whenever the STOP switch is depressed or whenever an error indicator lights (READ CHECK, PICK CHECK, STACK CHECK, or HOPPER CHECK).

Table 3-2
Rear Panel Controls

Control	Type	Function
LAMP TEST switch	pushbutton	When depressed, illuminates all indicators on the front control panel to determine if any of the indicator lamps are faulty.
SHUTDOWN switch	2-position toggle	Controls automatic operation of the input hopper blower. MAN position – blower operates continuously whether or not cards are in the input hopper. AUTO position – causes the blower to shut down automatically whenever the input hopper is emptied. Blower automatically restarts when cards are loaded into the hopper and the RESET switch is depressed. Blower activates approximately three seconds after RESET is depressed.
MODE switch	2-position toggle	Permits selection of either on-line or off-line operation. LOCAL position – removes the READ COMMAND input from the controller to allow the operator to run the reader off-line by using the RESET and STOP switches on the front control panel. REMOTE position – enables the READ COMMAND input from the controller to allow normal on-line operation under program control once RESET is depressed.

3.3 CARD HANDLING PROCEDURES

The following paragraphs present the recommended procedures for loading the input hopper, unloading the output stacker, and correcting error conditions.

3.3.1 Loading Cards

The following procedure is used when loading the input hopper with punched cards to be read:

Step	Procedure
1	Pull the hopper follower back with one hand and begin loading card decks into the hopper. Make certain that the first card to be read is placed at the front with the "9" edge down, column 1 to the left.
2	Continue placing cards into the input hopper until it is loosely filled (this is the approximate amount of cards listed as the capacity for a particular card reader model).
	CAUTION **Do not pack the input hopper so full that the air from the blower cannot riffle the cards properly. If the cards are packed too tightly, it impairs proper operation of the vacuum picker.**
3	Cards may continue to be loaded while the reader is operating provided tension is maintained on the front portion of the deck as cards are added to the rear. Additional cards should not be loaded, however, until the hopper is approximately 1/2 to 1/3 full.
	CAUTION **When maintaining tension on the card deck, use just enough pressure to maintain the riffle action to prevent card damage and jamming of the reader.**
4	Normally, all cards are moved through the reader into the stacker. However, if it is necessary to remove cards from the input hopper, simply pull back the follower and remove the card deck.

3.3.2 Unloading Cards

To unload cards from the output stacker, pull the stacker follower back with one hand and remove the card deck from the stacker, being careful to maintain the order of the deck. The stacker may be unloaded while the cards are being read.

3.3.3 Correcting Error Conditions

The four error alarm indicators on the front control panel of the card reader normally indicate a condition that can be corrected by operator intervention. These alarms, their causes, and the required operator intervention are given in Table 3-3.

3.4 OPERATING PROCEDURES

The CR11 Card Reader System can be used in either a local or remote operating mode. The local (off-line) mode is controlled by switches on the front and rear panels of the card reader. The remote (on-line) mode is controlled by programmed commands from the PDP-11 System.

Table 3-3
Error Alarm Causes and Remedies

Error Indicator	Possible Cause	Corrective Action
READ CHECK	Card edges torn Punch in 0 or 81st column	Remove faulty card and restart reader If READ CHECK occurs for every card, it indicates a malfunction in the reader read logic
PICK CHECK	Damage to leading edge Torn webs Cards stapled together	Remove faulty card and restart reader If there is no evidence of card damage, check for excessive warpage of card deck and/or a buildup of ink glaze on the picker face
STACK CHECK	Jam in card track Badly mutilated card	Correct jam or remove mutilated card and restart reader
HOPPER CHECK	Input hopper empty Output stacker full	Load input hopper Unload output stacker

The following paragraphs present procedures for both off-line and on-line operation of the card reader. Although procedures are given for setting up on-line operation, it is beyond the scope of this chapter to present any programming details. Programming information is covered in Chapter 4.

3.4.1 Off-Line Operation

Off-line operation of the card reader is used primarily for setting up and checking reader operation prior to switching to on-line use; for correcting error conditions; and for maintenance tests. When placed off-line, the reader can be operated locally from the control panels. The following procedure is used to energize the reader and check off-line operation prior to switching to on-line operation.

Step	Procedure
1	Make certain that the ac power cord is plugged in and that the circuit breaker on the rear base panel of the reader is in the ON position.
2	Set MODE switch to LOCAL position.
3	Set SHUTDOWN switch to AUTO position.
4	Depress POWER switch to energize reader. Note that POWER indicator lights but blower does not come on.
5	Depress LAMP TEST switch and observe that all front panel indicators are lit.
6	Load a card deck into the input hopper.
7	Depress RESET switch and observe that associated green indicator comes on. After approximately 3 seconds, cards should start being picked and moved through the read station into the output stacker.
8	When the input hopper is empty, observe that the HOPPER CHECK indicator lights, the green RESET indicator goes out, and the red STOP indicator lights.
9	The card reader may now be operated locally or switched to on-line operation.

3.4.2 On-Line Operation

The following procedure is used to place the CR11 Card Reader System on-line. When placed on-line, the system is controlled by programmed commands from the PDP-11 System.

Step	Procedure
1	Make certain that the card reader is operational by performing the procedure given in Paragraph 3.4.1.
2	Make certain the output stacker is empty. Load the input hopper with the cards to be read.
3	Set the MODE switch to REMOTE.
4	Depress the RESET switch and observe that the associated green indicator lights. The system is now on-line.
5	If the system goes off-line because of an error alarm, it can be placed back on-line by correcting the error and then depressing the RESET switch.
	Any time it is desired to go off-line, depress the STOP switch.

CHAPTER 4
PROGRAMMING INFORMATION

4.1 SCOPE

This chapter presents general programming information for software control of the CR11 Card Reader System. Although a typical program example is included, it is beyond the scope of this manual to provide detailed programs. For more detailed information on programming in general, refer to the *Paper Tape Software Programming Handbook*, DEC-11-GGPB-D.

This chapter is divided into three major portions: device registers, interrupts, and program example.

4.2 DEVICE REGISTERS

All software control of the CR11 Card Reader System is performed by two device registers within the controller. Although there are only two registers, three addresses have been assigned. The data buffer register, which holds one column of data from a card, can be addressed as a normal 12-bit register (compatible with standard Hollerith code) or it can be addressed so that the output passes through an encoding network to provide an 8-bit output (compressed Hollerith code).

The device registers and associated addresses are listed in Table 4-1. Note that these addresses can be changed by altering the jumpers on the address selection logic. However, any DEC programs or other software referring to these addresses must also be modified accordingly if the jumpers are changed.

Table 4-1
Standard Device Register Assignments

Register	Mnemonic	Address
Status Register	CRS	777160
Data Buffer Register	CRB1	777162
Data Buffer Register	CRB2	777164

NOTES:
1. CRB1 is the actual register that holds one column of data from a card (Hollerith code).
2. CRB2 is the gated output of CRB1 such that the 12-bit buffer output is compressed into an 8-bit character (compressed Hollerith code).
3. The data buffer register is a read-only register. It cannot be loaded by the program.

Depending on the specific card reader used, bits 12 and 13 in the status register may or may not be used. If they are not used, corresponding jumpers on the M8290 module should be removed. A list of card readers supplying signals for these bits is given in Appendix B.

Figures 4-1 through 4-3 show the bit assignments for the three register addresses. "Unused" bits are always read as 0s. Loading "unused" or "read only" bits has no effect on the bit position. No data can be loaded into the high-order byte; therefore, use only word or low-byte addressing for writing into the status register.

The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following: issuing a programmed RESET instruction; depressing the START switch on the processor console; or occurrence of a power up or power down condition of the processor power supply.

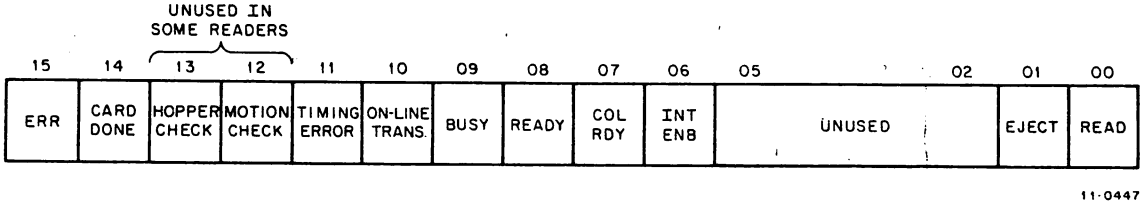


Figure 4-1 Status Register Bit Assignments

Bit		Meaning and Operation
15	ERROR	Used to indicate an error condition is present. This bit is set (indicating an error) whenever an internal error flip-flop is set. This flip-flop is set when either one of the following conditions occurs: *a.* The card reader goes off-line from an on-line condition. During normal operation, this occurs when a card reader check or supply error is sensed. *b.* A timing error is present when the reader completes reading of the card (card done). If an attempt is made to read a card while the error flip-flop is set and the error-causing conditions have not been corrected, the flip-flop remains set and subsequent read commands are ignored. This bit is connected to the interrupt logic so that the program can branch to an error handling routine. Read-only bit. Cleared by INIT. **NOTE** **With the error removed, bits 15, 14, 11, and 10 are automatically cleared when the status register is loaded. However, if using a DATOB for loading, the low-order byte must be used because the high-order byte has no effect on the status register.**

(continued on next page)

Bit		Meaning and Operation
14	CARD DONE	When set, indicates that one card has passed through the read station and the next card may be requested from the input hopper. This bit is connected to the interrupt logic. Read-only bit. Cleared by INIT or by loading the status register.
13	HOPPER CHECK	When set, this bit indicates that either the input hopper is empty or the output stacker is full. In either case, the condition must be corrected before further operation can take place. Only certain card readers provide this error signal. If a card reader is used that *does not* supply this signal, then the jumper to this bit in the status register must be removed. This bit is then always read as 0. A list of card readers supplying this signal is given in Appendix B. Read-only bit. Cleared by correcting error-causing condition.
12	MOTION CHECK	When set, this bit indicates the presence of an abnormal condition in the card reader. Any one of the following three conditions sets this bit: *a.* **Feed Error** – Indicates that card reader feed mechanisms failed to deliver a card to the read station when demanded. *b.* **Motion Error** – Indicates a card jam in the card reader. *c.* **Stack Fail** – Indicates that card has not been delivered to the output stacker. This bit is similar to bit 13 in that only certain card readers provide this signal. If a reader is used that *does not* supply this signal, the associated status register jumper must be removed. This bit is then always read as 0. A list of card readers supplying this signal is given in Appendix B. Read-only bit. Cleared by correcting error-causing condition.
11	TIMING ERROR	When set, this bit indicates that a new column of data has been loaded into the data buffer before a previously loaded column was read by the program. Clears COLUMN READY bit and causes ERROR bit to be indicated at CARD DONE time. Once the timing error bit is set, the COLUMN READY bit is inhibited from setting and no data transfers can take place until TIMING ERROR is cleared.

(continued on next page)

Bit		Meaning and Operation
11 (cont)	TIMING ERROR (cont)	When the EJECT bit is set, it prevents TIMING ERROR from setting because a timing error is not pertinent if the card is ejected. Read-only bit. Cleared by INIT or by loading the status register.
10	READER TRANSITION TO ON-LINE	When set, this bit indicates that the card reader has gone on-line and is now under program control. Depressing the card reader RESET switch brings the reader on-line, provided no error conditions exist. The card reader goes off-line whenever an error condition is sensed or the STOP switch is depressed. When the reader goes from on-line to off-line, the ERROR bit is set. This bit is connected to the interrupt logic so that the program can identify card reader availability. Read-only bit. Cleared by INIT or by loading the status register.
09	BUSY	When set, indicates that a card is in the process of being read. Read-only bit. Cleared when card is not in the read station or when the read command is removed.
08	READER READY STATUS	When set, this bit indicates that the reader is off-line. When clear, indicates that the reader is on-line and ready to accept read commands. Read-only bit.
07	COLUMN READY	When set, indicates that one column of data has been loaded into the data buffer and is ready for transfer to the bus. When this bit is set and a card is ejected, a timing error can still occur is the bit remains set when new data arrives at the data buffer. If a card is ejected or a timing error occurs before COLUMN READY bit is set, COLUMN READY is inhibited from setting. COLUMN READY is cleared when the data buffer is addressed (either CRB1 or CRB2). Note that this operation does not affect the contents of the data buffer but does clear the COLUMN READY bit. This bit is also connected to the interrupt logic so that a data transfer can take place once the data has been assembled in the buffer. Read-only bit. Cleared by INIT or by addressing the data buffer.

(continued on next page)

Bit		Meaning and Operation
06	INTERRUPT ENABLE	When set, allows an interrupt to occur provided one of the following bits is also set: ERROR (bit 15), CARD DONE (bit 14), TRANSITION TO ON-LINE (bit 10), or COLUMN READY (bit 07). Read/write bit. Cleared by INIT.
05–02	UNUSED	
01	EJECT	When set, this bit prevents the COLUMN READY flag from being set. However, data transfers between the card reader and the data buffer still take place. Although the remaining card columns are actually read by the card reader, absence of COLUMN READY flags make it seem to the controller that the card has been ejected from the read station. When EJECT is set, it also prevents the TIMING ERROR bit from being set because a timing error is not relevant if the card is ejected. Note that setting EJECT alone does not eject the card. The READ bit must also be set to fetch this card. Read/write bit. Cleared by INIT.
00	READ	When set, this bit causes the card reader feed mechanism to deliver one card to the read station for reading. This bit is always read as a 0. Cleared by INIT or by loading with a 0. This bit can be loaded by the program; it can also be read but is always read as a 0 whether set or cleared.

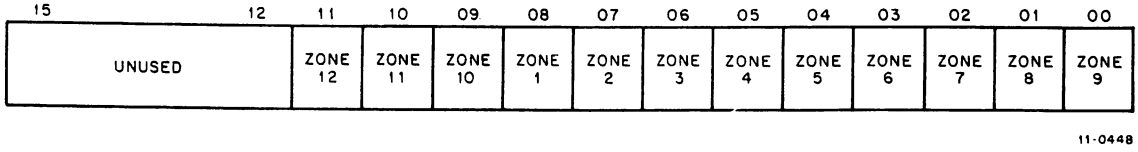


Figure 4-2 Data Buffer Register Bit Assignments (CRB1)

Bit		Meaning and Operation
15–12	UNUSED	
11–00	ZONES	These bits represent the output of a 12-bit data buffer register. During a read operation, data from a card is loaded into this buffer one column at a time. After each column is loaded, the contents of the buffer is placed on the Unibus for transfer to the processor or other bus device on demand. When the data buffer register is addressed as CRB1, the contents of the buffer is coupled to the 12 least-significant bus data lines as follows:

(continued on next page)

Bit		Meaning and Operation
11–00 (cont)	ZONES (cont)	

Bit	Corresponding Card Image
11	ZONE 12
10	ZONE 11
09–00	ZONES 10, 1–9, respectively

All bits are read-only bits.

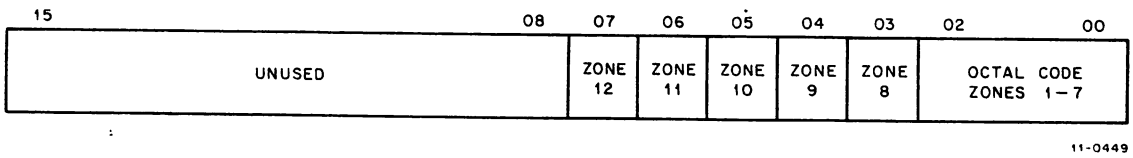


Figure 4-3 Data Buffer Register Bit Assignments (CRB2)

Bit		Meaning and Operation
15–08	UNUSED	
07–00	ZONES	These bits represent the output of a 12-bit data buffer register. During a read operation, data from a card is loaded into this buffer one column at a time. After each column is loaded, the contents of the 12-bit buffer are compressed into an 8-bit character by an encoding network and are then gated onto the Unibus as a low-order byte. This data compression is made available so that the card reader controller is fully compatible with the proposed expansion of the Hollerith code.

Bits 07 through 03 are encoded as follows:

Bit	Corresponding Card Image
07	ZONE 12
06	ZONE 11
05	ZONE 10
04	ZONE 09
03	ZONE 08

Bits 02 through 01 represent an octal code that defines the card zone as shown below. In the case of multiple zones, these bits are the inclusive OR of the octal codes of the zones.

Bit 02	Bit 01	Bit 00	Card Zone
0	0	0	zero, ZONES 1–7
0	0	1	ZONE 1
0	1	0	ZONE 2
0	1	1	ZONE 3
1	0	0	ZONE 4
1	0	1	ZONE 5
1	1	0	ZONE 6
1	1	1	ZONE 7

All bits are read-only bits.

4.3 INTERRUPTS

The CR11 Controller uses BR interrupts to gain control of the bus to perform a vectored interrupt, thereby causing a branch to a handling routine.

A BR interrupt can occur only if the interrupt enable (INT ENB) bit in the status register is set. When INT ENB is set, an interrupt request is generated whenever any one of the following bits in the status register is set: ERROR, CARD DONE, TRANSITION TO ON-LINE, or COLUMN READY.

When the ERROR bit is set, it indicates that some type of error condition exists. In this case, an interrupt is used to cause a program branch to an error handling routine.

When CARD DONE, TRANSITION TO ON-LINE, or COLUMN READY is set, it indicates that the controller is ready to perform a data transfer or accept a command. In these cases, an interrupt service routine is used to perform the desired bus cycle.

The interrupt priority level is 6 and the interrupt vector address is 230. Note that the priority level can be changed with a priority plug and the vector address can be changed by jumpers in the interrupt control logic. However, any DEC programs or other software referring to that level or address *must* also be changed if the priority plug or vector address is changed.

4.4 PROGRAM EXAMPLE

The following example shows a typical method of programming the CR11 Card Reader System. In this example, the card reader is used to read a bootstrap loader program from punched cards and load the program into core memory.

```
        177160                      CRS=177160          ;card reader status register
        177162                      CRB1=177162         ;12-bit data buffer
        1000                        .=1000              ;starting address for memory

        000001                      R1=%1
        000002                      R2=%2
        000003                      R3=%3
        000004                      R4=%4

1000    012701  177160  START:      MOV   #CRS, R1      ;set up address of CRS in R1
        012703  177162              MOV   #CRB1, R3     ;add data buffer address in R3

        031127  001400  RTST:       BIT   @R1, #1400    ;is reader on-line?
        001375                      BNE   RTST          ;no, so may as well wait.

        005211          RDCD:       INC   @R1           ;O.K., read a card

        031127  140000  RCHK:       BIT   @R1, #140000  ;special condition or card done
                                                         set?
        003374                      BGT   RDCD          ;special condition off but card
                                                         done on.
        001402                      BEQ   GOGO          ;both off

        000005          END:        RESET               ;special condition on, assume
        000112                      JMP   @R2           ;hopper empty and branch to
                                                         program
```

(continued on next page)

```
105711          GOGO:   TSTB    @R1             ;column ready?
100370                  BPL     RCHK            ;no, keep looking.
031327  000400          BIT     @R3,    #400    ;row 1 in this byte?
001404                  BEQ     GO2             ;no, must be data
111302                  MOVB    @R3,    R2      ;yes, is first address byte
000302                  SWAB    R2              ;move to high-order byte
010104                  MOV     R1,     R4      ;and set second-add.-byte flag
000761                  BR      RCHK            ;and get next column

010404          GO2:    MOV     R4,     R4      ;test second-add.-byte flags
001002                  BNE     GO3             ;if on, use this for add. byte
111322                  MOVB    @R3,    (R2)+   ;otherwise, store it in memory
000755                  BR      RCHK            ;and get next byte.

061302          GO3:    ADD     @R3,    R2      ;complete address makeup
005004                  CLR     R4              ;reset second-add.-byte flag
000752                  BR      RCHK            ;and go around

000001                  .END
```

CHAPTER 5
THEORY OF OPERATION

5.1 INTRODUCTION

This chapter provides a detailed description of the CR11 Card Reader Controller. The controller may be divided into five major functional areas: selection logic, interrupt logic, status register, data buffer, and compressed data logic. Each of these areas is covered separately in subsequent paragraphs. The purpose of each of these functional areas is as follows:

Selection Logic	Determines if the card reader has been selected for use, which register is to be used, and what type of transfer (DATI or DATO) is to be performed.
Interrupt Logic	Permits the controller to gain bus control and perform a program interrupt. Priority level of bus request (BR) line may be changed by user. Consists of interrupt control logic and the interrupt enable bit in the status register.
Status Register	A 16-bit register used to monitor operation of the controller and card reader; also used to provide certain commands for the card reader.
Data Buffer	Assembles data from one card column for parallel transmission to the bus. The 12-bit register corresponds to the 12 zones comprising a card column character.
Compressed Data Logic	An encoding network that converts the 12-bit output of the data buffer into an 8-bit character that is transferred as a low-order byte.

Earlier versions of the CR11 Controller consisted of three separate logic modules. This new version consists of a single quad type module. The 4015 IC circuit, which is shown on the print set as a single block, functionally can be used as four separate flip-flops or as a 4-bit register. For purposes of clarity, Appendix D of this manual includes circuit diagrams, a functional schematic, package diagram, and a truth table for this IC circuit.

5.2 ADDRESS SELECTION

The address selection logic (drawing CR-4) decodes the address information from the bus and provides three select line and two gating signals that determine which register has been selected and whether it is to perform an input or output function. Jumpers are arranged on the logic so that the module responds only to standard device register addresses 777160, 777162, 777164, and 777166 (jumpers in bit positions 3, 7, and 8). Although these addresses have been selected by DEC as the standard assignments for the CR11 Card Reader Controller, the user may change the jumpers to any address desired. However, any MainDEC program (or other software) that references the CR11 standard address assignments must be modified if other than the standard assignments are used.

The first five digits of the address (77716) indicate that the CR11 has been selected as the device to be used. The final digit, consisting of address lines A02, A01, and A00, determines which register has been selected and whether a word or byte operation is to be performed. The two mode control lines, C00 and C01, determine whether the selected register is to perform an input or output operation.

Address lines A02 and A01 are decoded to produce one of four select line signals (refer to Table 5-1) which select the register to be used. The two mode control lines produce IN and OUT gating signals (Table 5-1) which determine whether the bus cycle is a DATI or DATO. Note that an IN gating signal is provided for all three registers because all three can be read from the bus. However, an OUT gating signal is used only with the status register because it is the only register that can be loaded from the bus.

Table 5-1
Gating and Select Line Signals

Select Line	Gating Signal	Function Selected	Reg.	Bus Cycle
0	IN	Status to bus	CRS	DATI
2	IN	Data to bus	CRB1	DATI
4	IN	Compressed data to bus	CRB2	DATI
0	OUT	Bus to status	CRS	DATO or DATOB
6	IN or OUT	Unused	---	DATI, DATO, or DATOB

5.2.1 Inputs

A simplified block diagram of the address selection logic is shown in Figure 5-1. Note that IN and OUT are always used with respect to the master (controlling) device. Thus, when the card reader controller is used, an OUT transfer is a transfer of data out of the master (the processor) and into the device. Likewise, an IN transfer is the operation of the controller furnishing data to the processor.

The address selection logic input signals consist of 18 address lines, A ⟨17:00⟩; 2 bus control lines, C ⟨1:0⟩; and a master synchronization (MSYN) line. The address selection logic decodes the incoming address as described below. This address format is shown in Figure 5-2. Note that all input gates are standard bus receivers.

a. Line A00 is used for byte control.

b. Lines A01 and A02 are decoded to select one of the four addressable device registers.

c. Decoding of lines A ⟨12:03⟩ is determined by jumpers. When a given line contains a jumper, the address logic searches for a 0 on that line. If there is no jumper, the logic searches for a 1.

NOTE
Connection of jumpers on the quad module is identical to the method used on earlier versions of this device which employed an M105 Address Selector Module.

d. Address lines A ⟨17:13⟩ must be all 1s. This specifies an address within the top 4K byte address bounds for device registers.

NOTE
Pin EA1 (EXT. GND) must be grounded by the user to ensure proper operation of the address selection logic.

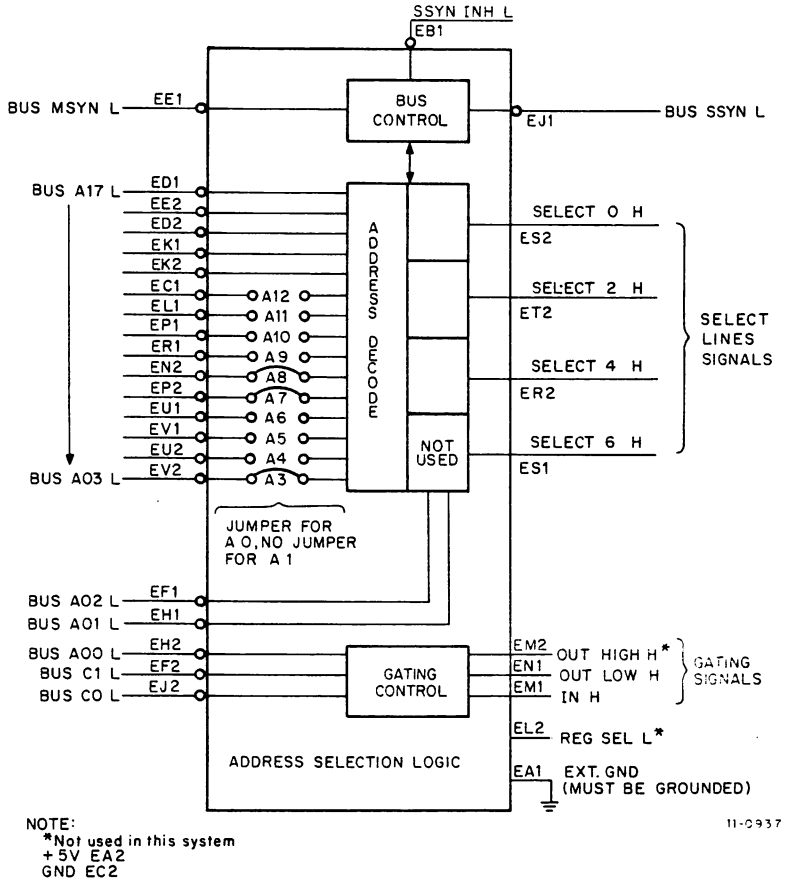


Figure 5-1 Address Selection Logic – Simplified Diagram

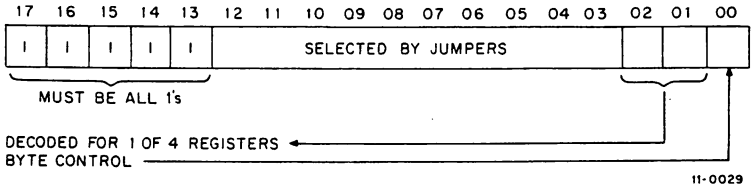


Figure 5-2 Controller Select Address Format

5.2.2 Outputs

The address selection logic output signals that are used in the CR11 permit selection of three 16-bit registers and provide two signals used for gating information to and out of the master device. All of the output signals are listed in Table 5-1. Note, however, that only two gating signals are used (IN AND OUT LOW). Actually, there are two OUT signals, OUT LOW and OUT HIGH. The logic diagram (drawing CR-4) shows an additional select line signal, SELECT 6. This particular signal is not used by the CR11 Controller but the controller responds to that address.

Tables 5-2 and 5-3 indicate the input signals that select the control output line states.

Table 5-2
Select Lines

Input Lines A ⟨02:01⟩	Select Lines True (+3V)
00	0
01	2
10	4
11	6*

NOTES: 1. Lines A ⟨17:13⟩ must be all 1s (0V on Unibus).
2. Lines A ⟨12:03⟩ are selected by jumpers.
* Not used on CR11.

Table 5-3
Gating Control Signals

Mode Control C ⟨1:0⟩	Byte Control A00	Gating Control Signals True (+3V)	Bus Sequence
00	0	IN	DATI
00	1	IN	DATI
01	0	IN	DATIP
01	1	IN	DATIP
10	0	OUT LOW OUT HIGH*	DATO
10	1	OUT LOW OUT HIGH*	DATO
11	0	OUT LOW	DATOB
11	1	OUT HIGH*	DATOB

NOTE: 1. Gating control signals may become true although select lines are not.
* Not used on CR11.

5.2.3 Slave Sync (SSYN)

When SSYN INH is grounded, it inhibits the acknowledgment signal (SSYN) normally generated by the address selection logic.

5.3 INTERRUPT CONTROL

The interrupt control logic (drawing CR-4) permits the CR11 Controller to gain control of the bus (become bus master) and perform an interrupt operation. The jumpers on this logic are arranged so that the logic has a normal vector address of 230 (jumpers in bit positions 3, 4, and 7). Although this is the recommended vector address, the user may change the jumpers to correspond to any address desired, but MainDEC programs and other software reference the standard vector address assignment of 230.

NOTE
Connection of jumpers on the quad module is the reverse of the method used on M782 and M7820 Interrupt Control Modules and the same as the M7821 module. On this module, a jumper represents a 1; no jumper represents a 0.

The interrupt control logic consists of a dual input request and grant acknowledge circuit for establishing bus control. The interrupt occurs at vector address 230 rather than 234 because vector bit 2 is used only with the disabled B input portion of the logic. The master control B portion of the logic is disabled because neither an INT B or INT ENB B can be generated by the controller logic. (These two input lines are grounded as shown on drawing CR-3.)

Before the interrupt control logic can generate an interrupt request, two input signals must be high: INT A and INT ENB A. The logic that generates these two signals is shown on drawing CR-3. When a 1 is loaded into bit 06 of the status register, it sets the INT ENB bit to produce INT ENB A H. This signal is applied to the interrupt control logic as an enabling signal.

The second signal that must be present to generate an interrupt is INT A H. The INT A H signal is produced by three OR gates and is true if any one of the following conditions exist: ERROR, CARD DONE, ON-LINE, or COLUMN READY. Each of these conditions is described separately in Paragraphs 5.4.1, 5.4.2, 5.4.6, and 5.4.9, respectively.

The master control section of the interrupt logic (see Figure 5-3) is used to gain control of the bus. When both the INT A and INT ENB A requesting inputs are asserted, a bus request is made on the BR level corresponding to the level of the priority plug in the logic. The standard level for the CR11 Controller is BR6 but this may be changed by the priority plug, if desired. When the priority arbitration logic in the processor recognizes the request and issues a bus grant signal, the master control circuit acknowledges with a SACK signal. When the controller has fulfilled all requirements to become bus master (BBSY false, SSYN false, and BG false), the master control section asserts BBSY.

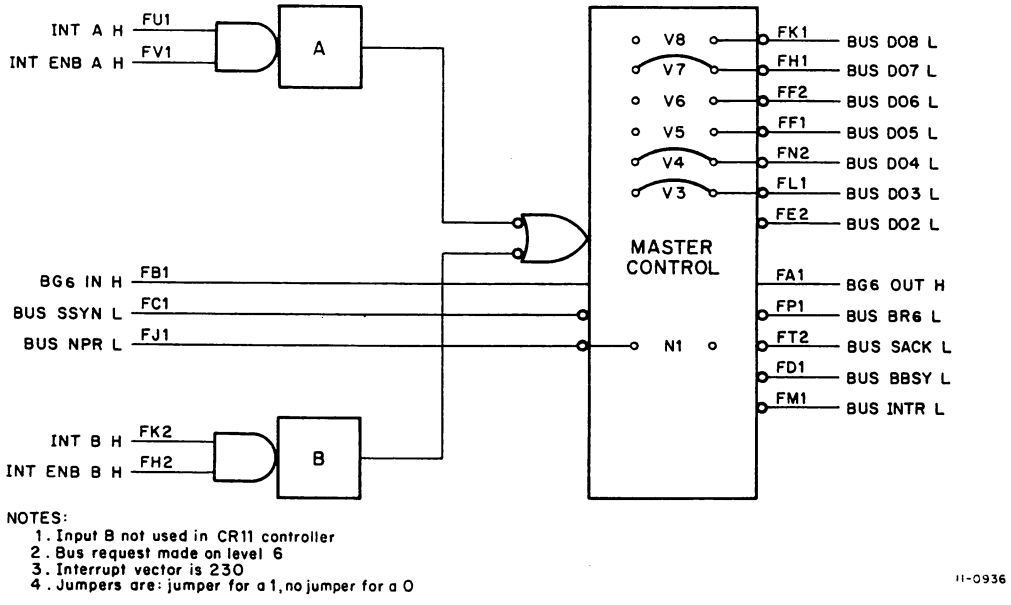


Figure 5-3 Interrupt Control Logic – Simplified Diagram

Once the controller has gained bus control by means of a BR request, an interrupt is generated. The interrupt vector address is selected by jumpers on the logic as shown on Figure 5-3. Because the vector is a 2-word (4-byte) block, it is not necessary to assert the state of bits 0 and 1. The six selectable lines determine the vector address. The least significant line is controlled by the V2 flip-flop. An interrupt on Channel A causes a vector at location

230 and an interrupt on Channel B would cause a vector at location 234. However, Channel B is not used by the CR11 Controller so the vector address is always 230.

The BG IN signal is allowed to pass through the logic to BUS BG OUT when the controller is not issuing a request. To request bus use, the AND condition of INT A and INT ENB A must be satisfied. These levels must be true until the interrupt service routine clears INT A or INT ENB A. Once bus control has been attained, it is released when the processor has strobed in the interrupt vector. After releasing bus control, the logic inhibits further bus requests even if INT A and INT ENB A remain asserted. In order to make another bus request, INT A or INT ENB A must be dropped and then reasserted to cause the logic to reassert the request line. This prevents multiple interrupts when the control logic is used to generate interrupts. Note that the interrupt control logic used in the CR11 Controller is not capable of issuing NPR requests.

In order to improve NPR latency, the NPR line is sampled and prevents an interrupt request until all NPRs have been honored. The sampling of the NPR line is controlled by a jumper (N1) on the controller module.

CAUTION

Only certain PDP-11 processors can work with the special circuit described above. The jumper (N1) on the module, when cut, prevents the special circuit from working.

5.4 STATUS REGISTER

The status register is used to monitor operation of both the card reader and controller and to provide commands to the card reader. The status register is a 16-bit register, of which four bits are not used. The following paragraphs describe the circuit logic for each bit in the register. The status register logic is shown on drawing CR-3.

Four of the status register bits (bits 15, 14, 10, and 06) function as individual flip-flops but are physically all on a single 4015 IC chip. In subsequent discussions, each bit is referred to as a single flip-flop; however, on the logic drawing (CR-3) they are shown as a 4015 IC. Therefore, Table 5-4 lists these bits and indicates the appropriate flip-flop inputs on the IC. Schematics of the 4015 IC itself are given in Appendix D.

Table 5-4
Status Register Bits on 4015 IC

Name	Bit	Data Input	Clock Input	Direct Set Input	Direct Clear Input	Output
ERROR	15	D3	CLK	SET 3	CLR	R3 (1)
CARD DONE	14	D2	CLK	SET 2	CLR	R2 (1)
INT ENB	06	D1	CLK	SET 1	CLR	R1 (1)
RDR TRANS TO ON-LINE	10	D0	CLK	SET 0	CLR	R0 (1)

5.4.1 ERROR (Bit 15)

This bit is used to indicate that an error condition is present. There are two conditions that cause an error indication: dropping of the card reader READY flag, or presence of a timing error when the reader completes the reading of a card.

The first condition occurs whenever the card reader goes off-line from an on-line condition; in other words, whenever the reader READY flag drops. This error is controlled by an ERROR flip-flop that not only signals an error but also contains an interlock circuit to prevent loading a new command until the error condition is corrected.

When the card reader is on-line and in the process of reading a card, the ERROR flip-flop is normally clear. If, however, the card reader READY line goes false (READY H goes low), then this transition direct sets the ERROR flip-flop. At the same time, the READ flip-flop is held cleared. The output of the ERROR flip-flop passes through an inverter and an OR gate and places a logic 1 on bus data line 15 to indicate an error condition when read by the program.

As an example of the operation of the error interlock circuits, assume that the ERROR flip-flop has been set by an error condition, that the ERROR bit has been read but the error *has not* been corrected by manual intervention at the card reader, and that the program is now attempting to load another READ command into the status register.

When a READ command is issued, a 1 is placed on bus data line 00 which qualifies one leg of a 2-input gate connected to the ERROR flip-flop. The other leg is qualified because the reader READY flag is still down because the error has not been corrected. The output of this gate prevents the clock input from clearing the ERROR flip-flop under these conditions.

Although absence of a READY flag provides a direct clear input to the READ flip-flop, thereby preventing any commands from being transmitted to the reader while the flag is down, the interlock circuit is used to inform the program that an error exists. This is necessary because the program is not able to read the state of the READ flip-flop.

The second condition that can cause an error indication is the presence of a timing error when the reader completes the reading of a card. In this case, the presence of a timing error causes the TIMING ERROR flip-flop to be set and its output is applied to one leg of a 2-input NAND gate. The other leg of the NAND gate is qualified by the output of the CARD DONE flip-flop, which is set when the reading of a card is complete. The output of this NAND gate is applied through an OR gate to bus data line 15 to indicate an error condition exists.

5.4.2 CARD DONE (Bit 14)

This bit is used to indicate that the reading of one card is complete and that the next card may be requested from the input hopper. The card reader logic indicates card reading complete by dropping the signal used to indicate the reader is in the process of reading a card. Although this method is used by all card readers, the actual signal name is different, depending on the type of reader used. In Documation readers, the appropriate signal is BUSY; in GDI readers, the signal is CIR (card in reader).

The card reader indicates that card reading is complete by dropping the BUSY (or CIR) signal. This causes the output of an AND gate in the controller to go high and qualify one leg of a subsequent AND gate. The other leg of this gate is qualified as long as the READ flip-flop is clear. With these two input conditions satisfied, the second AND gate produces a pulsed signal which direct sets the CARD DONE flip-flop.

The output of the CARD DONE flip-flop is tied to bus data line 14 and to an AND gate in the error logic (refer to Paragraph 5.4.1). The flip-flop output is also applied to the interrupt logic OR gates which produce the INT A H signal so that the interrupt control logic can initiate an interrupt request, provided the INT ENB A bit is also set. The purpose of this interrupt request is to allow the controller to issue a new read command so that a new card can be moved from the input hopper into the read station.

5.4.3 SUPPLY ERROR (Bit 13)

This bit is used to indicate that either the input hopper is empty or the output stacker is full. In either case, manual intervention is required by the operator before card reader operation can continue. The logic signal required for this indication is only supplied by certain card reader models, for example, the DOC 0M200. Therefore, a jumper is included in this bit position of the controller. This jumper *must be removed* when using any card reader not supplying a HOPPER CHECK signal. With the jumper removed, this bit position is always read as 0.

If this bit is used, the card reader logic produces a SUPPLY ERROR signal whenever the hopper is empty or the stacker is full. This signal passes through an inverter in the controller and qualifies an AND gate to produce a 1 in bus data line 13. The logic used to determine if the hopper is empty or the stacker is full is part of the card reader logic circuits; a description of this logic is beyond the scope of this manual.

5.4.4 CARD READER CHECK (Bit 12)

This bit is used to indicate that one of three abnormal conditions exists in the card reader. The logic signals required for this indication are only supplied by certain card reader models, for example, the DOC 0M200. Therefore, a jumper is included in this bit position of the controller. This jumper must be removed when using any card reader not supplying the appropriate signals. With the jumper removed, this bit position is always read as 0.

If this bit is used, and if any one of four signals from the card reader is a 1, it passes through an OR gate to produce a 1 on bus data line 12. A 1 in this bit position indicates a problem in the card reader. The three signals that may be present are:

a.	feed error	failure of the feed mechanism to deliver a card to the read station
b.	motion error	card jam
c.	stack fail	card not delivered to output stacker

5.4.5 TIMING ERROR (Bit 11)

This bit is used to indicate a timing error that is the result of loading data into the data buffer before the previously loaded column in the buffer is referenced by the program.

During normal operation, the card reader generates an INDEX MARKER signal when one complete column of data has been read. This signal is ANDed with the clear side of the TIMING ERROR flip-flop to produce a STROBE H signal (see drawing CR-2). This STROBE H signal is used as a clock for the COLUMN READY flip-flop. Because the two inputs to this flip-flop are both high (EJECT and TIMING ERROR are clear), the clock pulse sets the COLUMN READY flip-flop to indicate card column reading is complete. Although this causes a high to both inputs of the TIMING ERROR flip-flop, it cannot be set until the next STROBE H pulse occurs. However, before the next STROBE H appears, reading the data registers clears the COLUMN READY flip-flop, removing the high inputs to the TIMING ERROR flip-flop. Clearing the COLUMN READY flip-flop during reading is accomplished by an OR gate connected to the direct clear side of the flip-flop. This OR gate is qualified by either SELECT 2 or SELECT 4, which are true only when the data buffer or data buffer encoding network is addressed for reading.

Assume now that the COLUMN READY flip-flop is set but the data buffer register is not read by the program. When the card reader reads the next column and generates the INDEX MARKER signal, another STROBE H signal is produced. In this instance, however, it does set the TIMING ERROR flip-flop because the other two inputs are still high due to the fact that COLUMN READY was not cleared by reading and is, therefore, still set.

Once the TIMING ERROR flip-flop is set, the COLUMN READY flip-flop is inhibited from setting. When TIMING ERROR is set, the STROBE H clock pulse can no longer be generated because of the AND gate that uses TIMING ERROR (0) H as one of its inputs. Therefore, no further data transfers can take place until the TIMING ERROR flip-flop is cleared. The flip-flop can be cleared by BUS INIT or by loading the status register which produces the clearing signal LOAD STATUS H (SELECT 0 H and OUT LOW H).

If an EJECT command is issued by the controller, it prevents the COLUMN READY flip-flop from setting, which in turn prevents the TIMING ERROR flip-flop from setting. This is done because when a card is ejected, it is not necessary to read any further columns. The program simply waits for a CARD DONE signal and then issues a new READ command. The EJECT flip-flop is set by loading a 1 into bus data line 01. When set, the 0 side of the flip-flop goes low, holding one input of the COLUMN READY flip-flop low so that it cannot be set. The TIMING ERROR flip-flop cannot be set because it requires a high signal from the 1 side of COLUMN READY.

5.4.6 READER TRANSITION TO ON-LINE (Bit 10)

When set, this bit indicates that the card reader has gone on-line and is now under program control. When the READ START switch (GDI card readers) or RESET switch (Documation card readers) is depressed, the card reader goes on-line and produces a READY H signal to the controller. This signal transition is applied to the direct set input of the ON-LINE flip-flop, thereby setting it.

The output of the ON-LINE flip-flop places a logic 1 on the bus data line 10 driver and is also applied to the interrupt OR gates to produce the INT A H signal. The controller can now issue an interrupt request (provided INT ENB A is set).

If the card reader goes off-line at any time, the READY H line drops and the gating logic produces a pulsed signal that direct sets the ERROR flip-flop.

5.4.7 BUSY (Bit 09)

This bit, when set, indicates that a card is in the process of being read by the card reader. This bit position is controlled by an OR gate that is qualified by either one of two conditions: CIR (card in reader) or READ. Two conditions are necessary because READ is true only while the card is being picked from the hopper and delivered to the read station and CIR is true while the card is being read. Therefore, by using an OR gate for these two conditions, the BUSY bit is a 1 from the time the READ command is issued by the controller until the time card reading is complete, as indicated by the CARD DONE flag.

When the controller issues a READ command, it sets the READ flip-flop. When this flip-flop is set, the 0 side goes low and qualifies the OR gate which places a logic 1 on bus data line 09. When the card reader receives the READ command, it picks a card, delivers it to the read station, and issues either a CIR signal (GDI card readers) or a BUSY signal (Documation card readers). The CIR (or BUSY) signal is applied to an AND gate. The output of this gate qualifies the OR gate to retain the logic 1 on bus data line 09 and the occurrence of the first INDEX MARKER clears the READ flip-flop through an OR gate. The logic 1 remains on the bus data line driver until card reading is complete, at which time the reader drops CIR (or BUSY). Dropping CIR causes the data line driver input to return to 0, indicating that the card reader is no longer busy.

5.4.8 READER READY STATUS (Bit 08)

This bit, when set, indicates that the reader is off-line; when clear, it indicates that the card reader is on-line and able to accept commands from the controller.

This bit position is controlled by the READY line from the card reader. Whenever the READY H signal from the card reader is true, a controller gate disqualifies the bus driver, causing a logic 0 to be placed on bus data line 08. If the READY H line drops, the input AND gate is not qualified, the driver is qualified, and a logic 1 is placed on the bus data line driver.

Certain conditions within the card reader must be present before the READY H signal can be true. These conditions are:

a. Power applied and required run-up time completed.

b. Input hopper has been loaded.

c. No error or abnormal conditions exist.

d. The RESET switch (Documation readers) or the READ START switch (GDI readers) has been depressed.

5.4.9 COLUMN READY (Bit 07)

When set, this bit indicates that one column of data has been read by the card reader, loaded into the controller data buffer, and is ready for transfer to the bus.

The two data inputs to the COLUMN READY J/K flip-flop are from the 0 sides of the TIMING ERROR and EJECT flip-flops. COLUMN READY can never be set if a TIMING ERROR exists or if an EJECT command has been issued. When the card reader completes reading of one column, it generates an INDEX MARKER signal which is gated through the controller logic to become STROBE H as explained in Paragraph 5.4.5. This signal clocks the inputs, thereby setting the COLUMN READY flip-flop if no EJECT command has been given.

When set, the output of the COLUMN READY flip-flop places a logic 1 on the bus data line 07 driver to indicate data is ready to be transferred. The output also qualifies the interrupt gates to produce INT A H so that the interrupt control logic can initiate an interrupt request, provided the INT ENB A bit is also set. The purpose of this interrupt request is to allow the data in the data buffer to be read from the bus.

The COLUMN READY flip-flop is cleared whenever the data buffer or the data buffer encoding network is addressed. This is accomplished by an OR gate connected to the direct clear input of the flip-flop. The OR gate is qualified by either a SELECT 2 (read data buffer) or SELECT 4 (read encoding network) signal.

5.4.10 INTERRUPT ENABLE (Bit 06)

When set, this bit permits an interrupt to occur provided one of the following bits is also set: ERROR, CARD DONE, TRANSITION TO ON-LINE, or COLUMN READY.

Loading a 1 into status register bit 06 sets the INT ENB A flip-flop. The 1 on the data line is the data input to the flip-flop; the clock input is LOAD STATUS H, which is the result of ANDing SELECT 0 H and OUT LOW H (the two signals that are true when the status register has been addressed for loading the low byte). The output of the flip-flop, which is INT ENB A H, is applied to one input of an AND gate in the interrupt control logic. The other input to the AND gate is INT A H, which is produced by the interrupt OR gates whenever one of the four conditions mentioned above exists. The INT ENB A H signal is also applied to a bus driver to place a 1 on bus data line 06.

The INT ENB A flip-flop is cleared by INIT or by loading bus data line 06 with a 0.

5.4.11 EJECT (Bit 01)

When set, this bit indicates that a card is to be ejected (not transferred to the bus). This is accomplished by preventing the COLUMN READY flip-flop from setting. Although transfers to the bus are inhibited, transfers between the card reader and the controller still take place. Note that setting EJECT does not start card motion; this is accomplished only by the READ bit.

It should be noted that EJECT has no effect on the card reader itself. The reader continues to read the card a column at a time and transfer the data to the data buffer register in the controller. Because the buffer is loaded with new data without reading the previous data, a TIMING ERROR should normally occur. This is prevented, however, because the COLUMN READY flip-flop remains clear. A TIMING ERROR indication has no significance during an EJECT operation because the controller has no interest in the data until a CARD DONE flag is set to indicate that the card is out of the read station.

Loading a 1 into status register bit 01 sets the EJECT flip-flop. The 1 on the data line is the data input to the flip-flop; the clock input is LOAD STATUS H (refer to Paragraph 5.4.10). When the EJECT flip-flop is set, the 0 side goes low and holds one of the inputs to the COLUMN READY flip-flop low, preventing it from being set. The 1 side of the flip-flop is applied to a bus driver to place a logic 1 on the bus data line 01 driver.

5.4.12 READ (Bit 00)

When set, this bit causes the card reader feed mechanism to deliver one card to the read station for reading. The READ command is the only signal sent to the card reader by the controller.

The data input to the READ flip-flop comes from bus data line 00 and is high when a 1 is loaded into this bit position. The clock signal, LOAD STATUS H, is the result of ANDing SELECT 0 H and OUT LOW H. These latter two signals indicate that the low byte of the status register has been addressed for loading. Thus, whenever a 1 is loaded into bus line 00, the READ flip-flop is set. When set, the 0 side of the flip-flop passes through an inverter and is applied to the card reader as the READ COMMAND.

NOTE

Although READ COMMAND is the terminology used in the controller and some card readers, other card readers use the term PICK COMMAND. READ COMMAND and PICK COMMAND are synonomous.

Unlike other bits in the status register, the READ flip-flop output is not connected to a bus driver for reading. Therefore, this bit position is always read as 0.

An OR gate connected to the direct clear input of the READ flip-flop enables the flip-flop to be cleared if any one of three conditions occur: a BUS INIT signal is generated; the card reader ready line drops (READY H goes low), indicating that the card reader has gone off-line for some reason; or the CLR READ H signal goes low. This last signal goes low when INDEX MARKER is high (STROBE H is true), indicating that a column of data was sensed.

It should be noted that the READ command is used only to initiate operation of the reader and to cause a card to be moved from the input hopper to the read station. Once actual card reading begins, the READ COMMAND drops and the reader supplies a signal to the controller that signifies it is busy. This signal is CIR (GDI readers) or BUSY (when using Documation readers).

5.5 DATA BUFFER REGISTER

During read operations, the data buffer register receives and stores the data read by the card reader. Once a complete column is read and stored, the contents of the buffer are placed on the Unibus drivers for transfer to the memory or other bus device. The data buffer register and associated output gating logic is shown on drawing CR-2.

The data buffer register consists of 12 flip-flops, each flip-flop corresponding to one zone of a card column. The data input line of each flip-flop is connected to a corresponding data line in the card reader. As the card column is read, the card reader places either a 1 or 0 on the appropriate data line, depending on what is punched in the card.

NOTE

Although the buffer functionally consists of 12 flip-flops, it physically consists of three 4015 ICs. There are four flip-flops mounted on each IC register. Refer to Appendix D for schematics of this circuit.

After the entire column is read and the data has had time to settle, the card reader issues an INDEX MARKER signal. This signal is used by the controller to produce STROBE H, which is the clock input for each flip-flop. Thus, when the INDEX MARKER is issued by the card reader, STROBE H clocks the information on the data lines into the flip-flops. At this point, the status of each flip-flop corresponds to the information that was placed on the corresponding data line by the card reader.

In order to read the data buffer register, either the register itself (CRB1) or the encoding network (CRB2) must be addressed. This paragraph only covers operation of the data buffer; the encoding network is covered in Paragraph 5.6.

When CRB1 is addressed, SELECT 2 H is true. The SELECT 2 H signal is the enabling input for 12 gates. The other input for each gate comes from the 1 side of a corresponding flip-flop in the data buffer register. Thus, when the data buffer register is addressed, the data in the 12 flip-flops is gated through to the 12 bus data lines as a card image.

The STROBE H signal, which was used to load data into the register, is generated by passing the INDEX MARKER signal from the card reader through inverters and an AND gate that is qualified only if no TIMING ERROR is present [TIMING ERROR (0) H]. If a TIMING ERROR is present, STROBE H is not generated, and the data register cannot be loaded. For a description of the TIMING ERROR logic, refer to Paragraph 5.4.5.

5.6 ENCODING NETWORK

The encoding network is used to compress the 12-bit data character from the card reader into an 8-bit data character that is transferred to the Unibus as a low-order byte.

If the encoding network is selected, data is loaded into the data buffer register in the same manner as before (refer to Paragraph 5.5). However, when the bus is addressed for reading, a different set of drivers is used to gate the output of the register onto the bus.

When the encoding network (CRB2) is addressed, SELECT 4 H is true and SELECT 2 H is false. The normal output gates cannot be enabled because SELECT 2 H is false. The SELECT 4 H signal enables a second set of eight gates that are tied to the data buffer in a different manner. The five most significant bits of the buffer are tied directly to gates representing bus data lines 07 through 03. The seven least significant bits of the buffer are tied to an encoding network that provides three output lines which are tied to the gates driving bus data lines 02, 01, and 00.

The encoding network is simply a series of OR gates that convert the first seven bits of the buffer into an octal code representing the appropriate card zone. A truth table for this network is given in Table 5-5. In effect, the 12-bit character from the reader is compressed into an 8-bit character with the last three bits of the character representing an octal code defining a specific card zone. If more than one of Zones 1 through 7 are asserted, then bits 02, 01, and 00 read as the inclusive OR of the asserted bits.

Table 5-5
Encoding Network Truth Table

Bus Data Line 02	Bus Data Line 01	Bus Data Line 00	Card Zone Represented
0	0	0	zero (no punches in any zone from 1 to 7)
0	0	1	Zone 1
0	1	0	Zone 2
0	1	1	Zone 3
1	0	0	Zone 4
1	0	1	Zone 5
1	1	0	Zone 6
1	1	1	Zone 7

APPENDIX A
GDI CARD READERS

A.1 SCOPE

This appendix provides the user with pertinent information on the GDI 100 Punched Card Reader and the GDI 100M Mark Sense Card Reader in the event one of these card readers is used with the CR11 Card Reader Controller. The CR11 Controller is completely compatible with both GDI card readers and no modifications or special connections are required when one of these units is used in place of the Documation card reader. Note, however, that the two status register jumpers may or may not be removed depending on which of the two readers is used.

Specifications for the GDI Card Readers are listed in Table 1-4. The following paragraphs provide general descriptions and operating controls of the GDI 100 (Paragraph A.2) and the GDI 100M (Paragraph A.3) card readers.

A.2 GDI MODEL 100 CARD READER

The GDI Model 100 Card Reader (Figure A-1) accepts information from EIA standard punched data cards. It reads 12-row, 80-column punched cards at a nominal rate of 200 cards per minute by means of a photoelectric process. The card reader consists of a motorized card-transport deck, a photoelectric read station, and control and error detection logic.

Information from this reader may be read in either the complete 12-bit format or in the 8-bit format generated by the controller compression logic.

When the GDI Model 100 Card Reader is used with the controller, the jumpers for status register bits 13 and 12 (CARD SUPPLY ERROR and READER CHECK) must be removed because these two bits are not provided by the punched card readers.

Specifications for the Model 100 card reader are presented in Table 1-4. A list of signal names is presented in Appendix B. The operating controls and indicators are covered in Table A-1 and shown in Figure A-2.

Additional information on this card reader, such as maintenance and theory of operation, is covered in the appropriate GDI Technical Manual.

Table A-1
GDI Model 100 Controls and Indicators

Control or Indicator	Type	Function
ON/OFF switch	2-position toggle	When set to ON (up) position, applies primary power to all card reader circuits except the main drive motor.
MOTOR START switch	pushbutton	When depressed, applies power to main drive motor and lights the associated MOTOR START indicator.

(continued on next page)

Table A-1 (Cont)
GDI Model 100 Controls and Indicators

Control or Indicator	Type	Function
MOTOR START switch (cont)		Clears all error indicators provided the error condition has been corrected. This switch cannot operate if any one of the following error conditions exists: *a.* input hopper empty (HOPPER EMPTY light is on) *b.* output stacker is full (STACKER FULL light is on) *c.* all photocells are not lit (LIGHT CHECK light is on) *d.* internal power supply is not functioning properly (all indicators off; MOTOR START fails to operate).
READ START switch	pushbutton	When depressed, causes READY line to go high, thereby placing card reader under program control (on-line). Lights associated READ START indicator. If READ COMMAND from controller is open or high when this switch is depressed, card reading begins immediately at full rated speed.
READ STOP switch	pushbutton	When depressed, inhibits further card reading by dropping READY line. Lights associated READ STOP indicator. Drive motor continues running.
MOTOR START indicator	green light	When lit, indicates that power has been applied to main drive motor and that all error conditions and indicators have been cleared.
READ START indicator	green light	When lit, indicates that reader READY line is high and that reader can be operated on-line under program control.
READ STOP indicator	red light	When lit, indicates that the reader has been stopped manually if the drive motor is still running. If the drive motor has stopped and this indicator is lit, indicates that an error condition stopped card reader operation.
PICK FAIL indicator	red light	When lit, indicates that the reader failed to move a card into the read station after it received a READ COMMAND from the controller. Stops reader operation, lights READ STOP indicator, extinguishes READ START.

(continued on next page)

Table A-1 (Cont)
GDI Model 100 Controls and Indicators

Control or Indicator	Type	Function
DARK CHECK indicator	red light	When lit, indicates photocells are not dark at hypothetical 0 and 81st hole positions. Stops reader operation, lights READ STOP indicator, extinguishes READ START. Inhibits all data outputs of the reader.
STACKER FAIL indicator	red light	When lit, indicates that three cards have passed the read station and none have been stacked. Prevents more than three cards from being in the card track at once. Stops reader operation, lights READ STOP indicator, extinguishes READ START.
HOPPER EMPTY indicator	red light	When lit, indicates that input hopper is empty. Operator must reload hopper before operation can continue. Stops reader operation, lights READ STOP indicator, extinguishes READ START.
STACKER FULL indicator	red light	When lit, indicates that output stacker is full (approximately 400 cards). Operator must unload stacker before operation can continue. Stops reader operation, lights READ STOP indicator, extinguishes READ START.
SYNC FAIL indicator	red light	When lit, indicates that the internal timing signals have been lost. Stops reader operation, lights READ STOP indicator, extinguishes READ START.
LIGHT CHECK indicator	red light	All photocells are lit except during the time a card is read. The detector is inhibited each time the card enters the read station until a position of 84. If a card fails to leave the read station by this time, the LIGHT CHECK indicator lights. Stops reader operation, lights READ STOP indicator, extinguishes READ START.

A.3 GDI MODEL 100M CARD READER

The GDI Model 100M Optical Mark Reader (Figure A-3) reads either marked or punched Hollerith data cards with timing marks. The reader reads 12-row, 40-column, mark sensed cards and 12-row, 40-column punched cards. No special pencil is needed for recognition of the mark sensed cards.

The Model 100M automatically compensates for variations in average card reflection, thereby enabling the reader to accurately retrieve data even from soiled or excessively handled cards.

Information from this reader may be read in either the complete 12-bit format or in the 8-bit format generated by the controller compression logic.

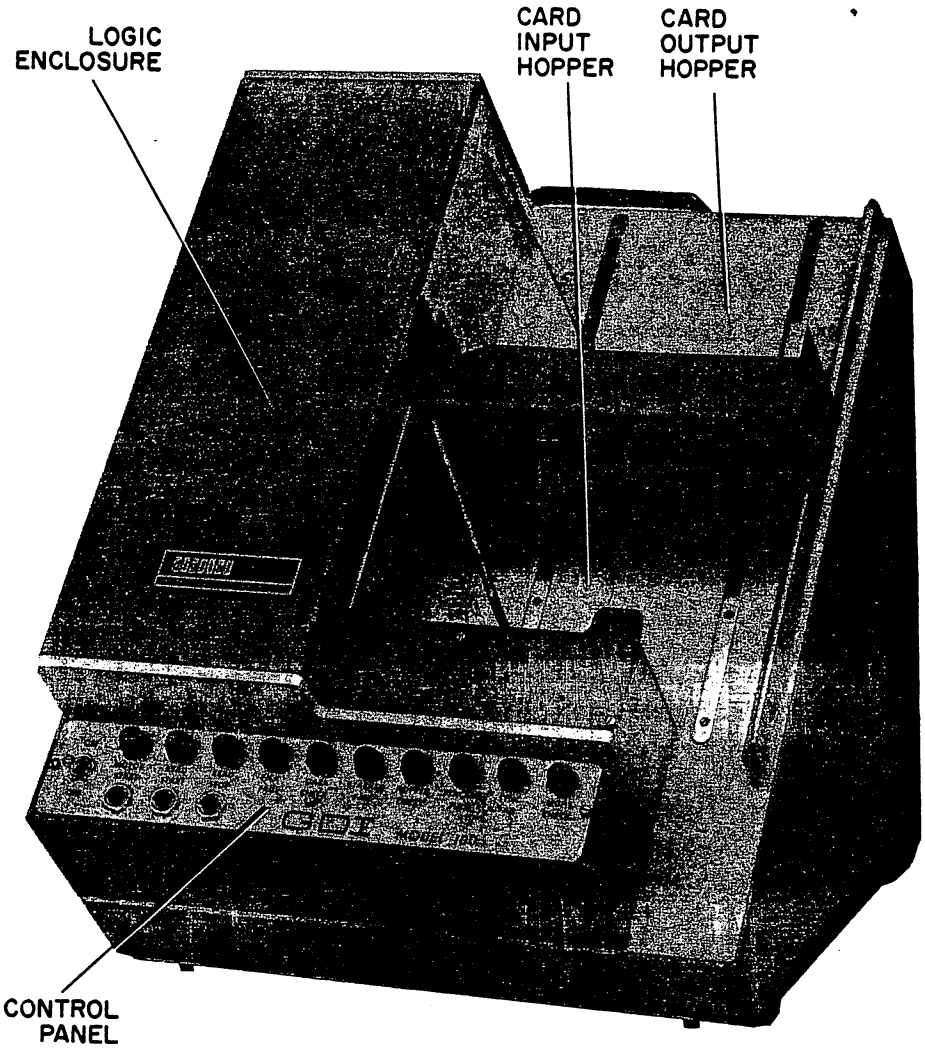


Figure A-1 GDI Model 100 Card Reader

Figure A-2 GDI Model 100 Control Panel

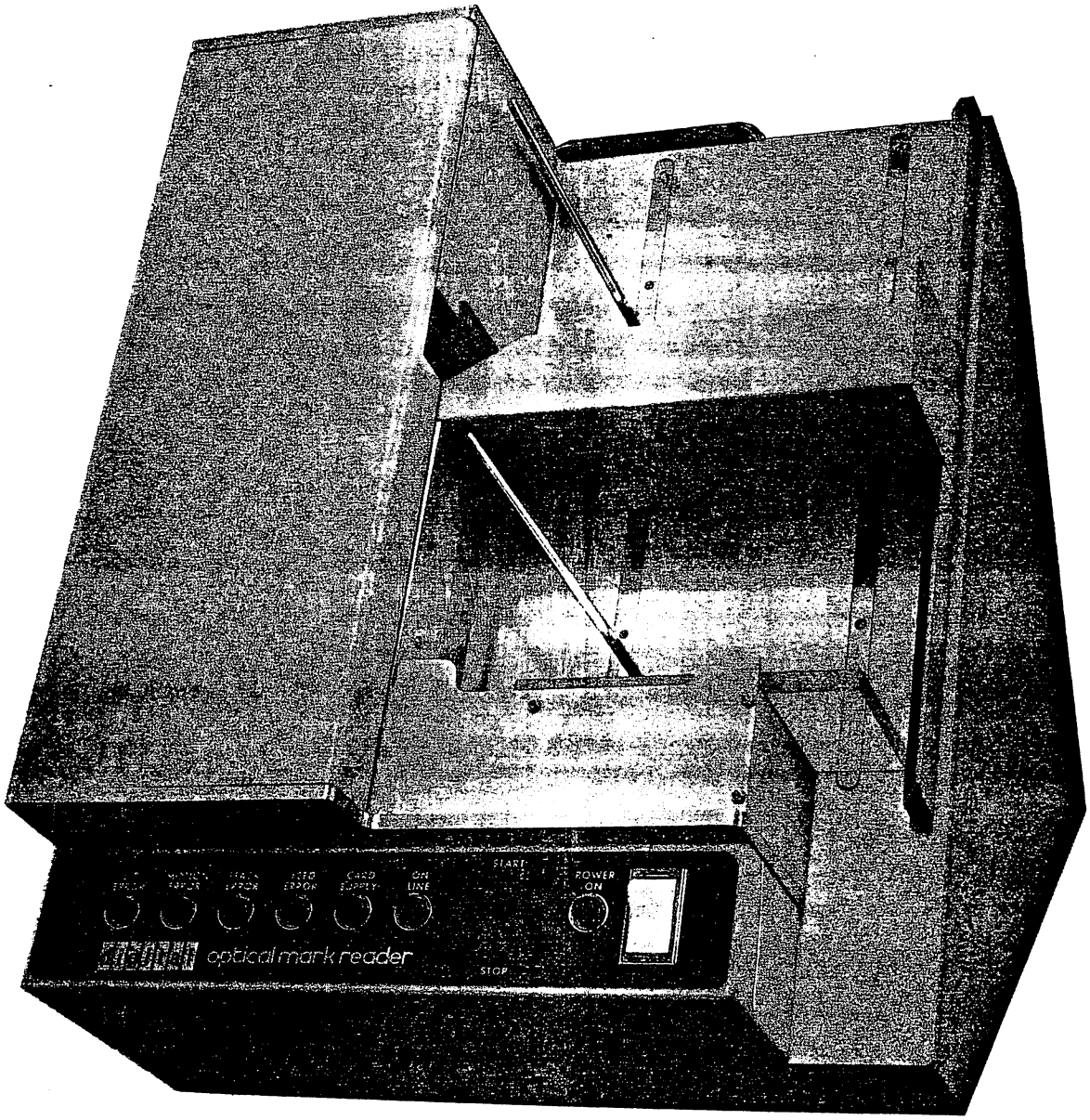


Figure A-3 GDI Model 100M Optical Mark Reader

When the GDI Model 100M Reader is used with the controller, the jumpers for status register bits 13 and 12 are **not to be removed** because both CARD SUPPLY ERROR and READER CHECK signals are provided by this reader.

Specifications for the Model 100M card reader are presented in Table 1-4. A list of signal names is presented in Appendix B. The operating controls and indicators are shown in Figure A-4 and described in Table A-2.

Additional information on this card reader, such as maintenance and theory of operation, is covered in the appropriate GDI Technical Manual.

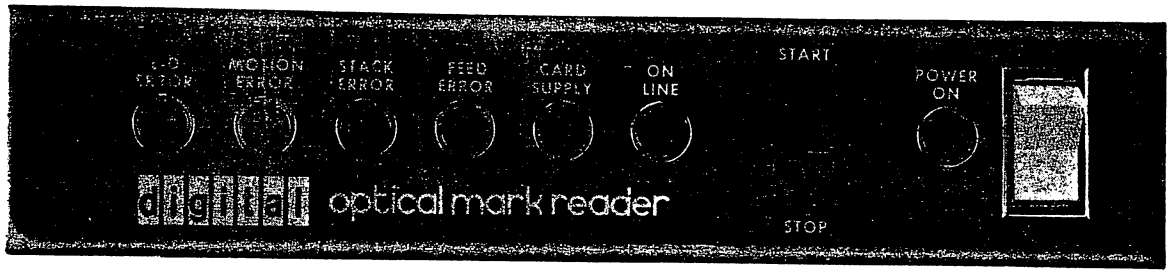


Figure A-4 GDI Model 100M Control Panel

Table A-2
GDI Model 100M Controls and Indicators

Control or Indicator	Type	Function
POWER ON switch	2-position rocker	When upper portion of switch is depressed, applies primary power to all card reader circuits except drive motor. Depressing lower portion of switch removes all power from reader.
POWER ON indicator	green light	When lit, indicates that primary ac power has been applied to the reader.
START switch	pushbutton	When depressed, starts main drive motor and resets all error indicators provided the error condition has been corrected. Upon releasing switch and allowing motor to come up to speed, the reader can accept a READ COMMAND from the controller and start processing cards. Lights ON LINE indicator.
STOP switch	pushbutton	When depressed, stops reader operation by stopping main drive motor. If this switch is depressed while card reading is in process, the current card cycle is completed before the motor stops. Extinguishes ON LINE indicator.
ON LINE indicator	green light	When lit, indicates that the reader is on-line and able to accept commands from the controller. This light comes on when the START switch is depressed. This light goes out whenever the STOP switch is depressed or whenever an error condition occurs.
CARD SUPPLY indicator	red light	When lit, indicates that either the input hopper is empty or that the output stacker is full. Condition must be corrected by the operator before card reading can continue. Stops reader operation and extinguishes ON LINE indicator.

(continued on next page)

Table A-2 (Cont)
GDI Model 100M Controls and Indicators

Control or Indicator	Type	Function
FEED ERROR indicator	red light	When lit, indicates that the card reader failed to move a card into the read station after it received a READ COMMAND from the controller. Stops card reader operation and extinguishes ON LINE indicator.
STACK ERROR indicator	red light	When lit, indicates that a card was not properly delivered to the output stacker after the read operation. Stops card reader operation and extinguishes ON LINE indicator.
MOTION ERROR indicator	red light	When lit, indicates a card jam in the read station. Stops card reader operation and extinguishes ON LINE indicator.
L.D. ERROR indicator	red light	When lit, indicates that the card failed to pass the light/dark check at the read station. Stops card reader operation and extinguishes ON LINE indicator.

APPENDIX B
CARD READER INTERFACE SIGNALS

The CR11 Controller is compatible with all GDI, Documation, and equivalent card readers. Each of these readers sends the same basic signals to the controller. However, each card reader manual uses different terminology for the same signal. In order to avoid confusion because of different terminology, a list of all interface signals is presented in Table B-1.

Table B-1 lists all interface signals and includes the terminology used by each reader for the specific signal. A brief description of the signal function is also included. Note that this table is not an attempt to provide interfacing data. The specific pins for each signal are covered in the appropriate reader manual.

Table B-1
Interfacing Signals

Controller	GDI 100	GDI 100M	Documation (all)	Function
READ COMMAND	READ	READ	PICK COMMAND	Initiates reader operation by causing reader feed mechanism to deliver one card to the read station for reading. This is the only signal from the controller to the card reader.
ZONE	DATA	DATA	DATA	12 parallel lines containing data read from 12 corresponding column zones.
INDEX MARKER	INDEX MARKERS	DATA STROBE	INDEX MARK	Timing mark indicating that one column of data has been read and can now be strobed into the controller buffer.
READY	READY	ON-LINE X+	READY	Indicates card reader is on-line and can accept a READ command
CIR	CARD IN READER	CARD IN READER	BUSY	Indicates card reader is engaged in reading a card and cannot accept a READ command at this time.
READER CHECK	None	READER CHECK	MOTION CHECK	Indicates certain error conditions within the reader such as a card jam. Error indication dependent on reader used.
CARD SUPPLY ERROR	None	SUPPLY ERROR	HOPPER CHECK	Indicates input hopper empty or output stacker full.

APPENDIX C
HOLLERITH CODE

Card Code		Compressed Code (octal)	Character	Card Code		Compressed Code (octal)	Character
Zone	Number			Zone	Number		
--	-	000	Blank	11-0	--	-	Invalid
12	8-2	212	?	11	1	101	J
12	8-3	213	.	11	2	102	K
12	8-4	214	)	11	3	103	L
12	8-5	215	]	11	4	104	M
12	8-6	216	<	11	5	105	N
12	8-7	217	!	11	6	106	O
12	-	200	+	11	7	107	P
11	8-2	112	:	11	8	110	Q
11	8-3	113	$	11	9	120	R
11	8-4	114	*	0	8-2	052	;
11	8-5	115	[	0	2	042	S
11	8-6	116	>	0	3	043	T
11	8-7	117	&	0	4	044	U
11	-	100	-	0	5	045	V
0	1	051	/	0	6	046	W
0	8-3	053	,	0	7	047	X
0	8-4	054	(	0	8	050	Y
0	8-5	055	"	0	9	060	Z
0	8-6	056	#	0	--	040	0
0	8-7	057	%	-	1	001	1
-	8-2	-	Invalid	-	2	002	2
-	8-3	013	=	-	3	003	3
-	8-4	014	@	-	4	004	4
-	8-5	015	↑	-	5	005	5
-	8-6	016	,	-	6	006	6
-	8-7	017	\	-	7	007	7
12-0	--	--	Invalid	-	8	010	8
12	1	201	A	-	9	020	9
12	2	202	B				
12	3	203	C				
12	4	204	D				
12	5	205	E				
12	6	206	F				
12	7	207	G				
12	8	210	H				
12	9	220	I				

APPENDIX D
INTEGRATED CIRCUIT DESCRIPTION

This appendix provides diagrams, schematics, and a truth table for the 4015 integrated circuit (IC) used in the CR11 Controller. The 4015 IC can functionally be used as four separate flip-flops or as a 4-bit register. The diagrams are shown in Figures D-1 through D-3 and the truth table is given in Table D-1.

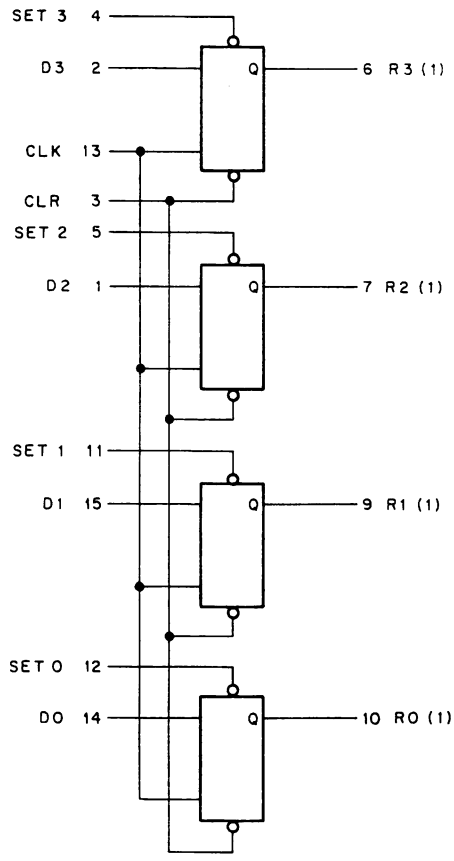
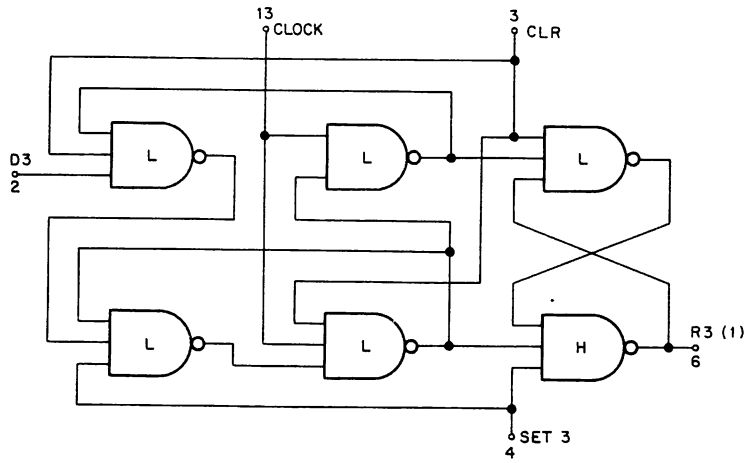


Figure D-1 Functional Logic Diagram



1/4 OF DEVICE SHOWN

CLOCK AND $\overline{\text{RESET}}$ COMMON TO ALL FOUR FLIP-FLOPS

V_{CC} = PIN 16

GND = PIN 8

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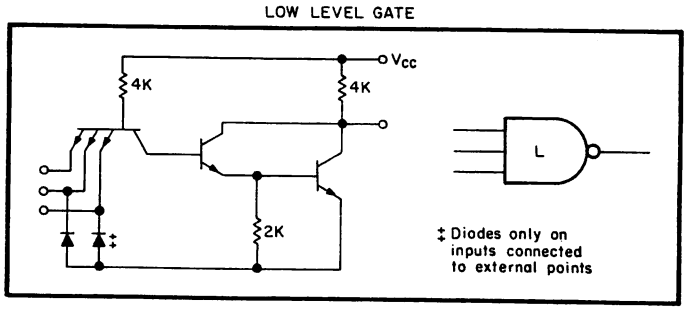
Figure D-2 Logic Schematic



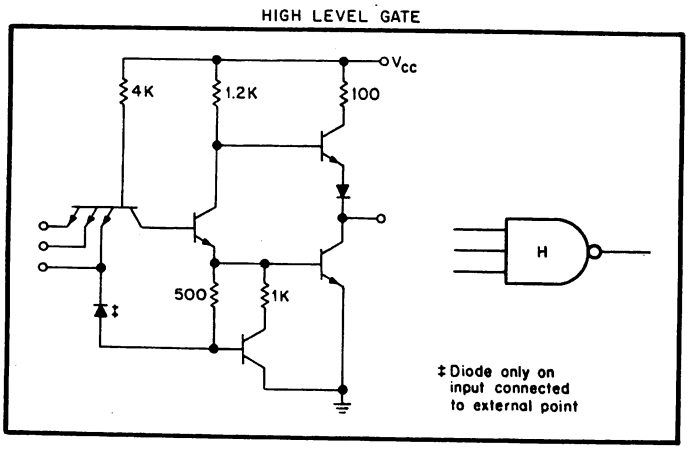


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Figure D-3 Circuit Schematic

Table D-1
Truth Table

D	Q_{n-1}	Q_n
0	0	0
0	1	0
1	0	1
1	1	1

Q_{n-1} = time period prior to clock pulse

Q_n = time period following clock pulse